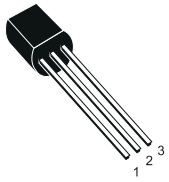
STQ1HNC60

N-CHANNEL 600V - 7Ω - 0.4A TO-92
PowerMesh™II MOSFET

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STQ1HNC60	600 V	< 8 Ω	0.4 A

- TYPICAL $R_{DS}(on)$ = 7 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

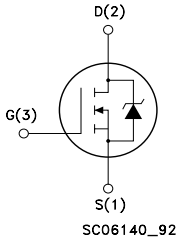


TO-92

DESCRIPTION

Using the latest high voltage MESH OVERLAY™II process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- SWITCH MODE LOW POWER SUPPIES (SMPS)
- CFL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	600	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	600	V
V_{GS}	Gate- source Voltage	± 30	V
I_D	Drain Current (continuos) at T_C = 25°C	0.4	A
I_D	Drain Current (continuos) at T_C = 100° C	0.25	A
I_{DM} (●)	Drain Current (pulsed)	1.6	A
P_{TOT}	Total Dissipation at T_C = 25° C	3.5	W
	Derating Factor	0.028	W/° C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T_{stg}	Storage Temperature	–65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I_{SD} ≤ 0.4 A, di/dt ≤100A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	35.7	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max (Surface Mounted)	60	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300	℃

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	0.4	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	100	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 0.4 A		7	8	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, I_D = 0.4 A		1.25		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		160		pF
C_{oss}	Output Capacitance			26		pF
C_{rss}	Reverse Transfer Capacitance			3.8		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 300V, I_D = 0.7 A		8		ns
t_r	Rise Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 3)		8		ns
Q_g	Total Gate Charge	V_{DD} = 480V, I_D = 1.4 A,		8.5	11.5	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10V, R_G = 4.7Ω		2.8		nC
Q_{gd}	Gate-Drain Charge			2.8		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 480 V, I_D = 1.4 A,		25		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		9		ns
t_c	Cross-over Time			34		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				0.4	A
I_{SDM} (2)	Source-drain Current (pulsed)				1.6	A
V_{SD} (1)	Forward On Voltage	I_{SD} = 0.4 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 1.4 A, di/dt = 100A/µs,		500		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 100V, T_j = 150° C (see test circuit, Figure 5)		950		µC
I_{RRM}	Reverse Recovery Current			3.8		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

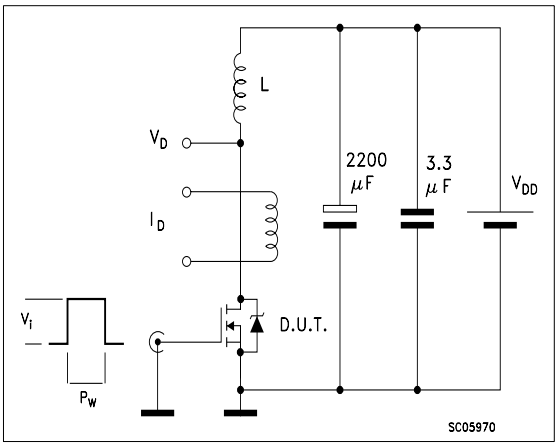


Fig. 2: Unclamped Inductive Waveform

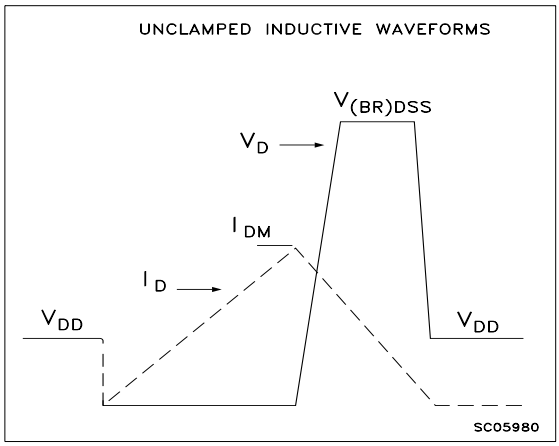


Fig. 3: Switching Times Test Circuit For Resistive Load

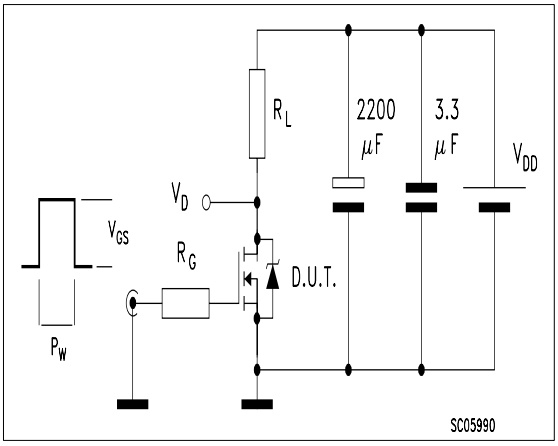


Fig. 4: Gate Charge test Circuit

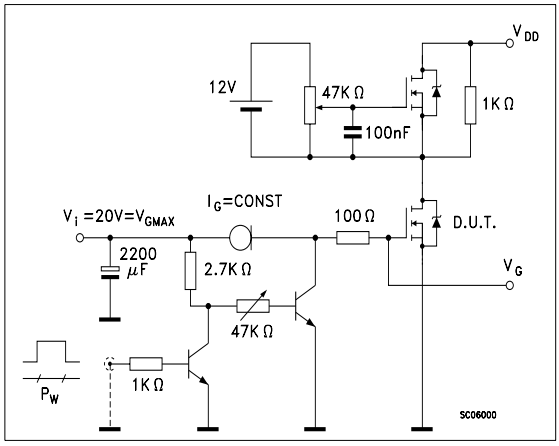
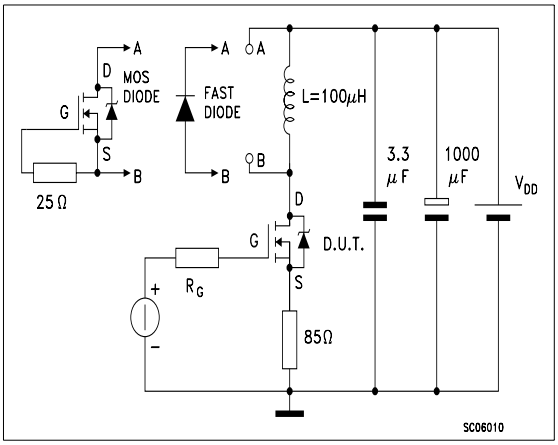


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-92 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.58		5.33	0.180		0.210
B	4.45		5.2	0.175		0.204
C	3.2		4.2	0.126		0.165
D	12.7			0.500		
E		1.27			0.050	
F	0.4		0.51	0.016		0.020
G	0.35			0.14