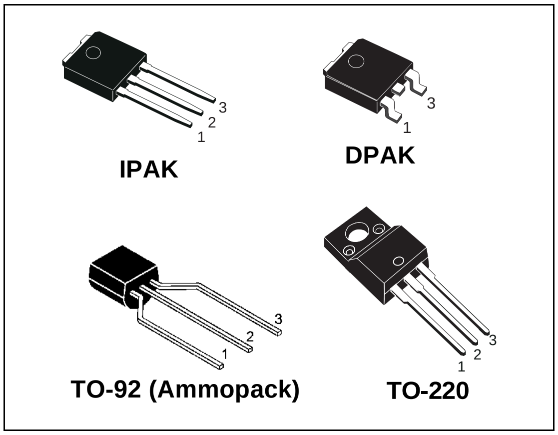
STD2HNK60Z - STD2HNK60Z-1
STF2HNK60Z - STQ2HNK60ZR-AP

N-channel 600V - 4.4Ω - 2A - TO-92/TO-220FP/DPAK/IPAK Zener-protected SuperMESH™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	P_{TOT}
STD2HNK60Z	600V	<4.8Ω	2A	45W
STD2HNK60Z-1	600V	<4.8Ω	2A	45W
STF2HNK60Z	600V	<4.8Ω	2A	20W
STQ2HNK60ZR-AP	600V	<4.8Ω	0.5A	3W

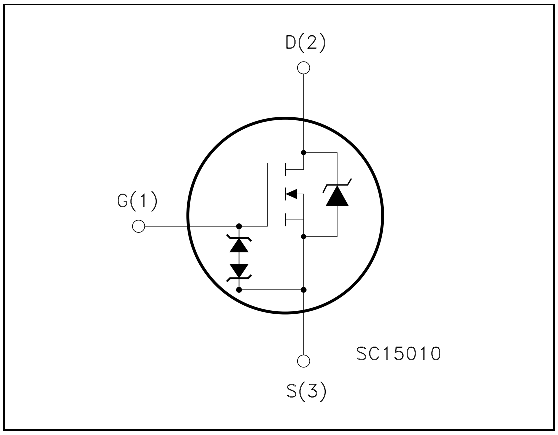
- Gate charge minimized
- 100% avalanche tested
- Extremely high dv/dt capability
- ESD improved capability
- New high voltage benchmark



Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established stripbased PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

Internal schematic diagram



Applications

- Switching application

Order codes

Sales Type	Marking	Package	Packaging
STD2HNK60Z	D2HNK60Z	DPAK	Tape & reel
STD2HNK60Z-1	D2HNK60Z	IPAK	Tube
STF2HNK60Z	F2HNK60Z	TO-220FP	Tube
STQ2HNK60ZR-AP	Q2HNK60ZR	TO-92	Ammopak

Contents:

1 Electrical ratings 3

2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuit 9

4 Package mechanical data 10

5 Revision history 13

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		IPAK/DPAK	TO-220FP	TO-92	
V_{DS}	Drain-Source Voltage (V_{GS} = 0)	600			V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20kΩ)	600			V
V_{GS}	Gate-Source Voltage	±30			V
I_D	Drain Current (continuous) at T_C = 25°C	2.0	2.0	0.5	A
I_D	Drain Current (continuous) at T_C=100°C	1.26	1.26	0.32	A
I_{DM}(1)	Drain Current (pulsed)	8	8	2	A
P_{TOT}	Total Dissipation at T_C = 25°C	45	20	3	W
	Derating Factor	0.36	0.16	0.025	W/°C
$V_{ESD(G-S)}$	Gate Source ESD (HBM-C=100pF, R=1.5kΩ)	2000			V
V_{ISO}	Insulation withstand voltage (DC)	--	2500	--	V
dv/dt(2)	Peak Diode Recovery voltage slope	4.5			V/ns
T_J T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150			°C
T_l	Maximum lead temperature for soldering purpose	300		260	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤2A, di/dt ≤200A/µs, V_{DD} =80%$V_{(BR)DSS}$

Table 2. Thermal data

		IPAK/DPAK	TO-220FP	TO-92	
$R_{thj-case}$	Thermal resistance junction-case Max	2.77	6.25	--	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient Max	100	62.5	120	°C/W
$R_{thj-lead}$	Thermal resistance junction-lead Max	--	--	40	°C/W

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by Tjmax)	2	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, I_D=I_{AR}, V_{DD}=50V)	120	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 1mA, V_{GS}= 0	600			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating, V_{DS} = Max Rating,Tc=125°C			1 50	µA µA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{GS} = ±20V			±10	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D = 50µA	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS}= 10V, I_D= 1.0A		4.4	4.8	Ω

Table 5. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} =15V, I_D = 1.0A		1.5		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		280 38 7		pF pF pF
$C_{oss\ eq}$(2)	Equivalent Output Capacitance	V_{GS}=0, V_{DS} =0V to 480V		30		pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=480V, I_D = 2.0A V_{GS} =10V (see Figure 18)		11 2.25 6	15	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD}=300V, I_D=1.0A, R_G=4.7Ω, V_{GS}=10V (see Figure 17)		10 30		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD}=300V, I_D=1.0A, R_G=4.7Ω, V_{GS}=10V (see Figure 17)		23 50		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain Current Source-drain Current (pulsed)				2.0 8.0	A A
V_{SD}(2)	Forward on Voltage	I_{SD}=2.0A, V_{GS}=0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=2.0A, di/dt = 100A/µs, V_{DD}=20 V, Tj=25°C		178 445 5		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=2.0A, di/dt = 100A/µs, V_{DD}=20 V, Tj=150°C		200 500 5		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-92

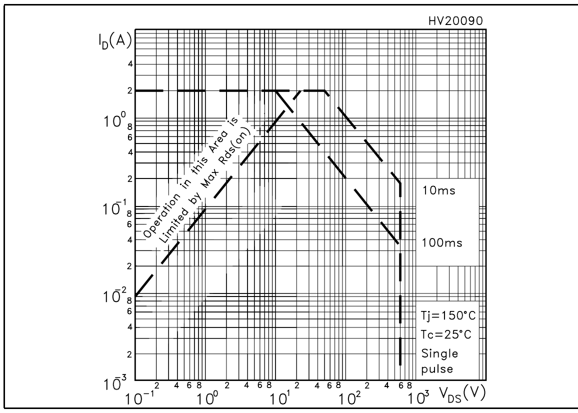


Figure 2. Thermal impedance for TO-92

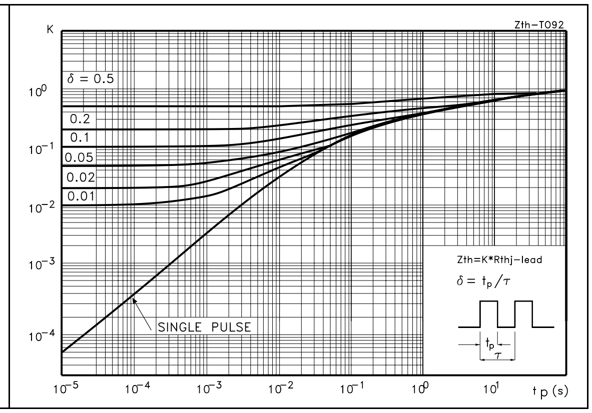


Figure 3. Safe operating area for TO-220FP

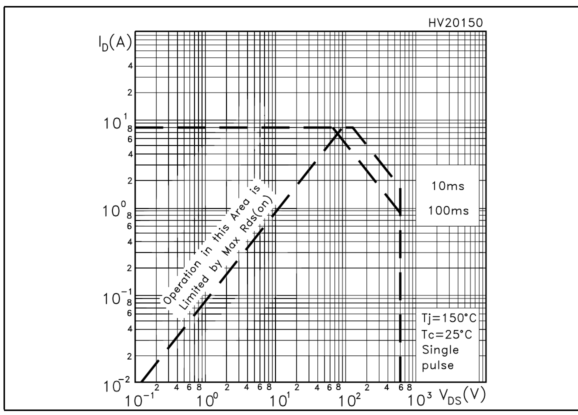


Figure 4. Thermal impedance for TO-220FP

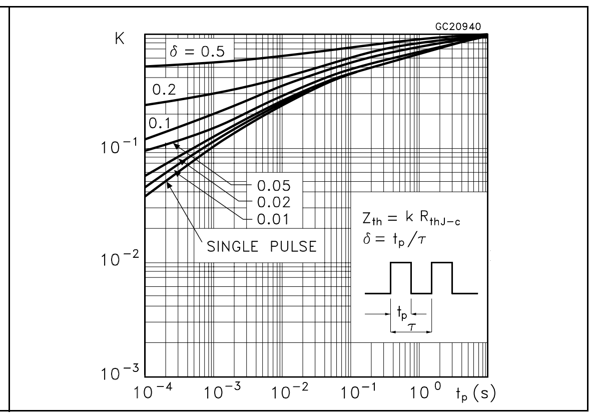


Figure 5. Safe operating area for IPAK/DPAK

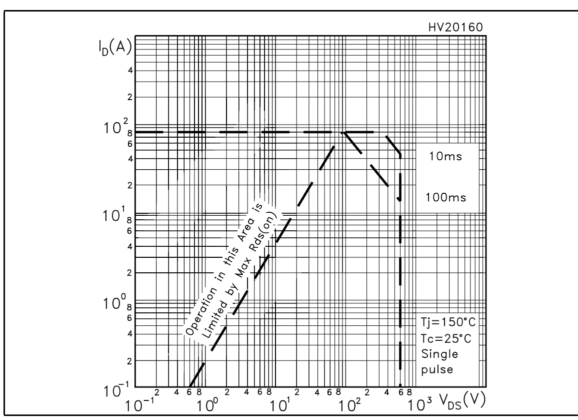


Figure 6. Thermal impedance for IPAK/DPAK

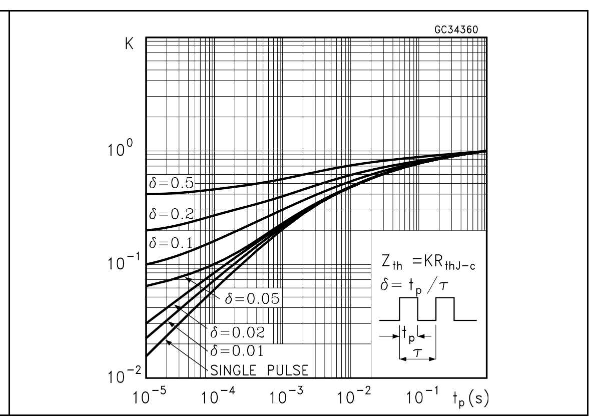


Figure 7. Output characterisics

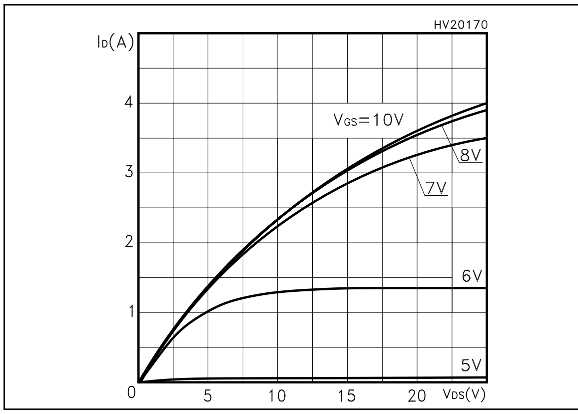


Figure 8. Transfer characteristics

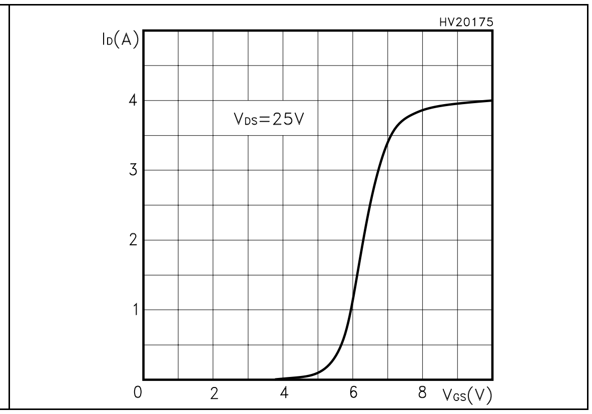


Figure 9. Normalized B_{VDSS} vs temperature

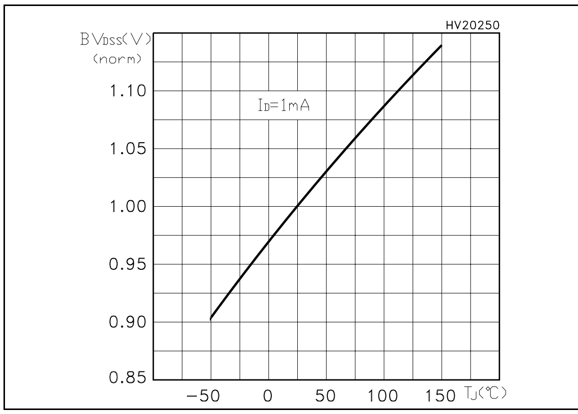


Figure 10. Static drain-source on resistance

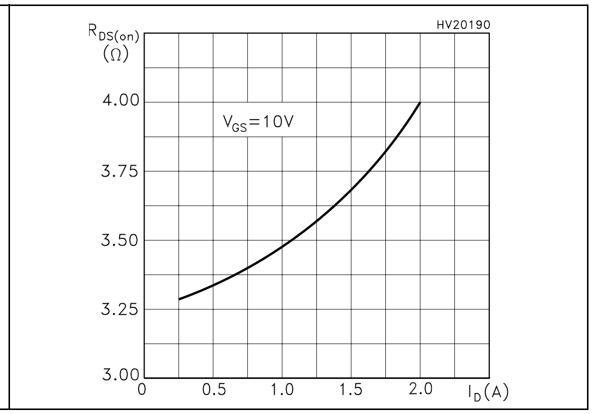


Figure 11. Gate charge vs gate-source voltage

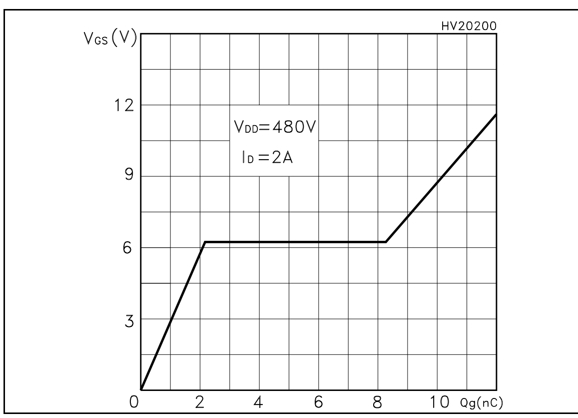


Figure 12. Capacitance variations

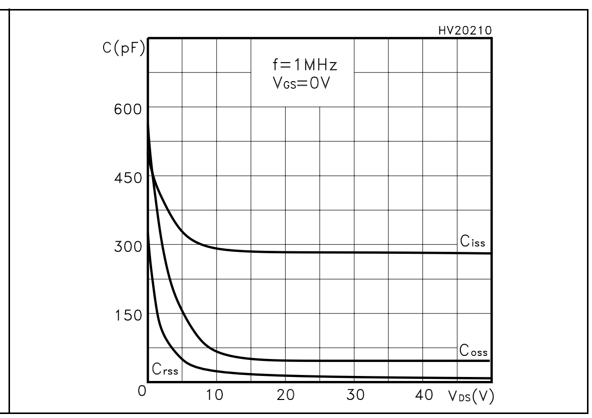


Figure 13. Normalized gate threshold voltage vs temperature

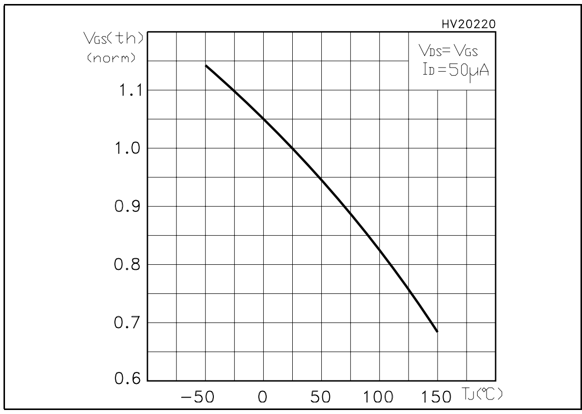


Figure 14. Normalized on resistance vs temperature

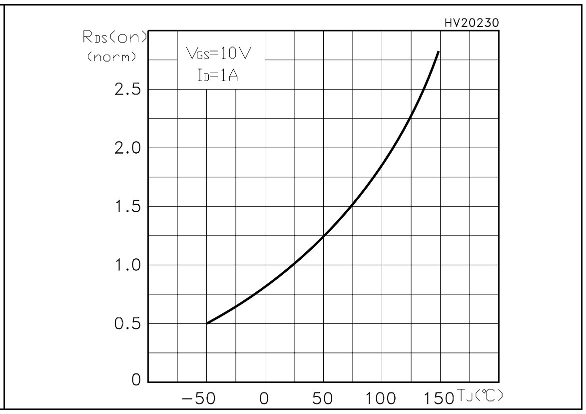


Figure 15. Source-drain diode forward characteristics

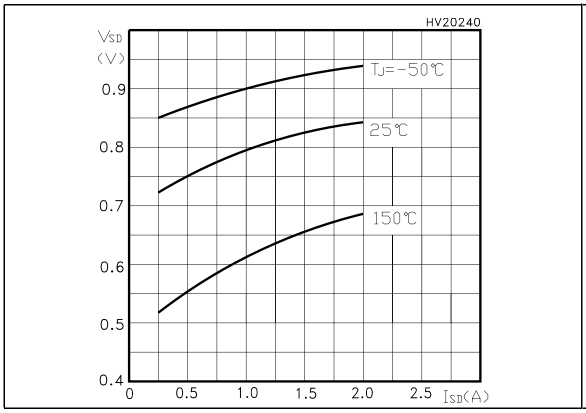
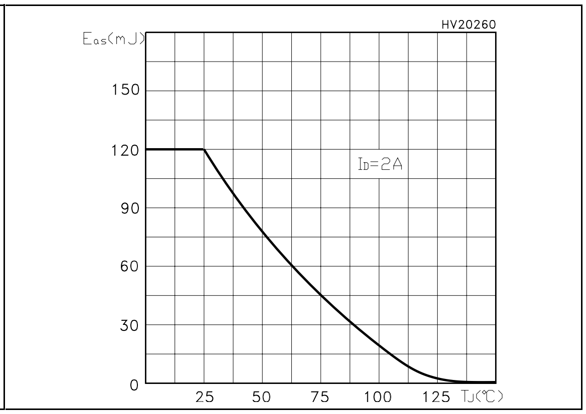


Figure 16. Maximum avalanche energy vs temperature



3 Test circuit

Figure 17. Switching times test circuit for resistive load

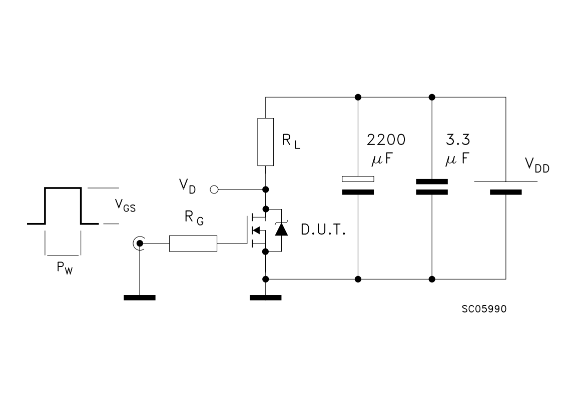


Figure 18. Gate charge test circuit

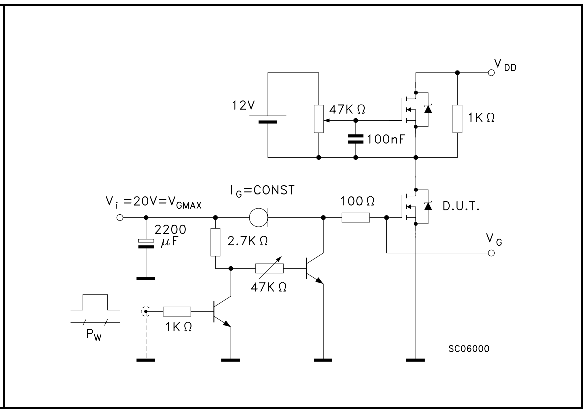


Figure 19. Test circuit for inductive load switching and diode recovery times

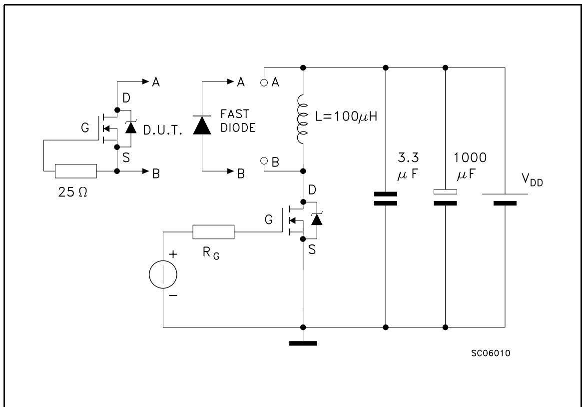


Figure 20. Unclamped inductive load test circuit

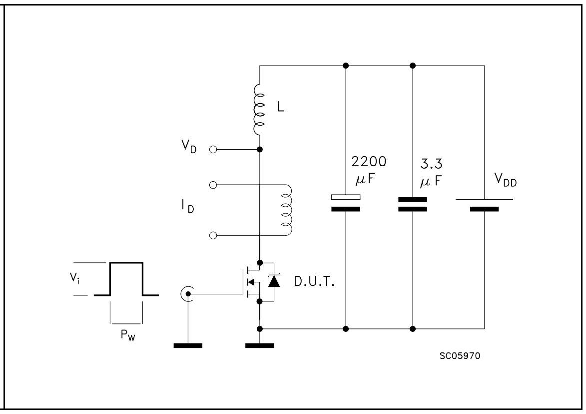


Figure 21. Unclamped inductive waveform

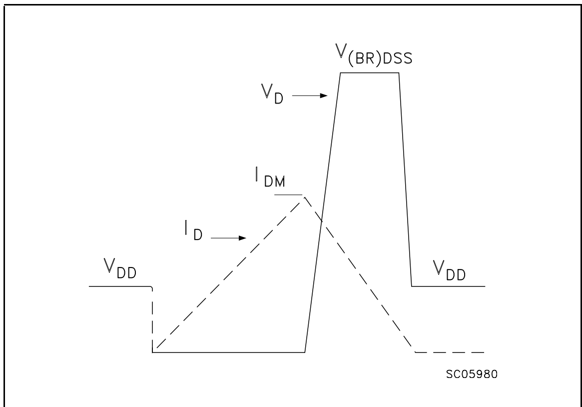
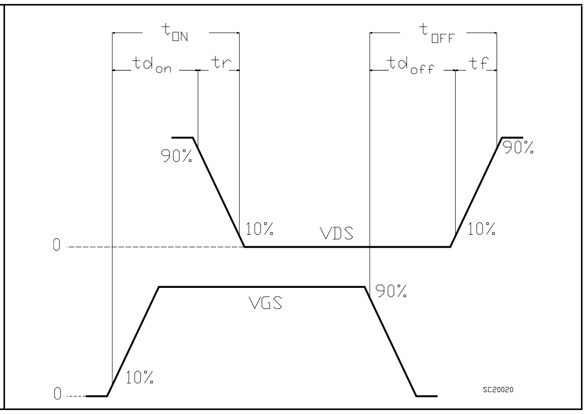


Figure 22. Switching time waveform

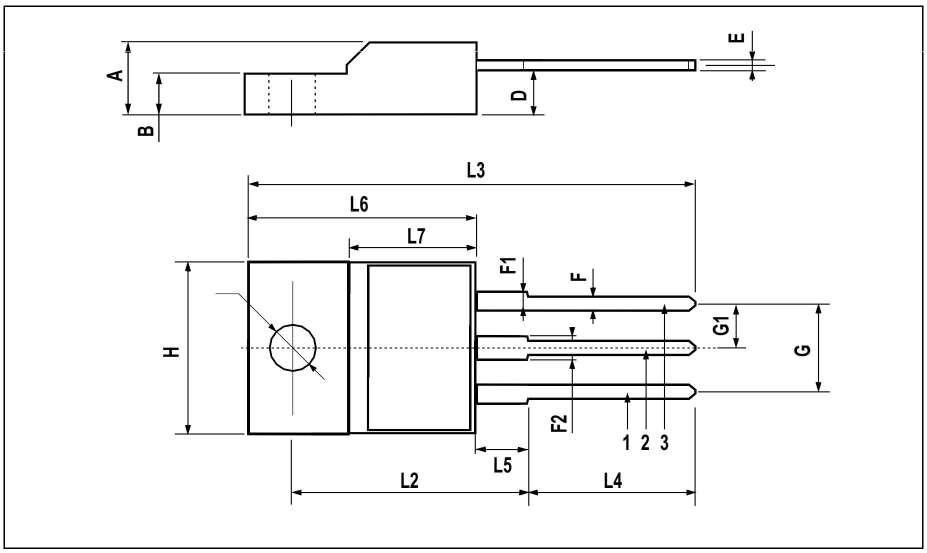


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

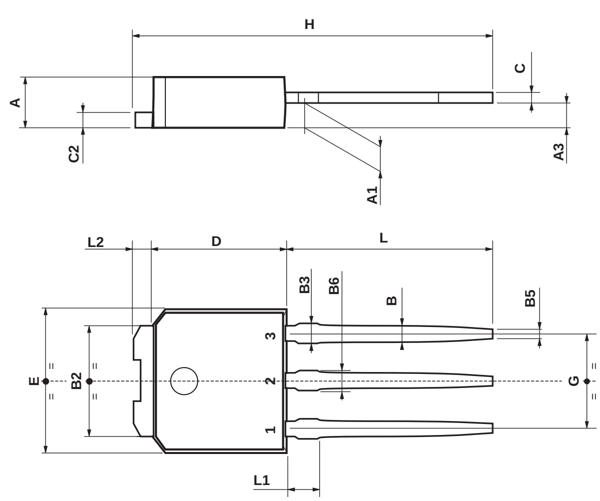
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-251 (IPAK) MECHANICAL DATA

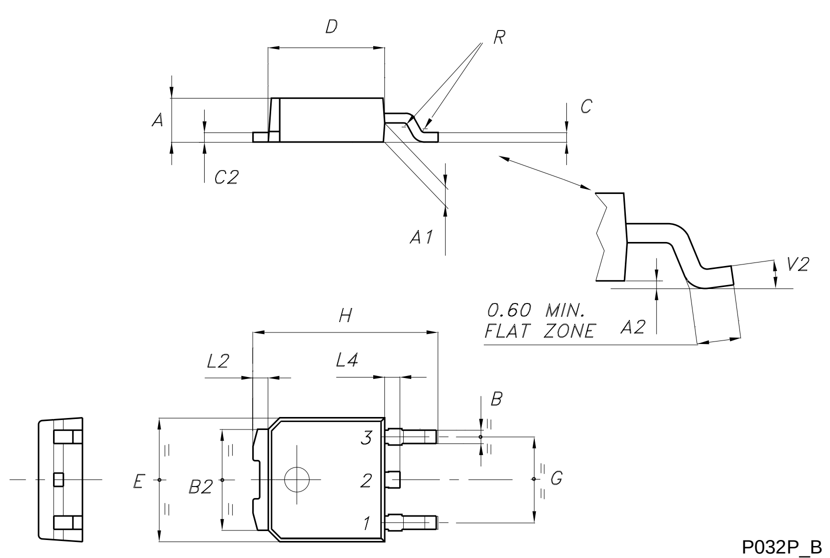
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



0068771-E

TO-252 (DPAK) MECHANICAL DATA

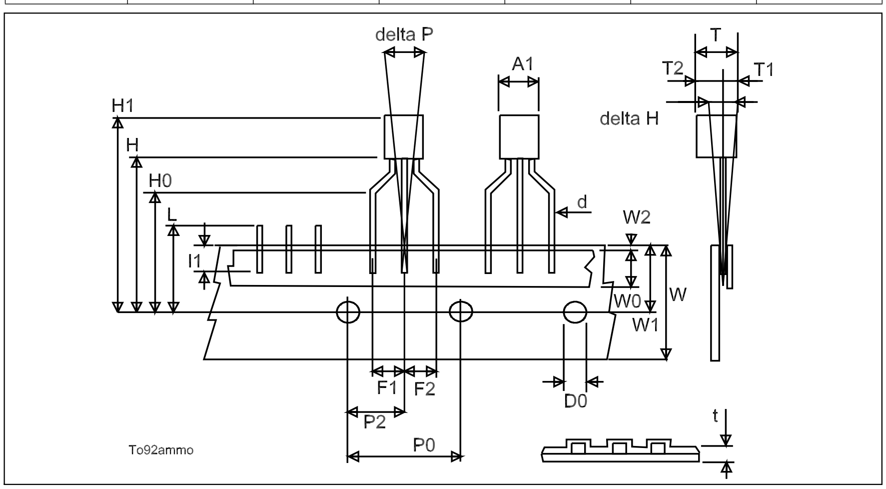
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



P032P_B

TO-92 AMMOPACK

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A1	4.45		4.95	0.170		0.194
T	3.30		3.94	0.130		0.155
T1			1.6			0.06
T2			2.3			0.09
d	0.41		0.56	0.016		0.022
P0	12.5	12.7	12.9	0.49	0.5	0.51
P2	5.65	6.35	7.05	0.22	0.25	0.27
F1, F2	2.44	2.54	2.94	0.09	0.1	0.11
delta H	-2		2	-0.08		0.08
W	17.5	18	19	0.69	0.71	0.74
W0	5.7	6	6.3	0.22	0.23	0.24
W1	8.5	9	9.25	0.33	0.35	0.36
W2			0.5			0.02
H	18.5		20.5	0.72		0.80
H0	15.5	16	16.5	0.61	0.63	0.65
H1			25			0.98
D0	3.8	4	4.2	0.15	0.157	0.16
t			0.9			0.035
L			11			0.43
I1	3			0.11		
delta P	-1		1	-0.04		0.04



5 Revision history

Table 8. Revision history

Date	Revision	Changes
09-Mar-2004	1	First release
23-Mar-2004	2	Modified title
02-Apr-2005	3	Complete version
06-Mar-2006	4	Inserted DPAK. New template