

FUDAN MICROELECTRONICS



复旦微电子

STF1001

Telephone IC Card Chip

Specification

May. 2008

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1. Product Overview

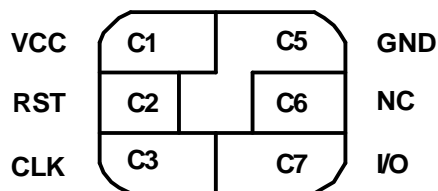
1.1. Description

STF1001 is designed for applications in prepaid cards. The chip is special for China Telecom with a specific Manufacturer Code. STF1001 consists of 104 bit memory and adopts 0.6μm CMOS EEPROM technology. The STF1001 is security ICs for telecom providing 88 bits of serial electrically erasable and programmable read-only memory (EEPROM) for counter with security.

1.2. Features

- 100% functional compatibility to SLE4406
- 88 bits EEPROM and 16 bits ROM
 - 16 bits Manufacturer code (ROM)
 - 48 bits for personalization data of card issuer (EEPROM)
 - 40 bits Counter Area including 1 bit for personalization (EEPROM)
- Counter with up to 37448 count units
 - Five stage counter
 - Due to the personalization bit a maximum of 33352 count units is guaranteed
- Transport Code protection for delivery
- Supply voltage: 4.5V~5.5V
- Supply current < 3mA
- EEPROM programming time 5 ms
- ESD protection minimum 2,000V; typical 4,000V
- Endurance minimum 100,000 write/erase cycles / bit
- Data retention for minimum of 30 years
- Contact configuration and Answer-to-Reset (synchronous transmission) in accordance to standard ISO/IEC 7816

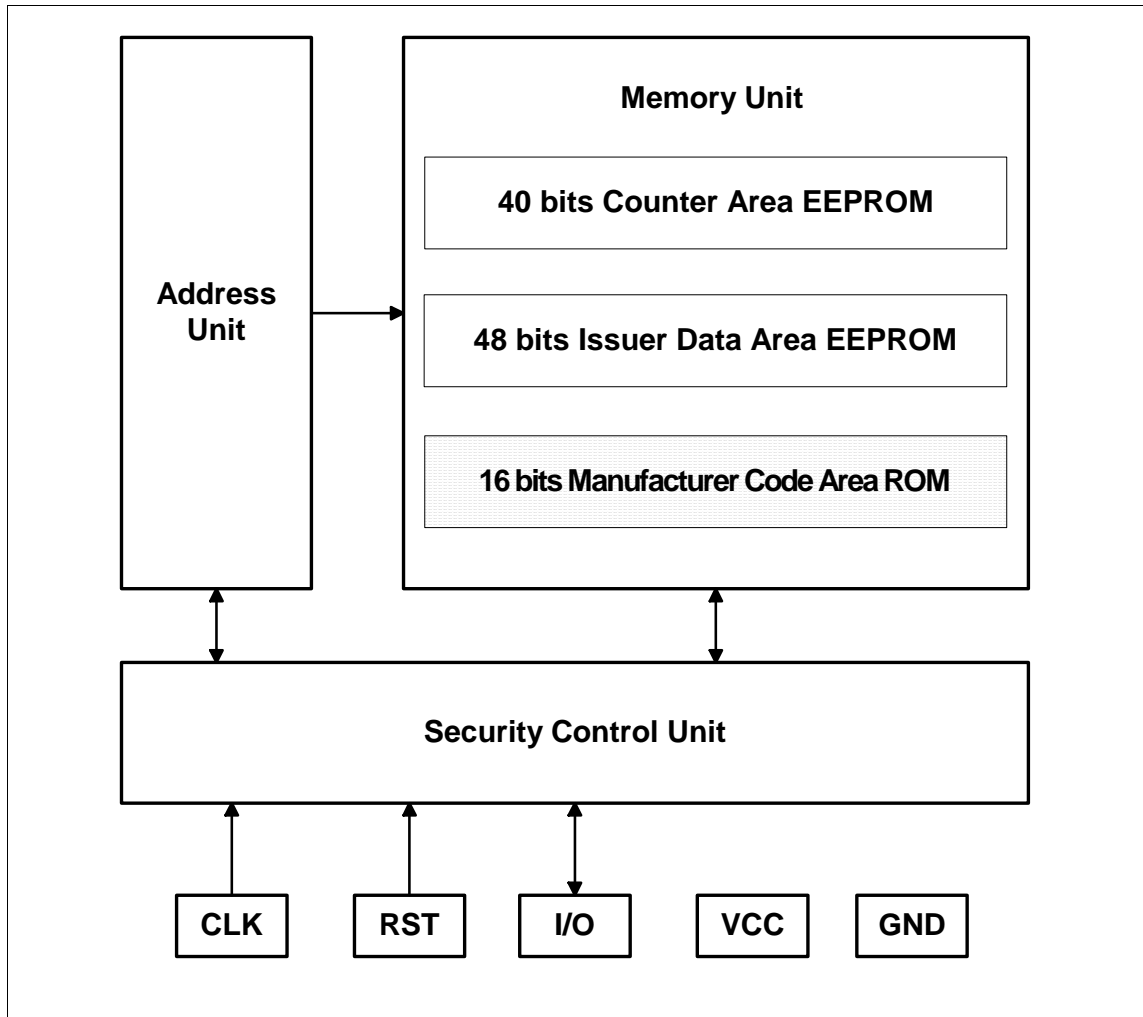
1.3. Pin Configurations



1.4. Pin Description

Card Contact	Symbol	Description
C1	VCC	Supply voltage
C2	RST	Control input (Reset Signal)
C3	CLK	Clock input
C5	GND	Ground
C6	N.C.	Not connected
C7	I/O	Bidirectional data line (open drain)

1.5. Block Diagram



2. Memory Organization

The memory is organized in 104×1 bit. Dependent on the status of the flag for personalization (address 64) the memory operates in two different modes.

2.1. Issuer Mode

The flag for personalization (address 64) is “1”. During delivery the chip is protected by a secret Transport Code with an Error counter. The Identification Area (address 0~63) and the Error counter (address 72~79) are readable, and only the Error counter is programmed. Only after correct verification of the Transport Code the whole memory is readable and programmed. The Counter Area (address 64~103) changes to a five stage counter.

2.2. User Mode

The flag for personalization (address 64) is “0”. The Identification Area (address 0~63) is protect against further programming.

3. Memory Map

Address	Issuer Mode							User Mode				
	TC not verified				TC verified			W	E	R	Definition	
	W	E	R	Definition	W	E	R					
96-103	N	N	1	TC Byte3	Y	In	Y	Y	In	Y	Counter Stage 1 (8 ⁰ unit)	
88-95	N	N	1	TC Byte2	Y	In	Y	Y	In	Y	Counter Stage 2 (8 ¹ unit)	
80-87	N	N	1	TC Byte1	Y	In	Y	Y	In	Y	Counter Stage 3 (8 ² unit)	
72-79 (77-79)	Y	N	Y	Error Counter	Y	In	Y	Y	In	Y	Counter Stage 1 (8 ³ unit)	
65-71 (69-71)	N	N	Y	(Reserved)	Y	N	Y	Y	N	Y	Counter Stage 5 (8 ⁴ unit)	
64	N	N	1	Personalization flag	Y	N	1	Y	N	0	Personalization flag	
16-63	N	N	Y	Personalization flag	Y	N	Y	N	N	Y	Personalization flag	
0-15	N	N	Y	Manufacturer code	N	N	Y	N	N	Y	Manufacturer code	

Access Conditions

W: Write ("1"→"0")	E: Erase ("0"→"1")	R: Read ("1" or "0")
Y: Yes N: No	N: No In: Indirectly	Y: Yes 1: read "1"

4. Count Unit

The Counter Area consists of a preloaded five stage counter as 5-digit octal counter. The highest counter stage 5 representing a value of 8^4 units; The lowest counter stage 1 representing a value of 8^0 unit.

Therefore a maximum number of units is

$$8 \cdot 8^4 + 8 \cdot 8^3 + 8 \cdot 8^2 + 8 \cdot 8^1 + 8 \cdot 8^0 = 37448$$

In practice the range is reduced to 33352 units due to the personalization bit (address 64).

Counting is done by writing bits from "1" to "0". If there are not enough bits in stage the erasing with carry has to be applied.

The erasing with carry consists of two consecutive write operations. The first pulse writes a carry bit in higher stage m to "0", the second pulse at same address erase all 8 bits of the lower stage m-1 to "1".

The counter stage 1 to 4 may completely be erased to "1". The highest counter stage 5 is not erasable, thus counter can be limited to certain number of units.

5. Transport Code Protection

The chip is protected with a 3bytes Transport Code (Issuer Mode). The Transport Code is programmed in counter stage 1 (address 96~103), 2 (address 88~95) and 3 (address 80~87) and the counter stage 4 (address 72~79) has the functionality of the Error Counter. It limits the Transport Code verification to 8 trials.

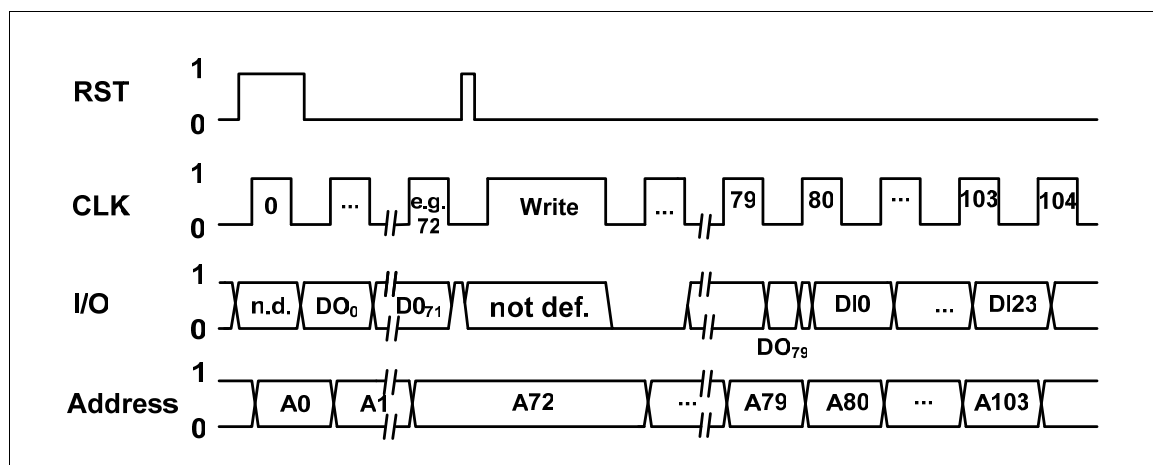
In the state the Identification Area (address 0~63) and the Error counter (address 72~79) are readable, and only the Error counter is programmed. Only after correct verification of the Transport Code the whole memory is readable and programmed.

The following procedure has to be applied to verify the Transport Code:

1. Address Reset.
2. Increment Error Counter by 1. Increment address counter to free Error Counter bit (=“1”) in the address from 72 to 79. Apply write operation on the addressed bit
3. Starting at address 80 the 24bit Transport Code has to be presented at I/O. Increment address counter from 80 to 103 and present data during CLK high. The internal comparison occurs during every CLK low. Add one clock pulse to finish the comparison.

The Transport Code mechanism is active until the personalization bit (address 64) is written (=“0”). The chip is irreversibly blocked for further use if all Error Counter bits are written without correct verification of the Transport Code.

Figure1. Entry of Transport Code



6. Electrical Characteristics

6.1. Absolute Maximum Ratings

Operating Temperature	-40°C ~ +85°C
Storage Temperature	-55°C ~ +125°C
Input voltage on Any Pin to Ground	-0.3V ~ +6.0V
Maximum Operating Voltage	6.0V

6.2. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current	$V_{CC} = 5V$		1.0	3.0	mA
V_{IH}	Input High Level (I/O, CLK, RST)		3.5		V_{CC}	V
V_{IL}	Input Low Level (I/O, CLK, RST)		0		0.8	V
I_{IH}	High Level Input Current (CLK)	$V_{IH} = 5V$, internal pull-down			100	μA
I_{IO}	Low Level Input Current (RST)	$V_{IH} = 0V$, internal pull-up		-	-100	μA
I_{OH}	High Level Output Current (I/O)	$V_{OH} = 5V$, open drain			10	μA
I_{OL}	Low Level Output Current (I/O)	$V_{OL} = 0.5V$, open drain	0.5			mA

6.3. AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{10}	RST High to CLK Setup time	5			μs
t_{11}	CLK Low to RST Hold time	5			μs
t_{12}	RST High time (address reset)	50			μs
t_{13}	RST Low to I/O Valid time			5	μs
t_{14}	RST Low to CLK Setup time (set address)	5			μs
t_{15}	CLK High time (set address)	10			μs
t_{16}	CLK Low time (set address)	10			μs
t_{17}	CLK Low to I/O Valid time			3.5	μs
t_R	CLK Rise time			1	μs
t_F	CLK Fall time			1	μs
t_1	CLK Low to RST Setup time	5			μs
t_2	RST Low to CLK Setup time (write address)	5			μs
t_3	RST High time (set write flag)	10			μs
t_4	CLK Low to CLK Setup time After Write	10			μs
t_W	CLK High time (write)	5			ms
t_5	CLK High to I/O Clear time			3.5	μs
t_6	I/O Setup to CLK Low time	3.5			μs
t_7	CLK High to I/O Hold time	3.5			μs

7. Timing Diagrams

Figure 2. Answer to Reset, Address setting and Read Operation

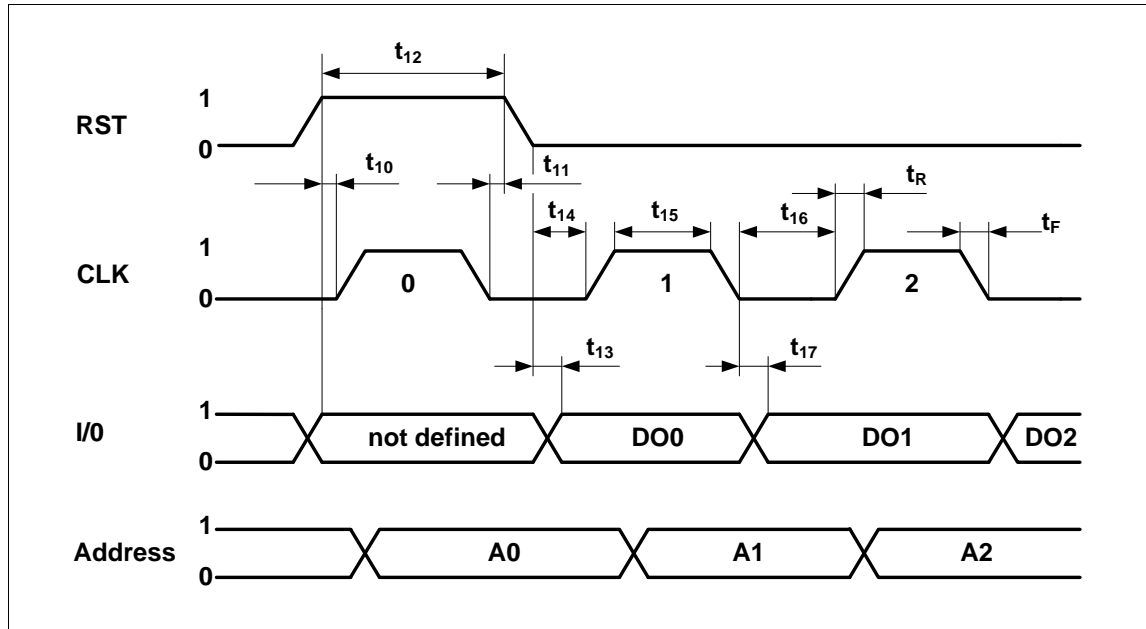


Figure 3. Write Operation

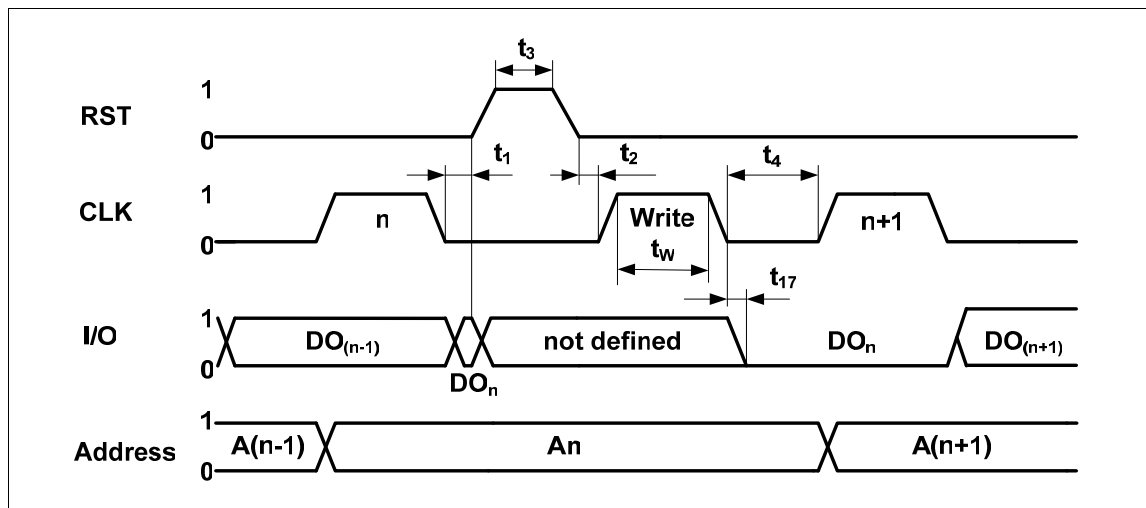


Figure 4. Erase 8 Bits with Carry Operation

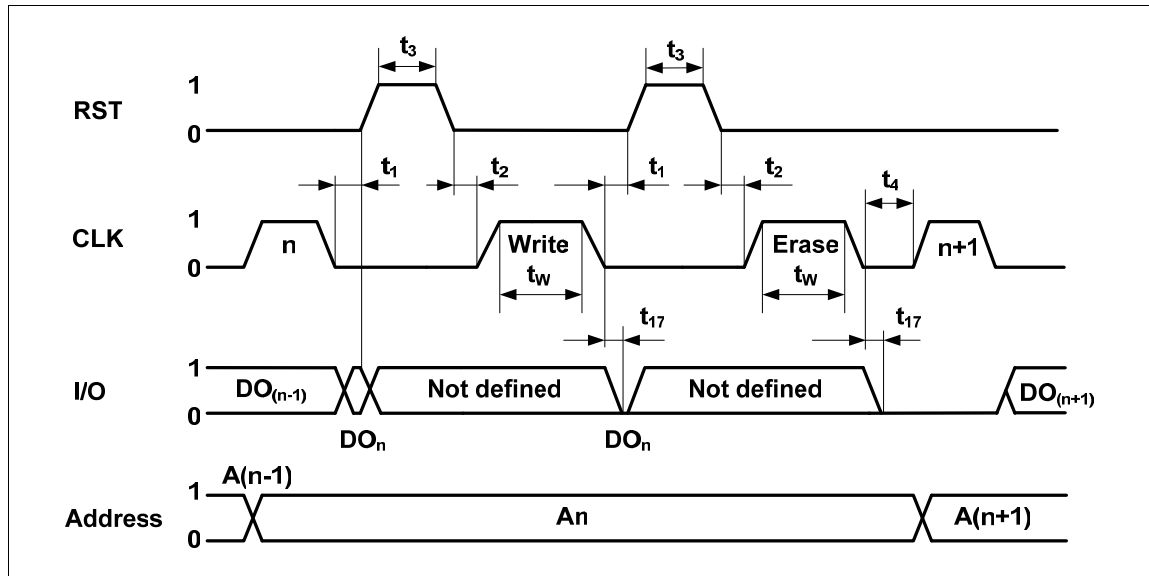
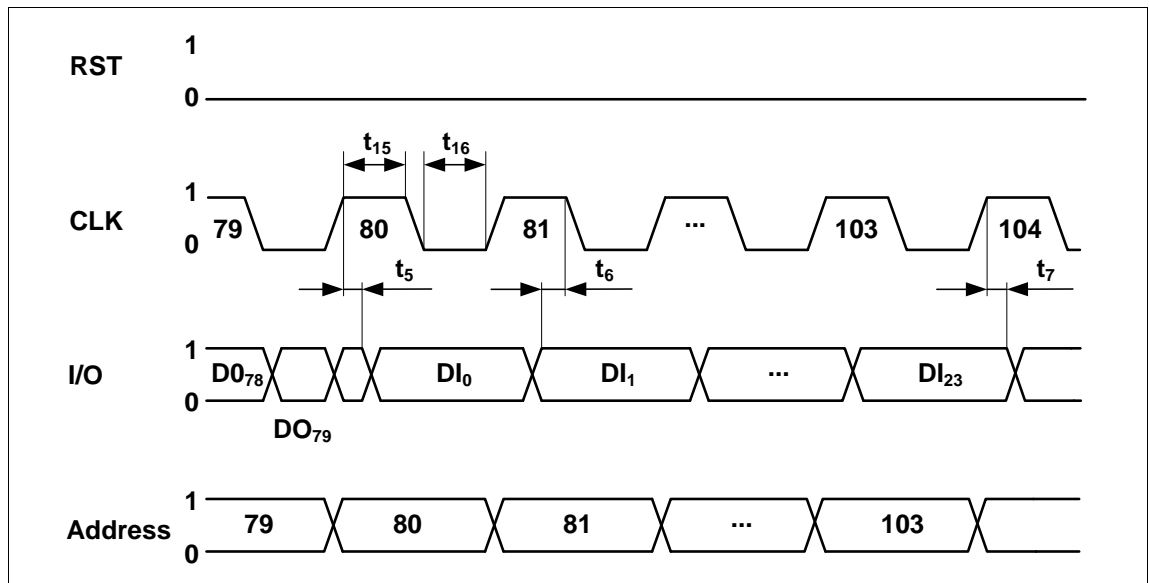


Figure 5. Entry of Transport Code





8. Ordering Information

Ordering Code	Package	Operating Range
STF1001-M3	Module Package (6Pin)	Industrial Temperature (-40°C ~ +85°C)



Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Oct. 2007	14		Initial Release.
1.1	May. 2008	14	Sales and service	Updated the address of HK office.

Sales and Service

Shanghai Fudan Microelectronics Co., Ltd.

Address: Bldg No. 4, 127 Guotai Rd,
Shanghai City China.
Postcode: 200433
Tel: (86-21) 6565 5050
Fax: (86-21) 6565 9115

Shanghai Fudan Microelectronics (HK) Co., Ltd.

Address: Unit 506, 5/F., East Ocean Centre, 98 Granville Road,
Tsimshatsui East, Kowloon, Hong Kong
Tel: (852) 2116 3288 2116 3338
Fax: (852) 2116 0882

Beijing Office

Address: Room.1208, Bldg C,
Zhongguancun Science and Technology Development Edifice, 34 zhongguancun Street (South),
Hai Dian District, Beijing City, China.
Postcode: 100081
Tel: (86-10) 6212 0682 6213 9558
Fax: (86-10) 6212 0681

Shenzhen Office

Address: Room.1301, Century Bldg, Shengtingyuan Hotel, Huaqiang Rd (North),
Shenzhen City, China.
Postcode: 518028
Tel: (86-755) 8335 3211 8335 6511
Fax: (86-755) 8335 9011

Web Site: <http://www.fmsk.com/>