NTD6415N

Product Preview

Power MOSFET

100 V, 20 A, Single N−Channel, DPAK/IPAK

Features

- Low $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- These are Pb−Free Devices

Applications

- CCFL Backlight
- DC Motor Control
- Class D Amplifier
- Power Supplies Secondary Side Synchronous Rectification

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	100	V
Gate−to−Source Voltage − Continuous			V_{GS}	±20	V
Gate−to−Source Voltage − Nonrepetitive (T_P < 10 μs)			V_{GS}	±30	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	20	A
		T_C = 100°C		14.5	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	P_D	83	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	42	A
Operating and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	20	A
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 50 V_{dc}, V_{GS} = 10 V, $I_{L(pk)}$ = 20 A, L = 0.1 mH, R_G = 25 Ω, V_{DS} = 40 V_{dc})			E_{AS}	TBD	mJ
Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 Seconds			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Case (Drain) Steady State (Note 1)	$R_{\theta JC}$	1.8	°C/W
	$R_{\theta JA}$	68	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

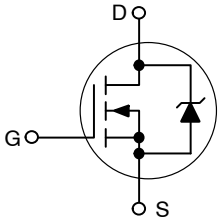
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).

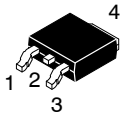
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ON Semiconductor®

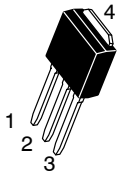
http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX (Note 1)
100 V	69 mΩ @ 10 V	20 A



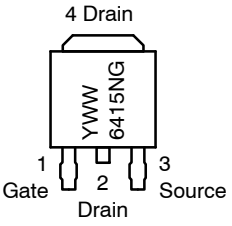


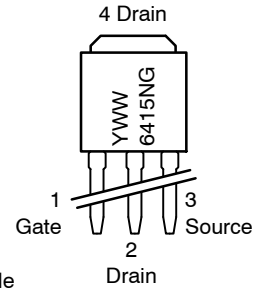
DPAK
CASE 369C
STYLE 2



IPAK
CASE 369D
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS





6415N	= Device Code
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		100			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				TBD		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 100 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				TBD		mV/°C
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A			60	69	mΩ
		V_{GS} = 10 V, I_D = 20 A			TBD	TBD	
Forward Transconductance	gFS	V_{DS} = 15 V, I_D = 15 A			TBD		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			1395	1495	pF
Output Capacitance	C_{OSS}				172		
Reverse Transfer Capacitance	C_{RSS}				TBD		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 80 V, I_D = 20 A			33	133	nC
Threshold Gate Charge	$Q_{G(TH)}$				TBD		
Gate−to−Source Charge	Q_{GS}				TBD		
Gate−to−Drain Charge	Q_{GD}				TBD		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 80 V, I_D = 20 A, R_G = 6.1 Ω			TBD		ns
Rise Time	t_r				TBD		
Turn−Off Delay Time	$t_{d(off)}$				TBD		
Fall Time	t_f				TBD		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		TBD	1.2	V
			T_J = 100°C		TBD		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 20 A			TBD		ns
Charge Time	T_a				TBD		
Discharge Time	T_b				TBD		
Reverse Recovery Charge	Q_{RR}				TBD		nC

2. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

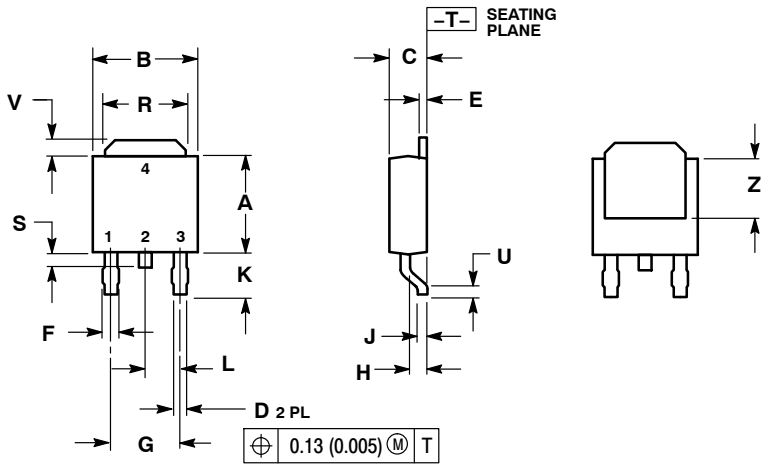
ORDERING INFORMATION

Device	Package	Shipping†
NTD6415NT4G	DPAK (Pb−Free)	2500 / Tape & Reel
NTD6415N−1G	IPAK (Pb−Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK
CASE 369C−01
ISSUE O

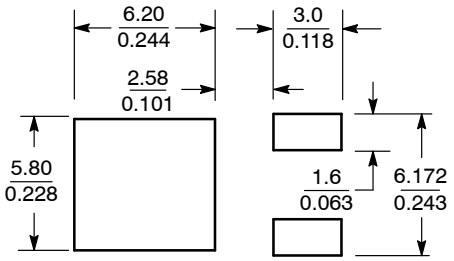


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



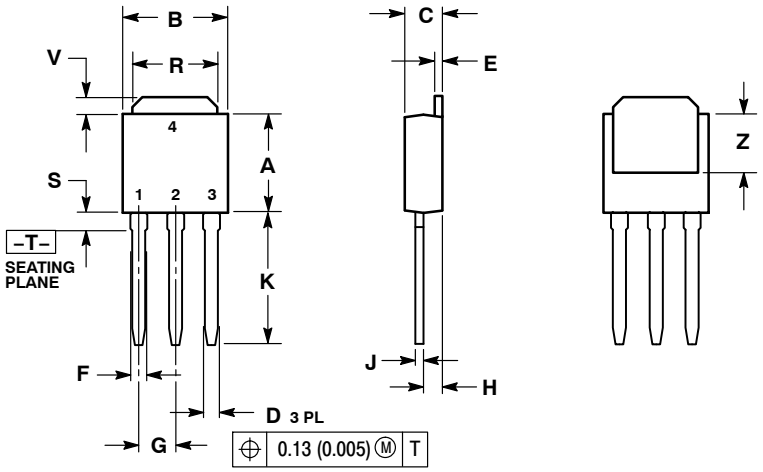
SCALE 3:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD6415N

PACKAGE DIMENSIONS

DPAK
CASE 369D−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NTD6415N/D