Datasheet

FS356

One Cell Lithium-ion/Polymer Battery Protection IC

Fortune Semiconductor Corporation
富晶電子股份有限公司
28F., No.27, Sec. 2, Zhongzheng E. Rd.,
Danshui Town, Taipei County 251, Taiwan
Tel.：886-2-28094742
Fax：886-2-28094874
www.ic-fortune.com

This manual contains new product information. **Fortune Semiconductor Corporation** reserves the rights to modify the product specification without further notice. No liability is assumed by **Fortune Semiconductor Corporation** as a result of the use of this product. No rights under any patent accompany the sale of the product.

1. General Description

FS356 is a series of lithium-ion and lithium polymer rechargeable battery protection ICs with high accurate voltage detection and delay circuits.
These ICs are suitable for protection of single cell lithium-ion or lithium polymer battery packs from over charge, over discharge, and over current.

2. Features

- Low supply currentOperation:
  - 3.0uA typ. @VDD=3.9V
- Power-down mode:
  - 0.1uA max. @VDD=2.0V
- Overcharge detection voltage (Vdet1):
  - 4.0V~4.4V, Accuracy of ±25mV (Ta=25°C)
- Overdischarge detection voltage (Vdet2):
  - 2.0V~3.0V, Accuracy of ±2.5%
- Excess discharge current detection voltage (Vdet3):
  - 0.05V~0.20V, Accuracy of ±30mV
- Excess charge current detection voltage (Vdet4):
  - Fixed at -0.1V, Accuracy of ±30mV
- Short circuit protection voltage (Vshort):
  - VDD – 1.1V, Accuracy of ±0.3V
- Delay times are generated by an internal circuit. (External capacitors are unnecessary.)
- DS pin for reduce preset output delay time
- 0V-Battery charging function
- With latch function after overcharge detection

3. Applications

- Protection IC for One-Cell Lithium-Ion / Lithium-Polymer Battery Pack

4. Ordering Information

FS356 A-XX

Serial code

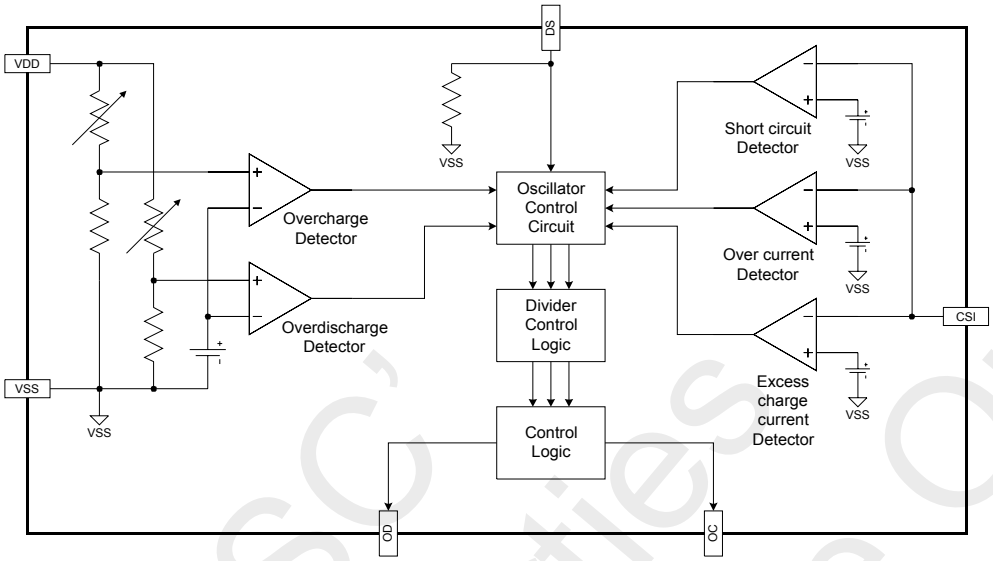
A: Package
- P(Pb-free SOT-26)
- SA(S:Pb-free DFN，Size 1.6*1.6 mm^2)

5. Product Name List

Model	Overcharge detection voltage [Vdet1] (V)	Overdischarge detection voltage [Vdet2] (V)	Overcurrent detection voltage [Vdet3] (mV)
FS356A	4.275	2.300	100
FS356B	4.275	2.600	50

Overcharge, overdischarge and overcurrent detection voltages can be changed at the customer's request.

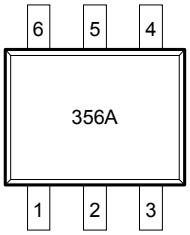
6. Block Diagram

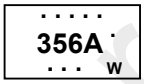


7. Pin Configuration and Package Marking Information

FS356A-P:

Pin No.	Symbol	Description
1	OD	FET gate connection pin for discharge control
2	CSI	Input pin for current sense, charger detect
3	OC	FET gate connection pin for charge control
4	DS	Test pin for reduce preset output delay time
5	VDD	Positive power input pin
6	VSS	Negative power input pin

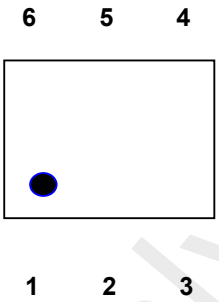


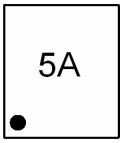


Top Point：Lot No.
Bottom Point：Year
w : week, A~Z & A ~ Z
A dot after marking : Pb Free

FS356B-SA:

Pin No.	Symbol	Description
1	NC	
2	OC	FET gate connection pin for charge control
3	OD	FET gate connection pin for discharge control
4	VSS	Negative power input pin
5	VDD	Positive power input pin
6	CSI	Input pin for current sense, charger detect

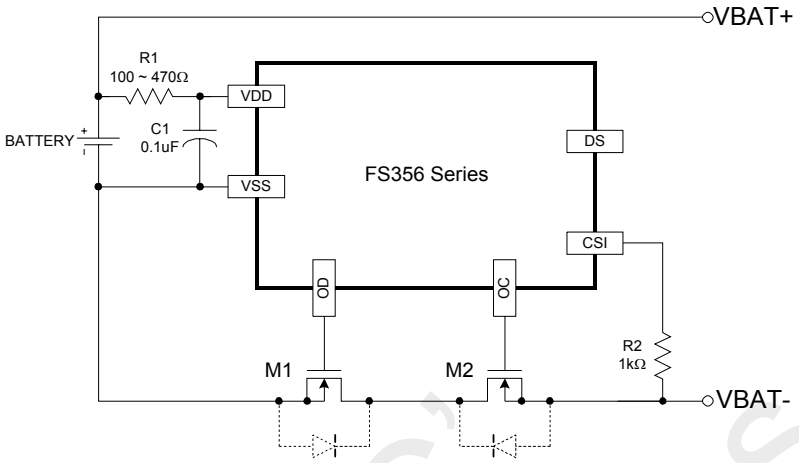




5: 356
A: Detection Voltage Type

Note: IC bottom center pad can connected VSS or Floating.

8. Typical Application Circuit



9. Absolute Maximum Ratings

(VSS=0V, Ta=25℃ unless otherwise specified)

Item	Symbol	Rating	Unit
Input voltage between VDD and VSS *	VDD	VSS-0.3 to VSS+12	V
OC output pin voltage	VOC	VDD-22 to VDD+0.3	V
OD output pin voltage	VOD	VSS-0.3 to VDD+0.3	V
CSI input pin voltage	VCSI	VDD-22 to VDD+0.3	V
DS input pin voltage	VDS	VSS-0.3 to VDD+0.3	V
Operating Temperature Range	TOP	-40 to +85	℃
Storage Temperature Range	TST	-40 to +125	℃

Note: This IC contains a circuit that protects it from static discharge, but take special care that no excessive static electricity or voltage which exceeds the limit of the protection circuit is applied to the IC.

* Pulse (μsec) noise exceeding the above input voltage (VSS+12V) may cause damage to the IC.

10. Electrical Characteristics

(VSS=0V, DS=Floating, Ta=25℃ unless otherwise specified)

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
CURRENT CONSUMPTION						
Supply Current	VDD=3.9V	IDD		3.0	6.0	uA
Power-Down Current	VDD=2.0V	IPD			0.1	uA
OPERATING VOLTAGE						
Operating input voltage	VDD-VSS	VDS1	1.8		8.0	V
DETECTION VOLTAGE						
Overcharge detection voltage		Vdet1	Vdet1 -0.025	Vdet1	Vdet1 +0.025	V
Overdischarge detection voltage		Vdet2	Vdet2 x 0.975	Vdet2	Vdet2 x 1.025	V
Excess discharge current detection voltage		Vdet3	Vdet3 -0.030	Vdet3	Vdet3 +0.030	V
Excess charge current detection voltage		Vdet4	-0.13	-0.10	-0.07	V
Short circuit protection voltage	VDD=3.0V	Vshort	VDD-1.4	VDD-1.1	VDD-0.8	V
Reset resistance for Over current protection	VDD=3.6V	Rshort	15	30	45	KΩ
DELAY TIME						
Overcharge detection delay time	VDD=3.6V to 4.4V	tVdet1		1.3	1.9	s
Overcharge release delay time	VDD=4V, V-=0V to 1V	tVrel1		17	24	ms
Overdischarge detection delay time	VDD=3.6V to 2.2V	tVdet2		30	42	ms
Overdischarge release delay time	VDD=(Vdet2-0.2V) to	tVrel2		1.5	2.2	ms

	(Vdet2+0.2V), V-=0V					
Excess discharge current detection delay time	VDD=3V, V-=0V to 1V	tVdet3		8	12	ms
Excess discharge current release delay time	VDD=3V, V-=3V to 0V	tVrel3		2.2	3.2	ms
Excess charge current detection delay time	VDD=3V, V-= 0V to -1V	tVdet4		15	22	ms
Excess charge current release delay time	VDD=3V, V-= -1V to 0V	tVrel4		2.4	3.4	ms
Short circuit detection delay time	VDD=3.0V	Tshort		800	1100	us
OTHER						
OC pin output “H” voltage	VDD=3.9V, Ioh=-50uA	Voh1	3.4	3.7		V
OC pin output “L” voltage	VDD=4.5V, CSI=0V	Vol1		0.1	0.5	V
OD pin output “H” voltage	VDD=3.9V, Ioh=-50uA	Voh2	3.4	3.7		V
OD pin output “L” voltage	VDD=2.0V, Iol=50uA	Vol2		0.1	0.5	V
Minimum operating Voltage for 0V charging. *Note1	Voltage defined as VDD-CSI, VDD-VSS=0V	Vst			1.5	V

Note1: Specified for 0V battery charging function version

11. Description of Operation

Normal Condition

The FS356 monitors the voltage of the battery connected between VDD and VSS pin and the voltage difference between CSI and VSS pin to control charging and discharging. When Vdet2<VDD<Vdet1 and Vdet4<VCSI<Vdet3, the IC turns the charging (M2) and discharging (M1) control FETs on. The charging and discharging processes can be operated normally. This condition is called the normal condition.

Note: When a battery is connected to the IC for the first time, the IC may not enter the normal condition (not dischargeable condition). If this occurs, set the CSI pin voltage equal to the VSS voltage (short the CSI and VSS pins or connect a charger) to enter the normal condition.

Overcharge Condition

When the battery voltage becomes higher than the overcharge detection voltage (Vdet1) during charging under the normal condition and the detection continues for the overcharge detection delay time (tVdet1) or longer, the FS356 turns M2 off to stop charging. This condition is called the overcharge condition.

Release of Overcharge Condition

There are two ways to return to normal condition from overcharge condition.
When the battery is self discharging, if VDD<Vdet1 and Vdet3>VCSI>Vdet4 occurs, M2 is to be turned on and back to normal condition.
Remove the charger and connected to a load, so that the discharging current flows through the parasitic diode in M2. At this moment VCSI increases momentarily Vf voltage of the parasitic diode from the VSS level. If VCSI>Vdet3 and VDD<Vdet1 occurs, M2 is to be turned on and back to normal condition.

Note 1: After entering the overcharge condition, if the charger is not removed and Vdet3>VCSI>Vdet4, then M2 will be turned on when the voltage of the battery is lower than Vdet1 (because the self-discharge of the battery). The system can enter the charge status again as 1).

Note 2: After entering the overcharge condition, if the charger is not removed and VCSI<Vdet4, then M2 will be kept off even though the voltage of the battery is lower than Vdet1 (because the self-discharge of the battery), and the system will not enter the charge status.

Overdischarge Condition

When the battery voltage falls below the overdischarge detection voltage (Vdet2) during discharging under the normal condition and the detection continues for the overdischarge detection delay time (tVdet2) or longer, the FS356 turns M1 off to stop discharging. This condition is called the overdischarge condition. In the meanwhile, CSI is pulled to VDD by way of internal resistance, RCSID. If VCSI>Vshort, the protection IC enters into Power-down mode. (Its current consumption is lower than 0.1uA).

Release of Power-down mode

After entering Power-down mode, if the system is connected to a charger, and the charging current flows through the parasitic diode in M1. If VCSI<Vshort occurs, then it will release Power-down mode. If keeping charging, there are two ways to enter the normal condition.

1) If VCSI<Vdet4 (Charger detection), then when VDD>Vdet2, M1 will be turned on, and the system enters the normal condition.

2) If Vdet4<VCSI<Vshort, then it must be VDD>Vdet2 for M1 to be turned on, and make the system enter the normal condition.

Charger Detection

In Power-down mode, when connecting to a charger, if VCSI<Vdet4, then M1 will be turned on when VDD>Vdet2, and the system will enter the normal condition as described in 1) of previous section, because the charger detection function is enabled. This action is called charger detection.

Excess Charge Current Condition

When a charger is connected to the battery in normal condition, if VDD<Vdet1 and VCSI<Vdet4 occurs for a delay time longer than tVdet4, then M2 will be turned off and charging stop. This condition is called the excess charge current condition
Excess charge current condition is released when the voltage of CSI pin becomes higher than excess charge current detection voltage(Vdet4), or the charger is removed.

Over Current / Short Circuit Condition

When the discharging current is too large during discharging under normal condition and the voltage detected from CSI is larger than Vdet3 (or Vshort) for over a certain delay time tVdet3 (or Tshort), it means the over current/short circuit condition occurred. M1 is turned off. CSI is pulled to VSS by way of an internal resistance, RCSIS. This condition is called the over current (short circuit) condition.

Release of Over Current / Short Circuit Condition

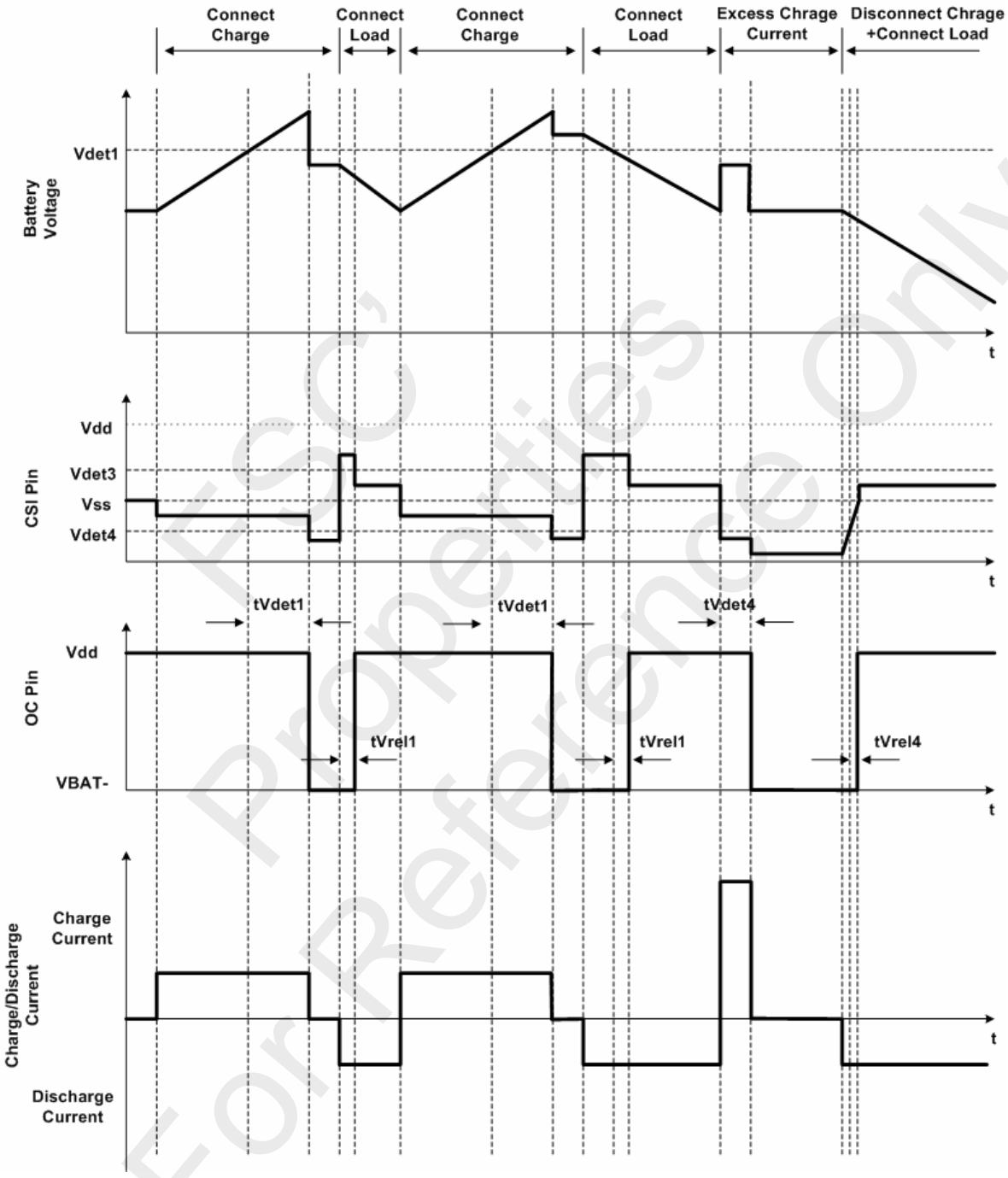
While the protection IC remains in Over current/Short circuit condition and load is removed or the impedance between VBAT+ and VBAT- is larger than 30KΩ and VCSI<Vdet3, M1 is to be turned on and back to normal condition.

DS Pin

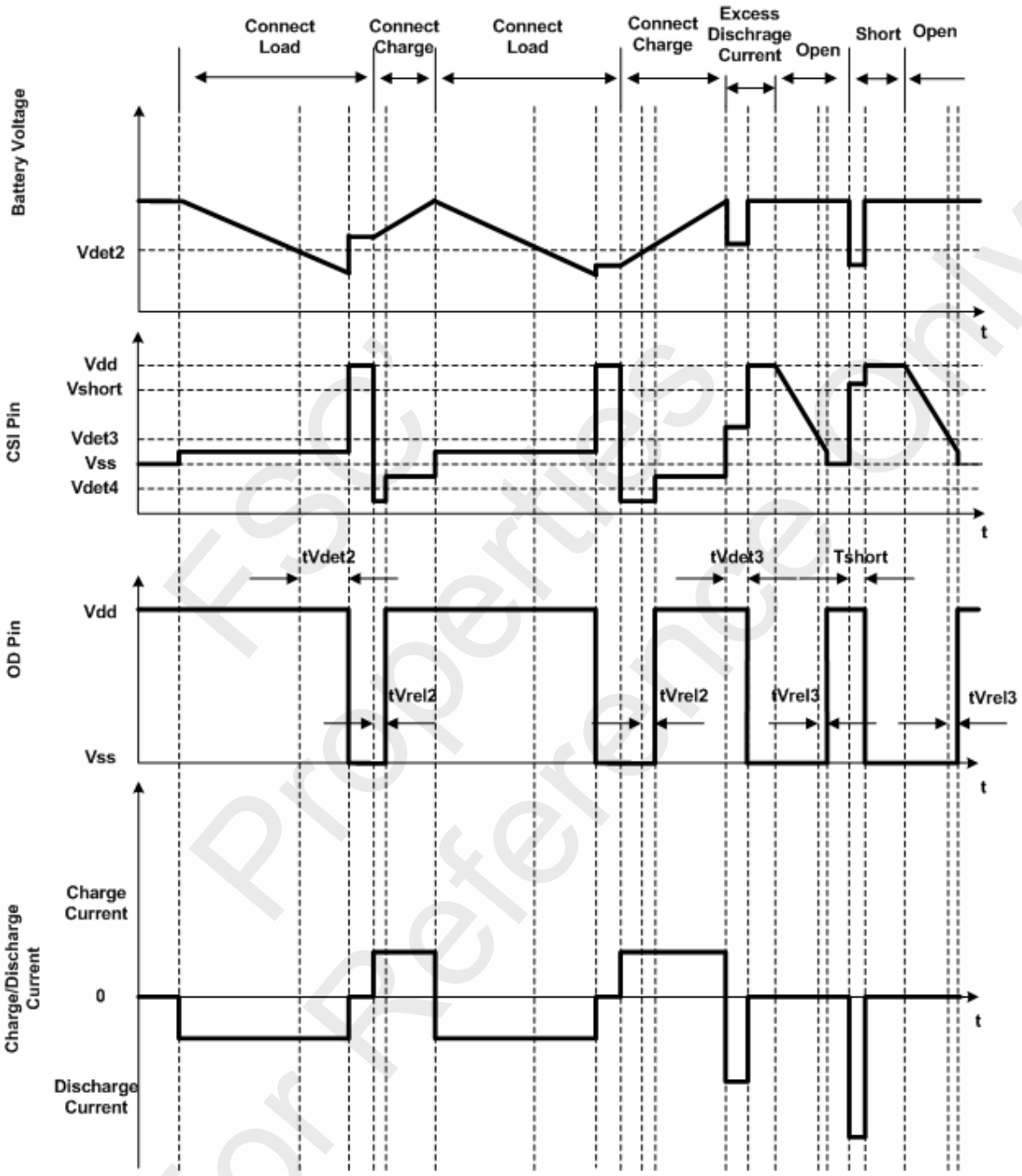
By forcing VDD voltage to DS pin, the delay time of overcharge and overdischarge can be reduced to within 50ms, therefore, testing time of protector circuit board can be reduced.
1.6MΩ pull down resistor is connected between DS pin and VSS internally.
DS pin should be open, or connected to VSS in the actual application.

12. Timing Diagram

Overcharge , Excess charge Current Operation



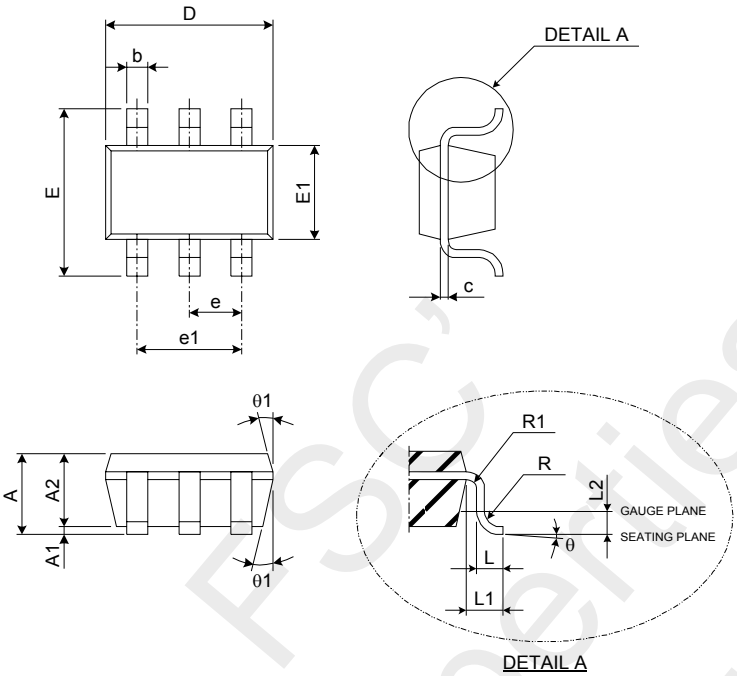
Overdischarge , Excess discharge current , Short circuit operation



13. Package Outline

13.1. SOT-23-6

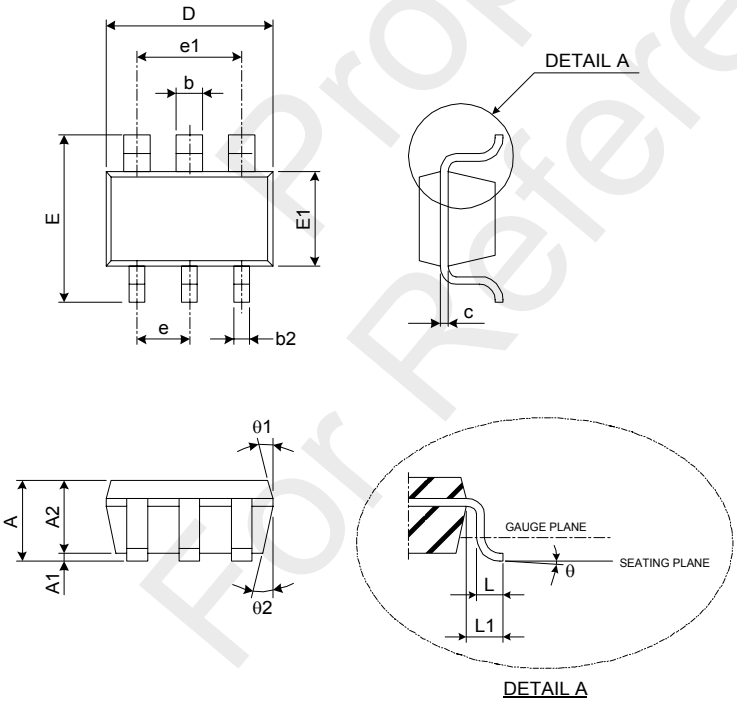
Dimensions (Package A)



Unit : mm

SYMBOL	MIN.	TYP.	MAX.
A	-	-	1.45
A1	-	-	0.15
A2	0.90	1.15	1.30
b	0.30	-	0.50
c	0.08	-	0.22
D		2.90 BSC.	
E		2.80 BSC.	
E1		1.60 BSC.	
e		0.95 BSC.	
e1		1.90 BSC.	
L	0.30	0.45	0.60
L1		0.60 REF.	
L2		0.25 BSC.	
R	0.10	-	-
R1	0.10	-	0.25
θ	0°	4°	8°
θ1	5°	10°	15°

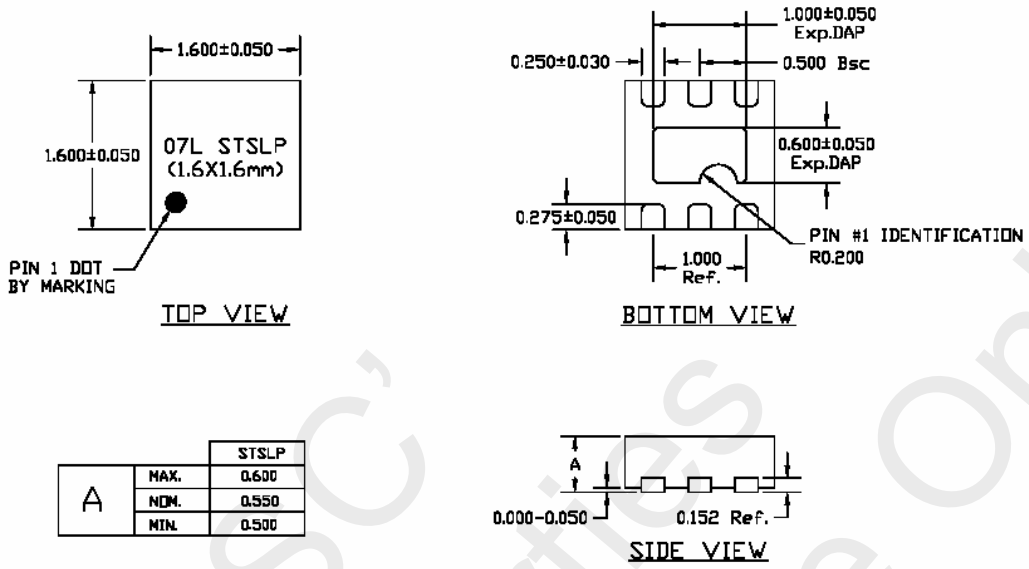
Dimensions (Package B)



Unit : mm

SYMBOL	MIN.	TYP.	MAX.
A	1.05	-	1.35
A1	0.05	-	0.15
A2	1.00	1.10	1.20
b	0.40	-	0.55
b2	0.25	-	0.40
c	0.08	-	0.20
D	2.70	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
L	0.35	0.45	0.55
L1		0.60 REF.	
e		0.95 BSC.	
e1		1.90 BSC.	
θ	0°	5°	10°
θ1	3°	5°	7°
θ2	6°	8°	10°

13.2. DFN (Package Size:1.6*1.6mm^2)



14. Revision History

Version	Date	Page	Description
0.1	2006/07/05	-	New release
0.2	2006/11/17	1,2,4,6	1. Revise new format 2. Add Package Marking Information 3. Revise delay time spec
0.3	2007/01/08	All	1. Revise symbol name 2. Revise Timing Diagram 3. Add Revision History
1.0	2007/02/26	-	Transfer 0.3 to 1.0 Version.
1.1	2007/04/02	3,6,8	1. Revise Vdet3 Spec Range 2. Revise Rshort 3. Delete Vnochg Specification and Note2
1.2	2007/04/12	3,5,12,13	1. Revise Ordering information 2. Revise Product Name List 3. Add DFN Pin Configuration and Package Marking Information 4. Add DFN Package outline