Datasheet

FS7755

Energy Metering IC with Impulse Output

Fortune
SEMICONDUCTOR CORPORATION

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1. General Description

The FS7755 is a high accuracy electrical energy measurement IC. The part specifications surpass the accuracy requirements as quoted in the IEC1036 standard.

The only analog circuitry used in the FS7755 is in the ADCs and reference circuit. All other signal processing (e.g., DSP) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

The FS7755 supplies average real power information on the low-frequency outputs F1 and F2. These logic outputs may be used to directly drive an electromechanical counter or interface to an MCU. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes or for interfacing to an MCU.

The FS7755 includes a power supply monitoring circuit on the AV_{DD} supply pin. The FS7755 will remain in a reset condition until the supply voltage on AV_{DD} reaches 4V. If the supply falls below 4V, the FS7755 will also be reset and no pulses will be issued on F1, F2, and CF.

An internal no load threshold ensures that the FS7755 does not exhibit any creep when there is no load.

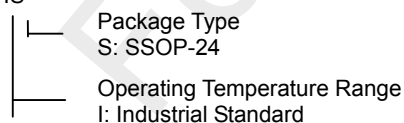The FS7755 is available in a 24-lead SSOP package.

2. Features

● High Accuracy, Surpasses 50Hz/60Hz IEC 687/1036

● Less than 0.1% Error over a Dynamic Range of 500 to 1

● Synchronous outputs with CF, F1 and F2

● The FS7755 Supplies Average Real Power on the Impulse Outputs F1 and F2

● The High-Frequency Output CF Is Intended for Calibration and Supplies Instantaneous Real Power

● The Logic Output REVP Can Be Used to Indicate a Potential Miswiring or Negative Power

● Direct Drive for Electromechanical Counters and Two Phase Stepper Motors (F1 and F2)

● A PGA (Programmable Gain Amplifier) in the Current Channel Allows the Use of Small Values of Shunt and Burden Resistance

● Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time

● On-Chip Power Supply Monitoring

● On-Chip Creep Protection (No Load Threshold)

● On-Chip Reference 2.5V ± 8% (30ppm/℃ Typical) with External Overdrive Capability

● Single 5V Supply, Low Power (15mW Typical)

● Low Cost CMOS Process

3. Applications

● Single Phase Electronic Energy Meter

4. Ordering Information

FS7755-IS

Package Type
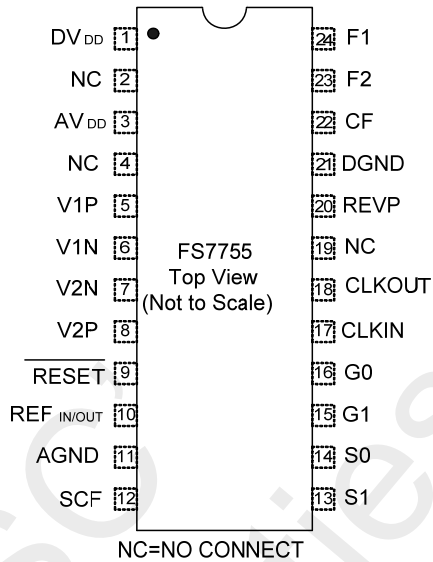S: SSOP-24

Operating Temperature Range
I: Industrial Standard

5. Pin Configuration

```
              DV DD  1  ●        24  F1
                NC   2           23  F2
              AV DD  3           22  CF
                NC   4           21  DGND
               V1P   5           20  REVP
               V1N   6    FS7755 19  NC
               V2N   7   Top View 18 CLKOUT
               V2P   8  (Not to Scale) 17 CLKIN
             RESET   9           16  G0
          REF IN/OUT 10          15  G1
              AGND  11           14  S0
               SCF  12           13  S1
```

NC=NO CONNECT

Fig1 Pin Configuration

6. Pin Description

Pin	Name	Function
1	DV$_{DD}$	Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the FS7755. The supply voltage should be maintained at 5V ± 5% for specified operation. This pin should be decoupled with a 10µF capacitor in parallel with a ceramic 100nF capacitor.
2, 4, 19	NC	No Connect
3	AV$_{DD}$	Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the FS7755. The supply should be maintained at 5V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. This pin should be decoupled to AGND with a 10µF capacitor in parallel with a ceramic 100nF capacitor.
5, 6	V1P, V1N	Analog Inputs for Channel 1 (Current Channel). These inputs are fully differential voltage inputs with a maximum differential signal level of ±470mV for specified operation. Channel 1 also has a PGA, and the gain selections are outlined in Table I. The maximum signal level at these pins is ±1V with respect to AGND. Both inputs have internal ESD protection circuitry. An overvoltage of ±6V can be sustained on these inputs without risk of permanent damage.
7, 8	V2P, V2N	Negative and Positive Inputs for Channel 2 (Voltage Channel). These inputs provide a fully differential input pair. The maximum differential input voltage is ±660mV for specified operation. The maximum signal level at these pins is ±1V with respect to AGND. Both inputs have internal ESD protection circuitry, and an over-voltage of ±6V can also be sustained on these inputs without risk of permanent damage.

| 9	$\overline{\text{RESET}}$	Reset Pin for the FS7755. A logic low on this pin will hold the ADCs and digital circuitry in a reset condition. Bringing this pin logic low will clear the FS7755 internal registers.
10	REF$_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5V ± 8% and a typical temperature coefficient of 30ppm/℃. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 10µF ceramic capacitor and 100nF ceramic capacitor.
11	AGND	This provides the ground reference for the analog circuitry in the FS7755, i.e., ADCs and reference. This pin should be tied to the analog ground plane of the PCB. The analog ground plane is the ground reference for all analog circuitry, e.g., anti-aliasing filters and current and voltage transducers. For good noise suppression, the analog ground plane should only connect to the digital ground plane at one point. A star ground configuration will help to keep noisy digital currents away from the analog circuits.
12	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table IV shows how the calibration frequencies are selected.
13, 14	S1, S0	These logic inputs are used to select one of four possible frequencies for the Power to Impulse Converter. This offers the designer greater flexibility when designing the energy meter. See Selecting a Frequency for an Energy Meter Application section.
15, 16	G1, G0	These logic inputs are used to select one of four possible gains for Channel 1, i.e., V1. The possible gains are 1, 8, 16 and 32. See Analog Input section.
17	CLKIN	An external clock can be provided at this logic input. Alternatively, a parallel resonant crystal can be connected across CLKIN and CLKOUT to provide a clock source for the FS7755. The clock frequency for specified operation is 3.579545MHz. Crystal load capacitance of between 22pF and 33pF (ceramic) should be used with the gate
18	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the FS7755. The CLKOUT Pin can drive one CMOS load when an external clock is supplied at CLKIN or by the gate oscillator circuit.
20	REVP	This logic output will go logic high when negative power is detected, i.e., when the phase angle between the voltage and current signals is greater than 900. This output is not latched and will be reset when positive power is once again detected. The output will go high or low at the same time as a impulse is issued on CF.
21	DGND	This provides the ground reference for the digital circuitry in the FS7755, i.e., DSP. This pin should be tied to the digital ground plane of the PCB. The digital ground plane is the ground reference for all digital circuitry, e.g., counters (mechanical and digital), MCUs, and indicator LEDs or LCDs. For good noise suppression, the analog ground plane
22	CF	Calibration Frequency Logic Output. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes. Also see SCF Pin description.
23, 24	F2, F1	Low Frequency Logic Outputs. F1 and F2 supply average real power information. The logic outputs can be used to directly drive electromechanical counters and two-phase stepper motors. See Transfer Function section.

7. Functional Block Diagram
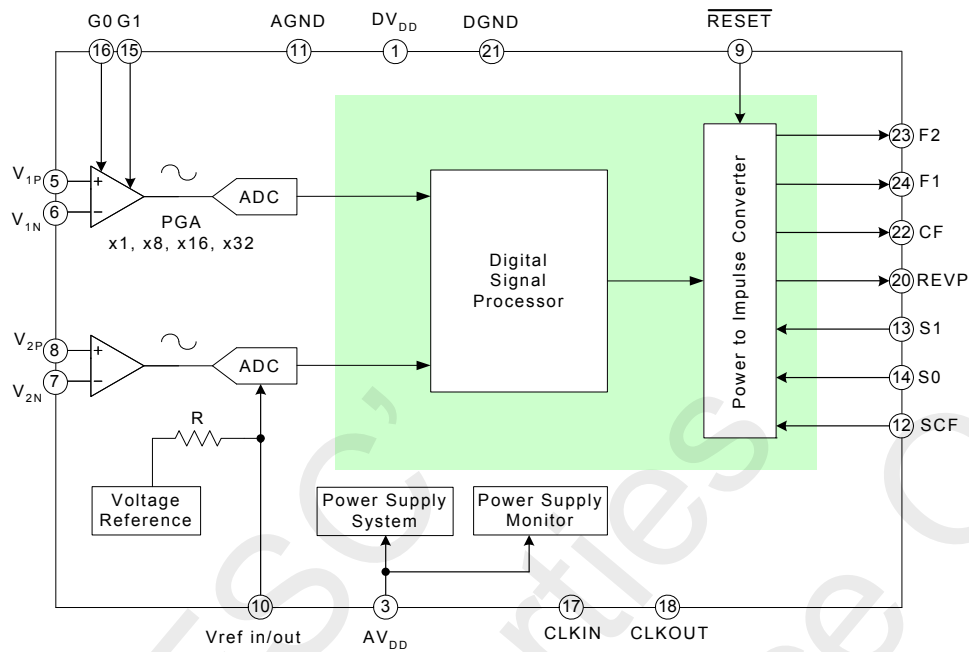
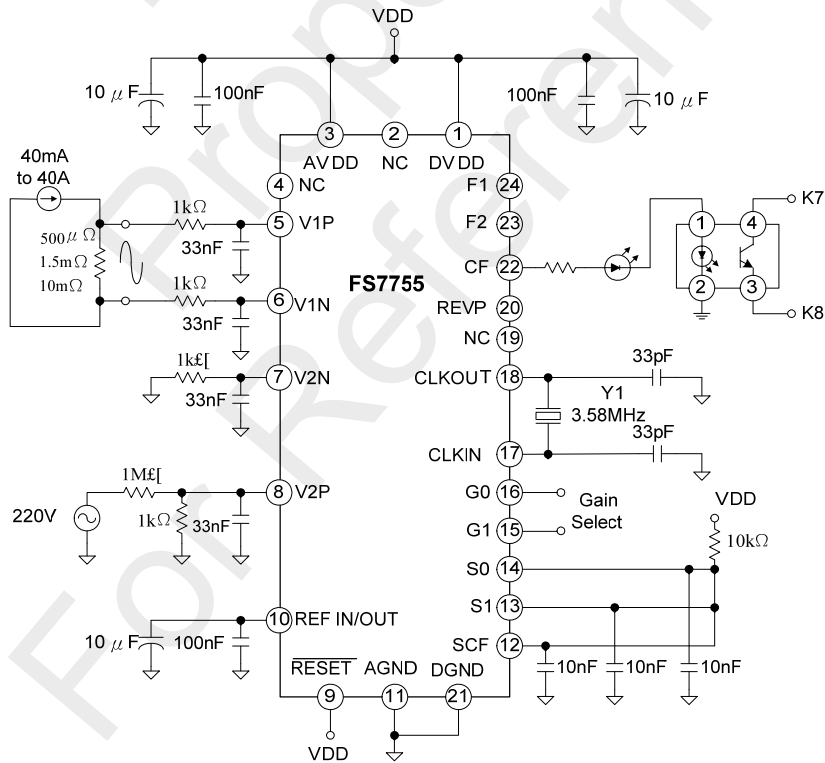Fig2 Functional Block Diagram

8. Typical Application Circuit

Fig3 Application Circuit

9. Absolute Maximum Ratings*

(T_A = 25℃ unless otherwise noted.)

AV_{DD} to AGND……………………………………………………………….…………………………… −0.3V to +7V
DV_{DD} to DGND……………………………………………………………………………………………… ..−0.3V to +7V
DV_{DD} to AV_{DD}.…………………………………………………………………….………… .−0.3V to +0.3V
Analog Input Voltage to AGND, V1P, V1N, V2P, and V2N.………………………………………… −6V to +6V
Reference Input Voltage to AGND……………………………………………….………−0.3V to AV_{DD} + 0.3V
Digital Input Voltage to DGND…………………………………………………….………..− −0.3V to DV_{DD} + 0.3V
Digital Output Voltage to DGND…………………………………………….…………...− −0.3V to DV_{DD} + 0.3V
Operating Temperature Range
   Industrial……………………………………………………………………………..…………-40℃ to +85℃
Storage Temperature Range……………………………………………..…………………….…..-65℃ to +150℃
Junction Temperature……………………………………………………………..…………………………150℃
24-Lead SSOP:
    Power Dissipation………………………………………………………………………………………450mW
    $θ_{JA}$ Thermal Impedance……………………………………………………………………………….112℃/W
    Lead Temperature, Soldering
       Phase Vapor(60sec)……..………………………………………………………………..215℃
       Infrared(15sec)…………………………………………………………………….………..220℃

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

10. Electrical Characteristics

(AV_{DD} = DV_{DD} = 5V ± 5%, AGND = DGND = 0V, On-Chip Reference, CLKIN = 3.579545MHz, T_{min} to T_{max} = -40℃ to +85℃.)

Parameter	Specifications	Unit	Test Conditions/Comments
Accuracy[1, 2]			
Measurement Error[1] on Channel 1			Channel 2 with Full-Scale Signal (±660 mV), 25℃
Gain = 1	0.1	% Reading typ	Over a Dynamic Range 500 to 1
Gain = 8	0.1	% Reading typ	Over a Dynamic Range 500 to 1
Gain = 16	0.1	% Reading typ	Over a Dynamic Range 500 to 1
Gain = 32	0.1	% Reading typ	Over a Dynamic Range 500 to 1
			Line Frequency = 45Hz to 65Hz
AC Power Supply Rejection[1]			
	0.2	% Reading typ	V1 = 100mV$_{rms}$, V2 = 100mV$_{rms}$, @50Hz
Output Frequency Variation (CF)			Ripple on AV_{DD} of 200mVrms @100Hz
			S0 = S1 = 1, G0 = G1 = 0
DC Power Supply Rejection[1]			
Output Frequency Variation (CF)	±0.3	% Reading typ	V1 = 100mV$_{rms}$, V2 = 100mV$_{rms}$,
			AV_{DD} = DV_{DD} = 5V ± 250mV
Analog Inputs			See Analog Inputs section
Maximum Signal Levels	±1	V max	V1P, V1N, V2N, and V2P to AGND
Input Impedance (DC)	390	kΩ min	CLKIN = 3.579545MHz
Bandwidth (–3dB)	14	kHz typ	CLKIN/256, CLKIN = 3.579545MHz
ADC Offset Error[1, 2]	±25	mV max	Gain = 1, See Terminology and Performance Graphs
Gain Error[1]	±7	% Ideal typ	External 2.5 V Reference, Gain = 1
			V1 = 470mV$_{dc}$, V2 = 660mV$_{dc}$
Gain Error Match[1]	±0.2	% Ideal typ	External 2.5 V Reference

Parameter	Specifications	Unit	Test Conditions/Comments
Reference Input			
REF$_{IN/OUT}$ Input Voltage Range	2.7	V max	2.5V + 8%
	2.3	V min	2.5V – 8%
Input Impedance	3.2	kΩ min	
Input Capacitance	10	pF max	
On-Chip Reference			Nominal 2.5V
Reference Error	±200	mV max	
Temperature Coefficient	±30	ppm/℃ typ	
CLKIN			**Note:**
Input Clock Frequency	4	MHz max	All Specifications for CLKIN of 3.579545MHz
	1	MHz min	
Logic Inputs[3] SCF,SO,S1,$\overline{RESET}$,GO,and G1			
Input High Voltage, V$_{INH}$	2.4	V min	DV$_{DD}$ = 5V ± 5%
Input Low Voltage, V$_{INL}$	0.8	V max	DV$_{DD}$ = 5 V ± 5%
Input Current, I$_{IN}$	± 3	µA max	Typically 10nA, V$_{IN}$ = 0 V to DV$_{DD}$
Input Capacitance, C$_{IN}$	10	pF max	
Logic Output[3] F1 and F2			
Output High Voltage, V$_{OH}$	4.5	V min	I$_{SOURCE}$ = 10mA DV$_{DD}$ = 5V
Output Low Voltage, V$_{OL}$	0.5	V max	I$_{SINK}$ = 10mA DV$_{DD}$ = 5V
CF and REVP			
Output High Voltage, V$_{OH}$	4	V min	I$_{SOURCE}$ = 5mA DV$_{DD}$ = 5V
Output Low Voltage, V$_{OL}$	0.5	V max	I$_{SINK}$ = 5mA DV$_{DD}$ = 5V
Power Supply			For Specified Performance
AV$_{DD}$	4.75	V min	5V – 5%
	5.25	V max	5V + 5%
DV$_{DD}$	4.75	V min	5V – 5%
	5.25	V max	5V + 5%
AI$_{DD}$	3	mA max	Typically 2mA
DI$_{DD}$	2.5	mA max	Typically 1.5mA

Note:
[1]See Terminology section for explanation of specifications.
[2]See Plots in Typical Performance Graphs.
[3]Sample tested during initial release and after any redesign or process changes that may affect this parameter.

Specifications subject to change without notice.

11.   Timing Characteristics1, 2

(AV_{DD} = DV_{DD} = 5V±5%, AGND = DGND = 0V, On-Chip Reference, CLKIN = 3.579545MHz, T_{min} to T_{max} = –40℃ to +85℃.)

Parameter	Specifications	Unit	Test Conditions/Comments
t_1^3	275	ms	F1 and F2 Pulse width (Logic Low)
t_2	See Table Ⅲ	sec	Output Pulse Period. See Transfer Function section.
t_3	1/2 t_2	sec	Time between F1 Falling Edge and F2 Falling Edge.
$t_4^{3, 4}$	90	ms	CF Pulse Width (Logic High).
t_5	See Table Ⅳ	sec	CF Pulse Period. See Transfer Function section.
t_6	CLKIN/4	sec	Minimum Time between F1 and F2 Pulse.

Note:
[1]Sample tested during initial release and after any redesign or process changes that may affect this parameter.
[2]See Fig4.
[3]The pulse widths of F1, F2, and CF are not fixed for higher output frequencies. See Frequency Outputs section.
[4]The CF pulse is always 18µs in the high frequency mode. See Frequency Outputs section and Table Ⅳ.

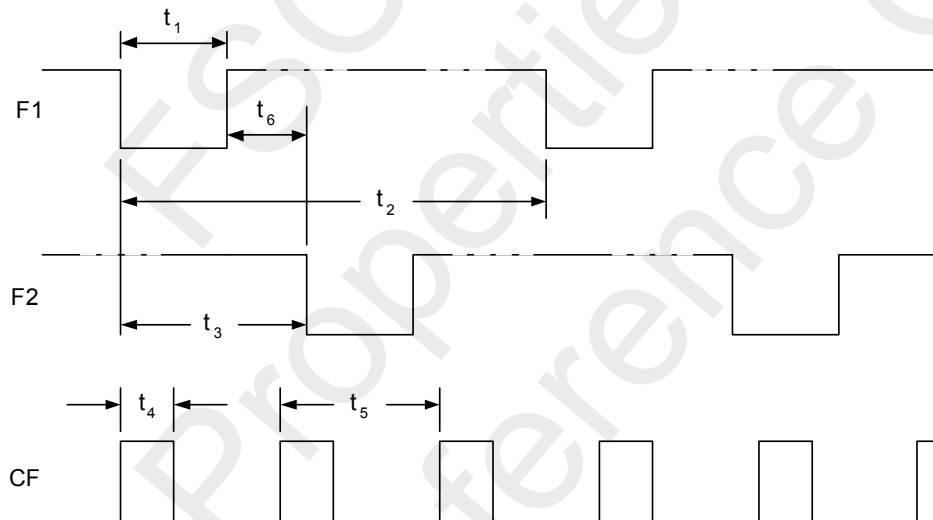Specifications subject to change without notice.

Fig4   Timing Characteristics for Impulse Output

12. Terminology

1   Measurement Error
The error associated with the energy measurement made by the FS7755 is defined by the following equation:

$$\text{Percentage Error} = \frac{\text{Energy Measured by the FS6611 - True Energy}}{\text{True Energy}} \times 100\%$$

2   Power Supply Rejection
This quantifies the FS7755 measurement error as a percentage of the reading when the power supplies are varied.

For the ac PSR measurement, a reading at nominal supplies (5V) is taken. A 200mV$_{rms}$/100Hz signal is then introduced onto the supplies and a second reading obtained under the same input signal levels. Any error introduced is expressed as a percentage of the reading (see Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (5V) is taken. The supplies are then varied ±5% and a second reading is obtained with the same input signal levels. Any error introduced is again expressed as a percentage of the reading.

3   ADC Offset Error
This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a small dc signal (offset). The offset decreases with increasing gain in Channel V1. This specification is measured at a gain of 1. At a gain of 16, the dc offset is typically less than 1mV.

4   Gain Error
The gain error of the FS7755 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. It is measured with a gain of 1 in Channel V1. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the FS7755 transfer function (see Transfer Function section).

5   Gain Error Match
The gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1 and a gain of 8, 16, or 32. It is expressed as a percentage of the output frequency obtained under a gain of 1. This gives the gain error observed when the gain selection is changed from 1 to 8, 16, or 32.

13. Detail Description

1   Theroy of Operation

The two ADCs digitize the voltage signals from the current and voltage transducers. These ADCs are 16-bit second order sigma-delta with an oversampling rate of 895 kHz. This analog input structure greatly simplifies transducer interfacing by providing a wide dynamic range for direct connection to the transducer and also by simplifying the anti-aliasing filter design. A programmable gain stage in the current channel further facilitates easy transducer interfacing.

The real power calculation is derived from the instantaneous multiplication of the current and voltage signals. In order to extract the real power component (i.e., the DC component), the instantaneous real power signal is a low pass filter output. Fig5 illustrates the instantaneous real power signal. This scheme correctly calculates instantaneous real power for non-sinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.
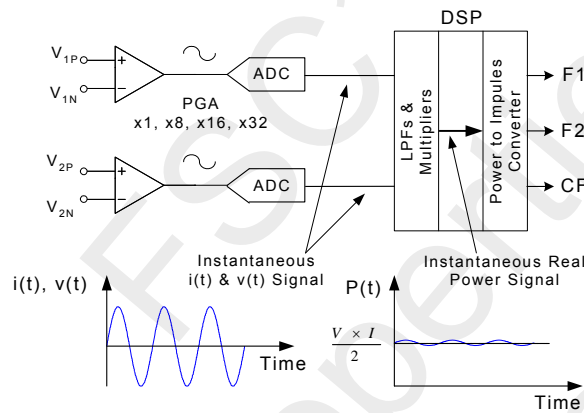

Fig5   Signal Flow Diagram

The low frequency output of the FS7755 is generated by accumulating this real power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average real power. This average real power information can, in turn, be accumulated (e.g., by a counter) to generate real energy information. Because of its high output frequency and shorter integration time, the CF output is proportional to the instantaneous real power. This is useful for system calibration purposes that would take place under steady load conditions.

2   Power Factor Considerations

The method used to extract the real power information from the instantaneous power signal (i.e., by low pass filtering) is still valid even when the voltage and current signals are not in phase. Fig6 displays the unity power factor and a power factor = 0.5 conditions, i.e., current signal lagging the voltage by 60^0. If we assume the voltage and current waveforms are sinusoidal, the real power component of the instantaneous power signal (i.e., the DC term) is given by:

$$\left(\frac{V \times I}{2} \right) \times \cos(60^0)$$
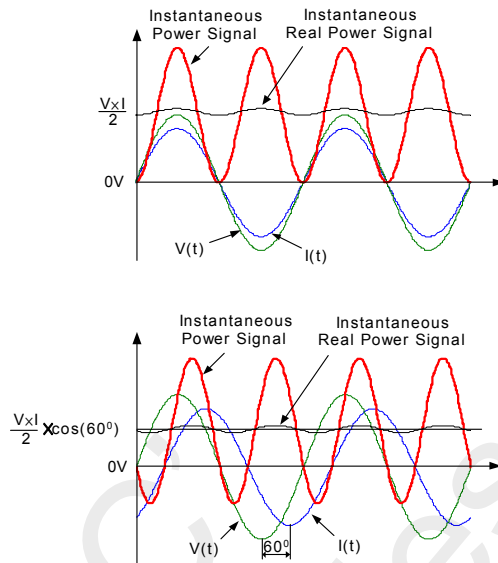
This is the correct real power calculation.

Fig6 DC Component of Instantaneous Power Signal
Conveys Real Power Information (PF $\leq$ 1)

3   Non-sinusoidal Voltage and Current

The real power calculation method also holds true for non-sinusoidal current and voltage waveforms. All voltage and current waveforms in practical applications will have some harmonic content. Using the Fourier Transform, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content.

$$v(t) = V_0 + \sqrt{2} \times \sum_{h \neq 0}^{\infty} V_h \times \sin(h\omega t + \alpha_h) \qquad (1)$$

Where:

$v(t)$ is the instantaneous voltage
V_0 is the average value
V_h is the rms value of voltage harmonic h

and

α_h is the phase angle of the voltage harmonic

$$i(t) = I_0 + \sqrt{2} \times \sum_{h \neq 0}^{\infty} I_h \times \sin(h\omega t + \beta_h) \qquad (2)$$

Where:

$i(t)$ is the instantaneous current
I_0 is the dc component
I_h is the rms value of current harmonic h

and

β_h is the phase angle of the current harmonic

Using Equations (1) and (2), the real power P can be expressed in terms of its fundamental real power (P_1) and harmonic real power (P_h).

$P = P_1 + P_h$

Where:

$P_1 = V_1 \times I_1 \cos\varphi_1 \qquad (3)$
$\varphi_1 = \alpha_1 - \beta_1$

and:

$$P_h = \sum_{h \neq 1}^{\infty} V_h \times I_h \cos\varphi_h \qquad (4)$$

$$\Phi_h = \alpha_h - \beta_h$$

As can be seen from Equation (4) above, a harmonic real power component is generated for every harmonic, provided that harmonic is present in both the voltage and current waveforms. The power factor calculation has previously been shown to be accurate in the case of a pure sinusoid; therefore the harmonic real power must also correctly account for the power factor since it is made up of a series of pure sinusoids.

Note:
The input bandwidth of the analog inputs is 14 kHz with a master clock frequency of 3.579545MHz.

4 Analog Inputs

4.1 Channel V1 (Current Channel)

The voltage output from the current transducer is connected to the FS7755 here. Channel V1 is a fully differential voltage input. V1P is the positive input with respect to V1N.

The maximum peak differential signal on Channel 1 should be less than ±470mV (330mV rms for a pure sinusoidal signal) for specified operation. Note that Channel 1 has a programmable gain amplifier (PGA) with user selectable gain of 1, 2, 8, or 16 (see Table I). These gains facilitate easy transducer interfacing.

Fig7 illustrates the maximum signal levels on V1P and V1N. The maximum differential voltage is ±470mV divided by the gain selection. The differential voltage signal on the inputs must be referenced to a common mode, e.g., AGND. The maximum common mode signal is ±100 mV as shown in Fig7.
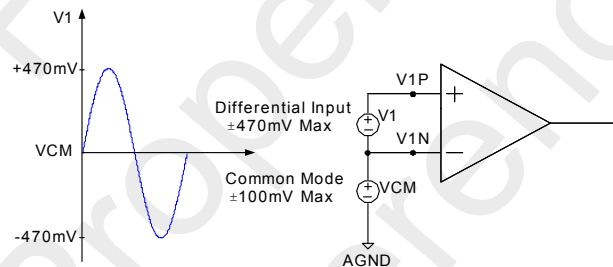

Fig7 Maximum Signal Levels (Channel 1, Gain = 1)

G1	G0	Gain	Maximum Differential Signal (mV)
0	0	1	±470
0	1	32	±15
1	0	8	±60
1	1	16	±30

Table I   Gain Selection for Channel 1

4.2 Channel V2 (Voltage Channel)

The output of the line voltage transducer is connected to the FS7755 at this analog input. Channel V2 is a fully differential voltage input. The maximum peak differential signal on Channel 2 is ± 660mV.
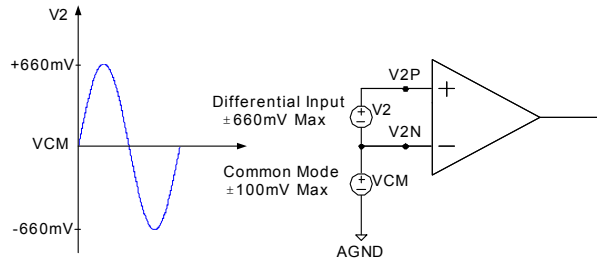

Fig8   Maximum Signal Levels (Channel 2)

Fig8 illustrates the maximum signal levels that can be connected to the FS7755 Channel 2. Channel 2 must be driven from a common-mode voltage, i.e., the differential voltage signal on the input must be referenced to a common mode (usually AGND). The analog inputs of the FS7755 can be driven with common-mode voltages of up to 100mV with respect to AGND. However, best results are achieved using a common mode equal to AGND.

4.3 Typical Connection Diagrams

Fig9 shows a typical connection diagram for Channel V1. A CT (Current Transformer) is the current transducer selected for this example. Notice the common-mode voltage for Channel 1 is AGND and is derived by center tapping the burden resistor to AGND. This provides the complementary analog input signals for V1P and V1N. The CT turns ratio and burden resistor R_b are selected to give a peak differential voltage of ±470mV/Gain at maximum load.
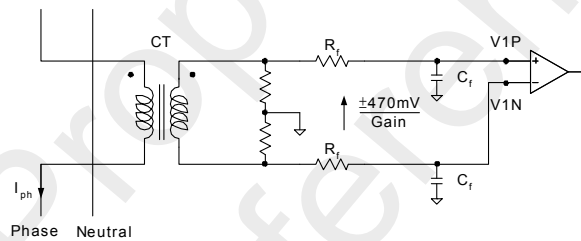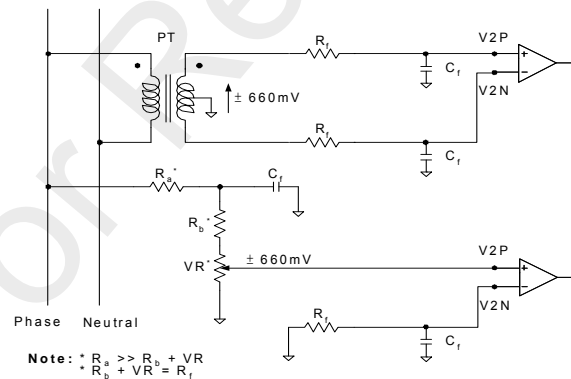

Fig9   Typical Connection for Channel 1

Fig10   Typical Connection for Channel 2

Fig10 shows two typical connections for Channel V2. The first option uses a PT (Potential Transformer) to provide complete isolation from the power line. In the second option, the FS7755 is biased around the neutral wire, and a resistor divider provides a voltage signal that is proportional to the line voltage. Adjusting the ratio of R_a, R_b and VR is also a convenient way of carrying out a gain calibration on the meter.

5 Power Supply Monitor

The FS7755 contains an on-chip power supply monitor. The Analog Supply (AV_{DD}) is continuously monitored by the FS7755. If the supply is less than 4V ± 5%, the FS7755 will be reset. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

In Fig11, the trigger level is nominally set at 4V. The tolerance on this trigger level is about ±5%. The power supply and decoupling for the part should be such that the ripple at AV_{DD} does not exceed 5V ± 5% as specified for normal operation.
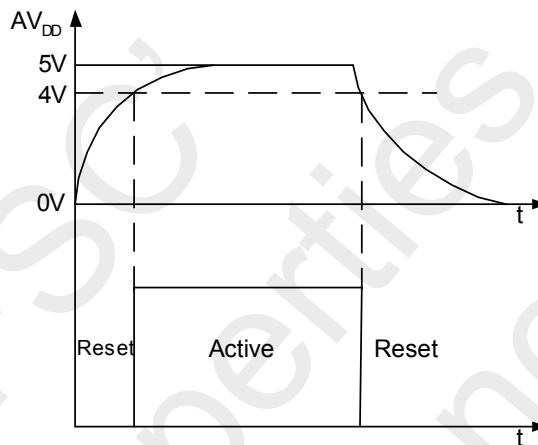

Fig11   On-Chip Power Supply Monitor

6 Power to Impulse Converter

As previous descriptions, the digital output of the low pass filter after multiplication contains the real power information. However, since this LPF is not an ideal "brick wall" filter implementation, the output signal also contains attenuated components at the line frequency and its harmonics, i.e., cos($h\omega$t) where h = 1, 2, 3, and so on. Fig12 shows the instantaneous real power signal at the output of the LPF, which still contains a significant amount of instantaneous power information, i.e. cos(2ωt). This signal is then passed to the digital to frequency converter where it is integrated (accumulated) over time to produce an output frequency. This accumulation of the signal will suppress or average out any non-DC components in the instantaneous real power signal. The average value of a sinusoidal signal is zero. Hence, the frequency generated by the FS7755 is proportional to the average real power. Fig12 shows the digital to frequency converter for steady load conditions, i.e., constant voltage and current.
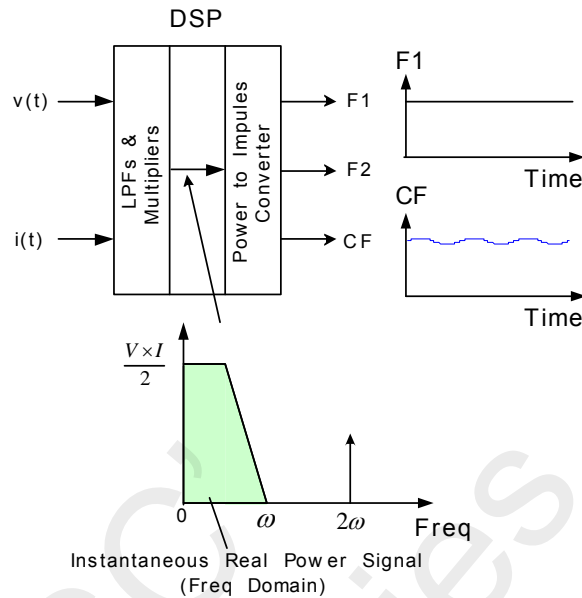
DSP

Fig12 Real Power to Impulse Converter

As can be seen in Fig12, the frequency output CF is seen to vary over time, even under steady load conditions. This frequency variation is primarily due to the cos(2ωt) component in the instantaneous real power signal. The output frequency on CF can be up to 2048 times higher than the frequency on F1 and F2. This higher output frequency is generated by accumulating the instantaneous real power signal over a much shorter time while converting it to a frequency. This shorter accumulation period means less averaging of the cos(2ωt) component. As a consequence, some of this instantaneous power signal passes through the digital to frequency converter. This will not be a problem in the application. When CF is used for calibration purposes, the frequency should be averaged by the impulse counter. This will remove any ripple. If CF is measuring energy, e.g., in a microprocessor based application, the CF output should also be averaged to calculate power. Because the outputs F1 and F2 operate at a much lower frequency, more averaging of the instantaneous real power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple-free frequency output.

7   Interfacing the FS7755 to a Micro- Controller for Energy Measurement

The easiest way to interface the FS7755 to a micro-Controller is to use the CF high frequency output with the output frequency scaling set to 2048×F1, F2. This is done by setting SCF = 0 and S0 = S1 = 1 (see Table IV). With full-scale AC signals on the analog inputs, the output frequency on CF will be approximately 5.57 kHz. Fig13 illustrates one scheme that could be used to digitize the output frequency and carry out the necessary averaging mentioned in the previous section.
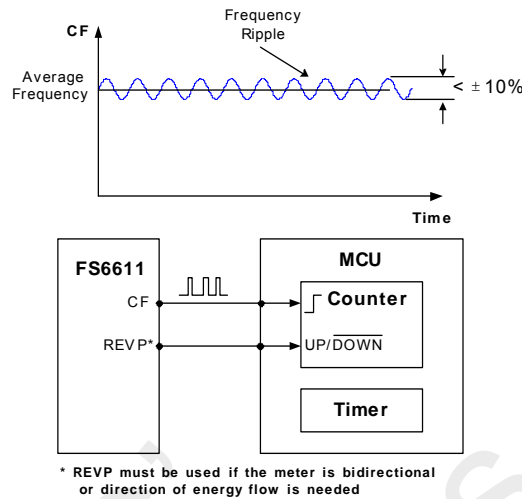
Fig13 Interfacing the FS7755 to MCU

As shown, the frequency output CF is connected to an MCU counter or port. This will count the number of pulses in a given integration time that is determined by an MCU internal timer. The average power proportional to the average frequency is given by:

$$\text{Average Frequency} = \text{Average Real Power} = \frac{\text{Counter}}{\text{Timer}}$$

The energy consumed during an integration period is given by:

$$\text{Energy} = \text{Average Power} \times \text{Time} = \frac{\text{Counter}}{\text{Time}} \times \text{Time} = \text{Counter}$$

For the purpose of calibration, this integration time can be 10 to 20 seconds to accumulate enough pulses to ensure correct averaging of the frequency. In normal operation, the integration time can be reduced to one or two seconds depending, for example, on the required update rate of a display. With shorter integration times on the MCU, the amount of energy in each update may still have some small amount of ripple, even under steady load conditions. However, over a minute or more, the measured energy will have no ripple.

7.1 Power Measurement Considerations

Calculating and displaying power information will always have some associated ripple that will depend on the integration period used in the MCU to determine average power and also the load. For example, at light loads, the output frequency may be 10Hz. With an integration period of two seconds, only about 20 pulses will be counted. The possibility of missing one pulse always exists, since the FS7755 output frequency is running asynchronously to the MCU timer. This would result in a one-in-twenty (or 5%) error in the power measurement.

8 Transfer Function

8.1 Frequency Outputs F1 and F2

The FS7755 calculates the product of two voltage signals (on Channel 1 and Channel 2) and then low pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low, e.g., 0.34Hz maximum for AC signals with S0 = S1 = 0 (see Table III). This means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average real power. The averaging of the real power signal is implicit to the power to impulse converter. The output frequency or pulse rate is related to the input voltage signals by the following equation.

$$\text{Freq} = \frac{8.06 \times V1 \times V2 \times Gain \times F_{1-4}}{V_{REF}^2}$$

Where:

Freq: Output frequency on F1 and F2 (Hz)

V1: Differential rms voltage signal on Channel 1 (Volts)

V2: Differential rms voltage signal on Channel 2 (Volts)

Gain: 1, 2, 8, or 16, depending on the PGA gain selection made using logic inputs G0 and G1

V_{REF}: The reference voltage (2.5V ± 8%)

F_{1-4}: One of four possible frequencies selected by using the logic inputs S0 and S1—see Table II

S1	S0	F_{1-4}(Hz)	XTAL/CLKIN[*]
0	0	1.7	3.579545MHz/2^{21}
0	1	3.4	3.579545MHz/2^{20}
1	0	6.8	3.579545MHz/2^{19}
1	1	13.6	3.579545MHz/2^{18}

Table II F_{1-4} Frequency Selection

Note:
[*]F_{1-4} is a binary fraction of the master clock and therefore will vary if the specified CLKIN frequency is altered.

14. Example

In this example, with AC voltages of ±470mV peak applied to V1 and ±660mV peak applied to V2, the expected output frequency is calculated as follows:

Gain = 1, G0 = G1 = 0
F_{1-4} = 1.7Hz, S0 = S1 = 0

V1 = rms of 470mV peak ac = 0.47/$\sqrt{2}$ Volts

V2 = rms of 660mV peak ac = 0.66/$\sqrt{2}$ Volts
V_{REF} = 2.5V (nominal reference value)

Note:
If the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$\text{Freq} = \frac{8.06 \times 0.47 \times 0.66 \times 1 \times 1.7}{\sqrt{2} \times \sqrt{2} \times 2.5^2} = 0.34 \text{ (Hz)}$$

Table Ⅲ shows a complete listing of all maximum output frequencies.

S1	S0	Max Frequency for AC Inputs (Hz)
0	0	0.34
0	1	0.68
1	0	1.36
1	1	2.72

Table Ⅲ Maximum Output Frequency on F1 and F2

1. Frequency Output CF

The pulse output CF (Calibration Frequency) is intended for use during calibration. The output pulse rate on CF can be up to 2048 times the pulse rate on F1 and F2. The lower the F_{1-4} frequency selected, the higher the CF scaling (except for the high frequency mode SCF = 0, S1 = S0 = 1). Table Ⅳ shows how the two frequencies are related, depending on the states of the logic inputs S0, S1, and SCF. Because of its relatively high pulse rate, the frequency at this logic output is proportional to the instantaneous real power. As is the case with F1 and F2, the frequency is derived from the output of the

low-pass filter after multiplication. However, because the output frequency is high, this real power information is accumulated over a much shorter time. Hence, less averaging is carried out in the digital to frequency converter. With much less averaging of the real power signal, the CF output is much more responsive to power fluctuations (see Fig2, Signal Processing Block Diagram).

SCF	S1	S0	F_{1-4} (Hz)	CF Max for AC Signals (Hz)
1	0	0	1.7	128×F1, F2 = 43.52
0	0	0	1.7	64×F1, F2 = 21.76
1	0	1	3.4	64×F1, F2 = 43.52
0	0	1	3.4	32×F1, F2 = 21.76
1	1	0	6.8	32×F1, F2 = 43.52
0	1	0	6.8	16×F1, F2 = 21.76
1	1	1	13.6	16×F1, F2 = 43.52
0	1	1	13.6	2048×F1, F2 = 5570

Table Ⅳ   Maximum Output Frequency on CF

2. Selecting a Frequency for an Energy Meter Application

As shown in Table II, the user can select one of four frequencies. This frequency selection determines the maximum frequency on F1 and F2. These outputs are intended to be used to drive the energy register (electromechanical or other). Since only four different output frequencies can be selected, the available frequency selection has been optimized for a meter constant of 100imp/kWhr with a maximum current of between 10A and 120A. Table V shows the output frequency for several maximum currents (I_{Max}) with a line voltage of 220V. In all cases the meter constant is 100imp/kWhr.

I_{Max} (A)	F1 and F2 (Hz)
12.5	0.076
25	0.153
40	0.244
60	0.367
80	0.489
120	0.733

Table Ⅴ   F1 and F2 Frequency at 100imp/kWhr

The F_{1-4} frequencies allow complete coverage of this range of output frequencies on F1 and F2. When designing an energy meter, the nominal design voltage on Channel 2 (voltage) should be set to half scale to allow for calibration of the meter constant. The current channel should also be no more than half scale when the meter sees maximum load. This will allow over current signals and signals with high crest factors to be accommodated. Table VI shows the output frequency on F1 and F2 when both analog inputs are half scale. The frequencies listed in Table VI align very well with those listed in Table V for maximum load.

S1	S0	F_{1-4} (Hz)	Frequency on F1 and F2 (Hz) (Ch1 and Ch2 Half Scale AC Inputs)
0	0	1.7	0.085
0	1	3.4	0.17
1	0	6.8	0.34
1	1	13.6	0.68

Table VI   F1 and F2 Frequency with Half Scale AC Inputs

When selecting a suitable F_{1-4} frequency for a meter design, the frequency output at I_{Max} (maximum load) with a meter constant of 100imp/kWhr should be compared with Column 4 of Table VI. The frequency that is closest in Table VI will determine the best choice of frequency (F_{1-4}). For example, if a meter with a maximum current of 25A is being designed, the output frequency on F1 and F2 with a meter constant of 100imp/kWhr is 0.153Hz at 25A and 220V (from Table V). Looking at Table VI, the closest frequency to 0.153Hz in column four is 0.17Hz. Therefore, F2 (3.4Hz—see Table II) is selected for this design.

Fortune

2.1 Frequency Outputs

Fig4 shows a timing diagram for the various frequency outputs. The outputs F1 and F2 are the low frequency outputs that can be used to directly drive a stepper motor or electromechanical impulse counter. The F1 and F2 outputs provide two alternating low going pulses. The pulse width (t_1) is set at 275ms and the time between the falling edges of F1 and F2 (t_3) is approximately half the period of F1 (t_2). If, however, the period of F1 and F2 falls below 550ms (1.81Hz), the pulse width of F1 and F2 is set to half of their period. The maximum output frequencies for F1 and F2 are shown in Table Ⅲ.

The high frequency CF output is intended to be used for communications and calibration purposes. CF produces a 90ms wide active high pulse (t_4) at a frequency proportional to active power. The CF output frequencies are given in Table Ⅳ. As in the case of F1 and F2, if the period of CF (t_5) falls below 180 ms, the CF pulse width is set to half the period. For example, if the CF frequency is 20Hz, the CF pulse width is 25ms.
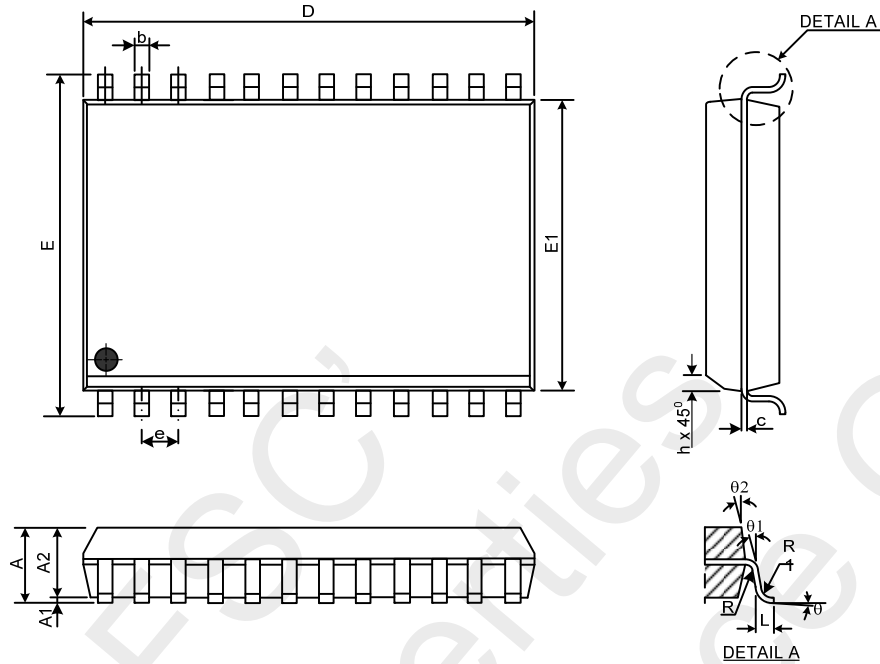
Note:
When the high frequency mode is selected, (i.e., SCF = 0, S1 = S0 = 1), the CF pulse width is fixed at 18μs. Therefore, t4 will always be 18μs, regardless of the output frequency on CF.

3. No Load Threshold

The FS7755 also includes a "no load threshold" and "startup current" feature that will eliminate any creep effects in the meter. The FS7755 is designed to issue a minimum output frequency on all modes except when SCF = 0 and S1 = S0 = 1. The no load detection threshold is disabled on this output mode to accommodate specialized application of the FS7755. Any load generating a frequency lowers than this minimum frequency will not cause a pulse to be issued on F1, F2, or CF. The minimum output frequency is given as 0.0014% of the full scale output frequency for each of the F_{1-4} frequency selections (see Table II). For example, an energy meter with a meter constant of 100imp/kWhr on F1 and F2, using F2 (3.4Hz), the maximum output frequency at F1 or F2 would be 0.0014% of 3.4Hz or $4.76×10^{-5}$Hz. This would be $3.05×10^{-3}$Hz at CF (64 ×F1 Hz). In this example, the no-load threshold is equivalent to 1.7W of load or a start up current of 8mA at 220V. IEC1036 states that the meter must start up with a load current equal to or less than 0.4% I_b. For a 5A (I_b) meter, 0.4% I_b is equivalent to 20mA. The start up current of this design therefore satisfies the IEC requirement. As illustrated from this example, the choice of F_{1-4} and the ratio of the stepper motor display will determine the start up current.

15. Package Outline

SSOP-24

Note:
1. Controlling dimension: mm
2. Refer to JEDEC MO – 150AG
3. Dimension "D" does not include Mold Flash, Protrusions or Gate Burrs. Mold Flash, Protrusions and Gate Burrs shall not exceed 0.006" (0.15mm) per end;
4. Dimension "E" does not include Interlead Flash or Protrusions. Interlead Flash and Protrusion shall not exceed 0.010" (0.25mm) per side;
5. Tolerance: ±0.010" (0.25mm) unless otherwise specified
6. Otherwise dimension follow acceptable spec.

Symbols	Dimensions in mm			Dimensions in Inches		
	Min	Nom	Max	Min	Nom	Max
A	──	──	2.0	──	──	0.079
A1	0.05	──	──	0.002	──	──
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	──	0.38	0.009	──	0.015
C	0.09	──	0.25	0.004	──	0.01
D	7.90	8.20	8.50	0.311	0.323	0.345
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	0.65 BSC			0.026 BSC		
L	0.55	0.75	0.95	0.022	0.030	0.037
R1	0.09	──	──	0.004	──	──
R2	0.09	──	──	0.004	──	──
y	──	──	0.10	──	──	0.004
θ	0°	4°	8°	0°	4°	8°
θ1	0°	──	──	0°	──	──
θ2	7° TYP			7° TYP		