MX26LV004T/B

Macronix NBit™ Memory Family

4M-BIT [512K x 8] CMOS SINGLE VOLTAGE 3V ONLY HIGH SPEED eLiteFlash™ MEMORY

FEATURES

- Extended single - supply voltage range 3.0V to 3.6V
- 524,288 x 8
- Single power supply operation
  - 3.0V only operation for read, erase and program operation
- Fast access time: 55/70ns
- Low power consumption
  - 30mA maximum active current
  - 30uA typical standby current
- Command register architecture
  - Byte Programming (55us typical)
  - Sector Erase (Sector structure 16K-Byte x1, 8K-Byte x2, 32K-Byte x1, and 64K-Byte x7)
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Status Reply
  - $\overline{\text{Data}}$ polling & Toggle bit for detection of program and erase operation completion.
- Ready/$\overline{\text{Busy}}$ pin (RY/$\overline{\text{BY}}$)
  - Provides a hardware method of detecting program or erase operation completion.
- 2,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Package type:
  - 40-pin TSOP
  - 32-pin PLCC
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash
- 20 years data retention

GENERAL DESCRIPTION

The MX26LV004T/B is a 4-mega bit Flash memory organized as 512K bytes of 8 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX26LV004T/B is packaged in 40-pin TSOP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX26LV004T/B offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX26LV004T/B has separate chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) controls.

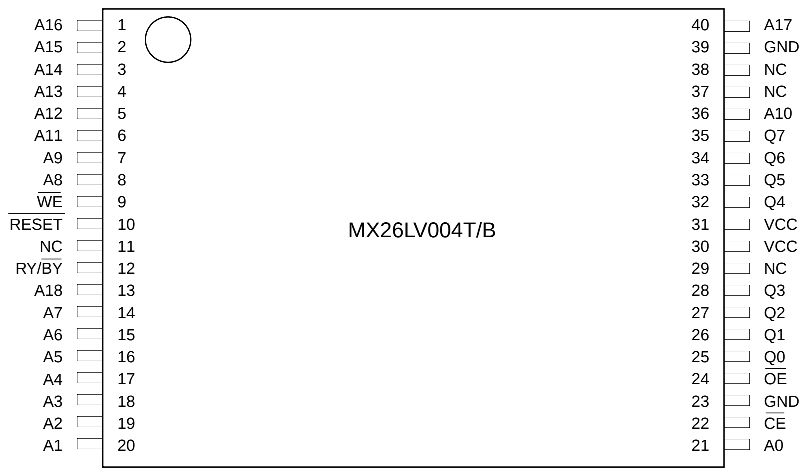
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX26LV004T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 2,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and program operations produces reliable cycling. The MX26LV004T/B uses a 3.0V~3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

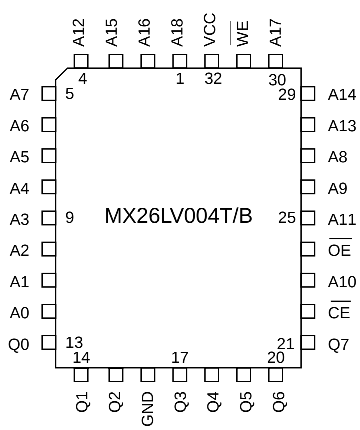
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

40 TSOP (Standard Type) (10mm x 20mm)



32 PLCC



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A18	Address Input
Q0~Q7	Data Input/Output
CE	Chip Enable Input
WE	Write Enable Input
RESET	Hardware Reset Pin
OE	Output Enable Input
RY/BY	Ready/Busy Output
VCC	Power Supply Pin (3.0V~3.6V)
GND	Ground Pin

BLOCK STRUCTURE

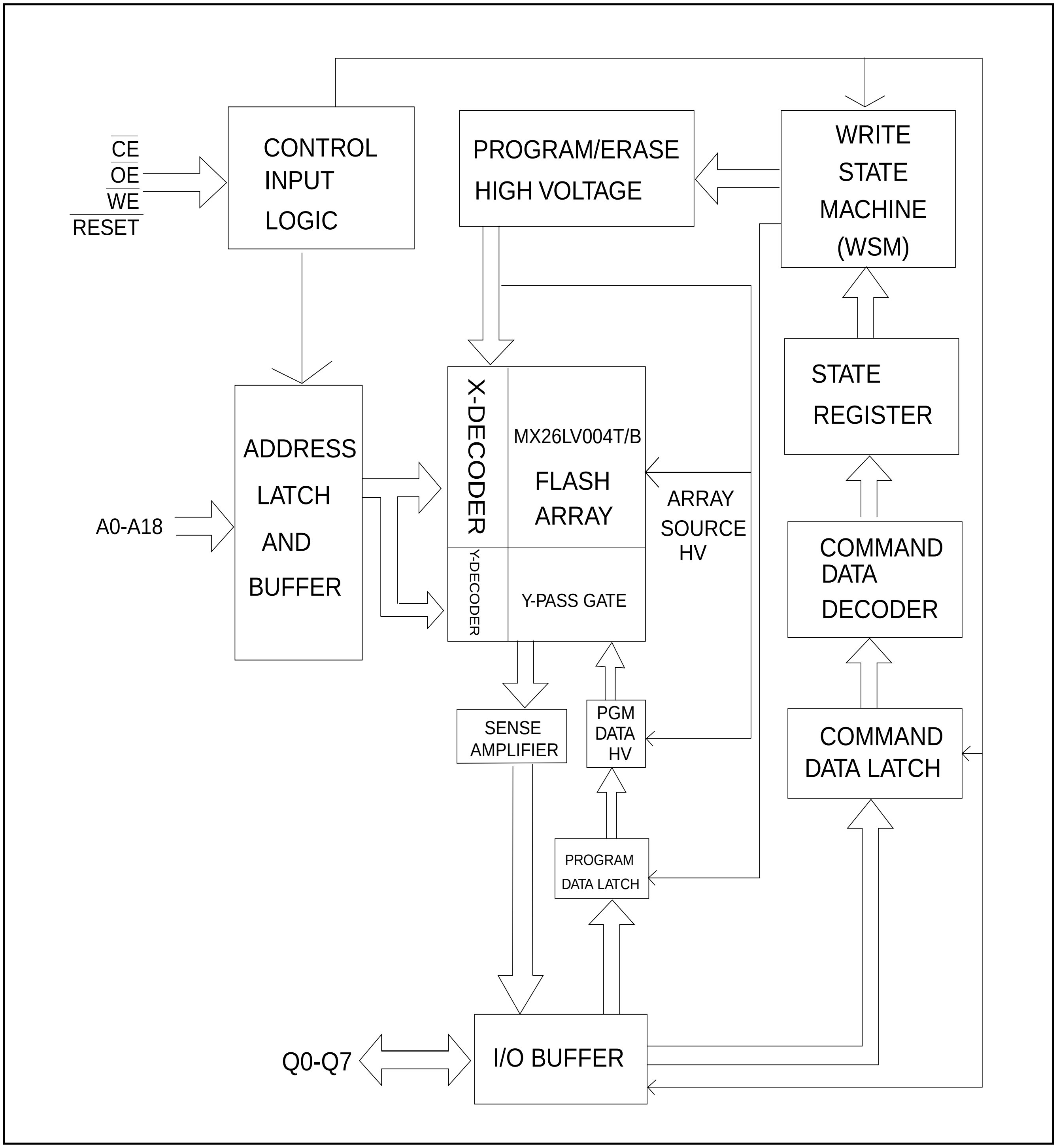
Table 1: MX26LV004T SECTOR ARCHITECTURE

Sector	Sector Size	Address range	Sector Address					
	Byte Mode	Byte Mode (x8)	A18	A17	A16	A15	A14	A13
SA0	64Kbytes	00000-0FFFF	0	0	0	X	X	X
SA1	64Kbytes	10000-1FFFF	0	0	1	X	X	X
SA2	64Kbytes	20000-2FFFF	0	1	0	X	X	X
SA3	64Kbytes	30000-3FFFF	0	1	1	X	X	X
SA4	64Kbytes	40000-4FFFF	1	0	0	X	X	X
SA5	64Kbytes	50000-5FFFF	1	0	1	X	X	X
SA6	64Kbytes	60000-6FFFF	1	1	0	X	X	X
SA7	32Kbytes	70000-77FFF	1	1	1	0	X	X
SA8	8Kbytes	78000-79FFF	1	1	1	1	0	0
SA9	8Kbytes	7A000-7BFFF	1	1	1	1	0	1
SA10	16Kbytes	7C000-7FFFF	1	1	1	1	1	X

Table 2: MX26LV004B SECTOR ARCHITECTURE

Sector	Sector Size	Address range	Sector Address					
	Byte Mode	Byte Mode (x8)	A18	A17	A16	A15	A14	A13
SA0	16Kbytes	00000-03FFF	0	0	0	0	0	X
SA1	8Kbytes	04000-05FFF	0	0	0	0	1	0
SA2	8Kbytes	06000-07FFF	0	0	0	0	1	1
SA3	32Kbytes	08000-0FFFF	0	0	0	1	X	X
SA4	64Kbytes	10000-1FFFF	0	0	1	X	X	X
SA5	64Kbytes	20000-2FFFF	0	1	0	X	X	X
SA6	64Kbytes	30000-3FFFF	0	1	1	X	X	X
SA7	64Kbytes	40000-4FFFF	1	0	0	X	X	X
SA8	64Kbytes	50000-5FFFF	1	0	1	X	X	X
SA9	64Kbytes	60000-6FFFF	1	1	0	X	X	X
SA10	64Kbytes	70000-7FFFF	1	1	1	X	X	X

BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX26LV004T/B is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to DATA polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation. Refer to write operation status, table 7, for more information on these status bits.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX26LV004T/B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device. An erase operation can erase one sector, multiple sectors, or the entire device.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the erasing operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of WE or CE, whichever happens first.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX26LV004T/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

AUTOMATIC SELECT

The auto select mode provides manufacturer and device identification, through identifier codes output on Q7~Q0. This mode is mainly adapted for programming equipment on the device to be programmed with its programming algorithm. When programming by high voltage method, automatic select mode requires VID (11V to 12V) on address pin A9 and other address pin A6, A1 and A0 as referring to Table 3. In addition, to access the automatic select codes in-system, the host can issue the automatic select command through the command register without requiring VID, as shown in table 4.

TABLE 3. MX26LV004T/B AUTO SELECT MODE OPERATION

Description		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A18 | A13	A12 | A10	A9	A8 | A7	A6	A5 | A2	A1	A0	Q7~Q0
Read Silicon ID	Manufacturer Code	L	L	H	X	X	VID	X	L	X	L	L	C2H
	Device ID (Top Boot Block)	L	L	H	X	X	VID	X	L	X	L	H	B5H
	Device ID (Bottom Boot Block)	L	L	H	X	X	VID	X	L	X	L	H	B6H

NOTE:SA=Sector Address, X=Don't Care, L=Logic Low, H=Logic High

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 4 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress.

TABLE 4. MX26LV004T/B COMMAND DEFINITIONS

Command		Bus Cycle	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset		1	XXXH	F0H										
Read		1	RA	RD										
Read Silicon ID	Top Boot	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
	Bottom Boot	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
Program		4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase		6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase		6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H

Note:

1. ADI = Address of Device identifier; A1=0, A0 = 0 for manufacturer code,A1=0, A0 = 1 for device code. A2-A18=do not care. (Refer to table 3)
   DDI = Data of Device identifier : C2H for manufacture code, B5/B6 (Top/Bottom Boot) for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
2. PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address of the sector.
3. Address A18-A11 are don't cares for unlock and command cycles.

TABLE 5. MX26LV004T/B BUS OPERATION

DESCRIPTION	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	ADDRESS								Q0~Q7
					A18 | A13	A12 | A10	A9	A8 | A7	A6	A5 | A2	A1	A0	
Read	L	L	H	H	AIN								Dout
Write	L	H	L	H	AIN								DIN(3)
Reset	X	X	X	L	X								High Z
Output Disable	L	H	H	H	X								High Z
Standby	Vcc±0.3V	X	X	Vcc±0.3V	X								High Z

NOTES:

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 4.
2. VID is the Silicon-ID-Read high voltage, 11V to 12V.
3. Refer to Table 4 for valid Data-In during a write operation.
4. X can be VIL or VIH.

REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the CE and OE pins to VIL. CE is the power control and selects the device. OE is the output control and gates array data to the output pins. WE should remain at VIH.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid address on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

WRITE COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory , the system must drive WE and CE to VIL, and OE to VIH.

The "Byte Program Command Sequence" section has details on programming data to the device.

An erase operation can erase one sector, multiple sectors , or the entire device. Table indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Writing specific address and data commands or sequences into the command register initiates device operations. Table 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

STANDBY MODE

When using both pins of CE and RESET, the device enter CMOS Standby with both pins held at Vcc ± 0.3V. If CE and RESET are held at VIH, but not within the range of VCC ± 0.3V, the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation, Vcc active current (Icc2) is required even CE = "H" until the operation is completed. The device can be read with standard access time (tCE) from either of these standby modes, before it is ready to read data.

OUTPUT DISABLE

With the OE input at a logic high level (VIH), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

RESET OPERATION

The RESET pin provides a hardware method of resetting the device to reading array data. When the RESET pin is driven low for at least a period of tRP, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity

Current is reduced for the duration of the RESET pulse. When RESET is held at VSS±0.3V, the device draws CMOS standby current (ICC4). If RESET is held at VIL but not within VSS±0.3V, the standby current will be greater.

The RESET pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firm-ware from the Flash memory.

If RESET is asserted during a program or erase operation, the RY/BY pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of tREADY (during Embedded Algorithms). The system can thus monitor RY/BY to determine whether the reset operation is complete. If RESET is asserted when a program or erase operation is completed within a time of tREADY (not during Embedded Algorithms). The system can read data tRH after the RESET pin returns to VIH.

Refer to the AC Characteristics tables for RESET parameters and to Figure 20 for the timing diagram.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage (VID). However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX26LV004T/B contains a Silicon-ID-Read operation to supple traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register.

SET-UP AUTOMATIC CHIP/SECTOR ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H or sector erase command 30H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 7), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last WE or CE pulse, whichever happens first in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 6. SILICON ID CODE

Pins	A0	A1	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	VIL	VIL	1	1	0	0	0	0	1	0	C2H
Device code for MX26LV004T	VIH	VIL	1	0	1	1	0	1	0	1	B5H
Device code for MX26LV004B	VIH	VIL	1	0	1	1	0	1	1	0	B6H

READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to re-trieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The sys-tem can read array data using the standard read tim-ings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. Af-ter completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See erase Suspend/Erase Resume Commands" for more infor-mation on this mode. The system must issue the reset command to re-en-able the device for reading array data if Q5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the se-quence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the se-quence cycles in a program command sequence be-fore programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the se-quence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend).

If Q5 goes high during a program or erase operation, writing the reset command returns the device to read-ing array data (also applies during Erase Suspend).

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Sector Erase Set-up command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later, while the command (data) is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. Each successive sector load cycle started by the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later must begin within 50us from the rising edge of the preceding $\overline{WE}$ or $\overline{CE}$, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

BYTE PROGRAM COMMAND SEQUENCE

The device programs one byte of data for each program operation. The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 1 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using Q7, Q6, or RY/$\overline{BY}$. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set Q5 to "1" ," or cause the $\overline{Data}$ Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/$\overline{BY}$. Table 10 and the following subsections describe the functions of these bits. Q7, RY/$\overline{BY}$, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Q7: $\overline{Data}$ Polling

The $\overline{Data}$ Polling bit, Q7, indicates to the host sys-tem whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend. $\overline{Data}$ Polling is valid after the rising edge of the final $\overline{WE}$ pulse in the program or erase command sequence.

During the Automatic Program algorithm, the device outputs on Q7 the complement of the datum programmed to Q7. This Q7 status also applies to programming during Erase Suspend. When the Automatic Program algorithm is complete, the device outputs the datum programmed to Q7. The system must provide the program address to read valid status information on Q7.

During the Automatic Erase algorithm, Data Polling produces a "0" on Q7. When the Automatic Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data Polling produces a "1" on Q7. This is analogous to the complement/true datum out-put described for the Automatic Program algorithm: the erase function changes all the bits in a sector to "1" prior to this, the device outputs the "complement," or "0". The system must provide an address within any of the sectors selected for erasure to read valid status information on Q7.

When the system detects Q7 has changed from the complement to true data, it can read valid data at Q7-Q0 on the following read cycles. This is because Q7 may change asynchronously with Q0-Q6 while Output Enable (OE) is asserted low.

RY/BY:Ready/Busy

The RY/BY is a dedicated, open-drain output pin that indicates whether an Automatic Erase/Program algorithm is in progress or complete. The RY/BY status is valid after the rising edge of the final WE or CE, whichever happens first, in the command sequence. Since RY/BY is an open-drain output, several RY/BY pins can be tied together in parallel with a pull-up resistor to Vcc.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

Table 7 shows the outputs for RY/BY during write operation.

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE or CE, whichever happens first, in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE or CE to control the read cycles. When the operation is complete, Q6 stops toggling.

When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. However, the system must also use Q2 to determine which sectors are erasing. Alternatively, the system can use Q7.

Q6 stops toggling once the Automatic Program algorithm is complete.

Table 7 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE or CE, whichever happens first, in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE or CE to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 7 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector maynot be reused, (other sectors are still functional and can be reused).

The time-out condition will not appear if a user tries to program a non blank location without erasing. Please note that this is not a device failure condition since the device was incorrectly used.

Table 7. WRITE OPERATION STATUS

	Status	Q7 (Note1)	Q6	Q5 (Note2)	Q3	Q2	RY/$\overline{BY}$
In Progress	Byte Program in Auto Program Algorithm	$\overline{Q7}$	Toggle	0	N/A	No Toggle	0
	Auto Erase Algorithm	0	Toggle	0	1	Toggle	0
Exceeded Time Limits	Byte Program in Auto Program Algorithm	$\overline{Q7}$	Toggle	1	N/A	No Toggle	0
	Auto Erase Algorithm	0	Toggle	1	1	Toggle	0

Note:

1. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. Q5 switches to '1' when an Auto Program or Auto Erase operation has exceeded the maximum timing limits. See "Q5 : Exceeded Timing Limits" for more information.

Q3
Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

DATA PROTECTION

The MX26LV004T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

POWER-UP SEQUENCE

The MX26LV004T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages . . . . -65°C to +150°C

Ambient Temperature

with Power Applied. . . . . -65°C to +125°C

Voltage with Respect to Ground

VCC (Note 1) . . . . -0.5 V to +4.0 V

A9, $\overline{OE}$, and

$\overline{RESET}$ (Note 2) . . . . -0.5 V to +12 V

All other pins (Note 1) . . . . -0.5 V to VCC +0.5 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on pins A9, $\overline{OE}$, and $\overline{RESET}$ is -0.5 V. During voltage transitions, A9, $\overline{OE}$, and $\overline{RESET}$ may overshoot VSS to -2.0 V for periods of up to 20 ns. See Figure 6. Maximum DC input voltage on pin A9 is +12V which may overshoot to 13.5V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS

Commercial (C) Devices

Ambient Temperature (T_A). . . . . 0° C to +70° C

V_{CC} Supply Voltages

V_{CC} for full voltage range. . . . . +3.0 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN1	Input Capacitance			8	pF	VIN = 0V
CIN2	Control Pin Capacitance			12	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

Table 8. DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 3.0V ~ 3.6V

Symbol	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS	
ILI	Input Leakage Current			±1	uA	VIN = VSS to VCC	
ILIT	A9 Input Leakage Current			100	uA	VCC=VCC max; A9=12V	
ILO	Output Leakage Current			±1	uA	VOUT = VSS to VCC, VCC = VCC max	
ICC1	VCC Active Read Current		20	30	mA	$\overline{CE}$=VIL,	@5MHz
			8	14	mA	$\overline{OE}$=VIH	@1MHz
ICC2	VCC Active write Current		26	30	mA	$\overline{CE}$=VIL, $\overline{OE}$=VIH	
ICC3	VCC Standby Current		30	100	uA	$\overline{CE}$; $\overline{RESET}$=VCC ±0.3V	
ICC4	VCC Standby Current During Reset		30	100	uA	$\overline{RESET}$=VSS ±0.3V	
VIL	Input Low Voltage (Note 1)	-0.5		0.8	V		
VIH	Input High Voltage	0.7xVCC		VCC+ 0.3	V		
VID	Voltage for Automative Select	11		12	V	VCC=3.3V	
VOL	Output Low Voltage			0.45	V	IOL = 4.0mA, VCC = VCC min	
VOH1	Output High Voltage(TTL)	0.85xVCC				IOH = -2mA, VCC =VCC min	
VOH2	Output High Voltage (CMOS)	VCC-0.4				IOH = -100uA, VCC min	

NOTES:
1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.
3. Automatic sleep mode enable the low power mode when addresses remain stable for tACC +30ns.

AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 3.0V~3.6V

Table 9. READ OPERATIONS

			26LV004T/B-55		26LV004T/B-70			
SYMBOL	PARAMETER		MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tRC	Read Cycle Time (Note 1)		55		70		ns	
tACC	Address to Output Delay			55		70	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay			55		70	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay			25		30	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)		0	25	0	30	ns	$\overline{CE}$=VIL
tOEH	Output Enable	Read	0		0		ns	
	Hold Time	Toggle and $\overline{Data}$ Polling	10		10		ns	
tOH	Address to Output hold		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

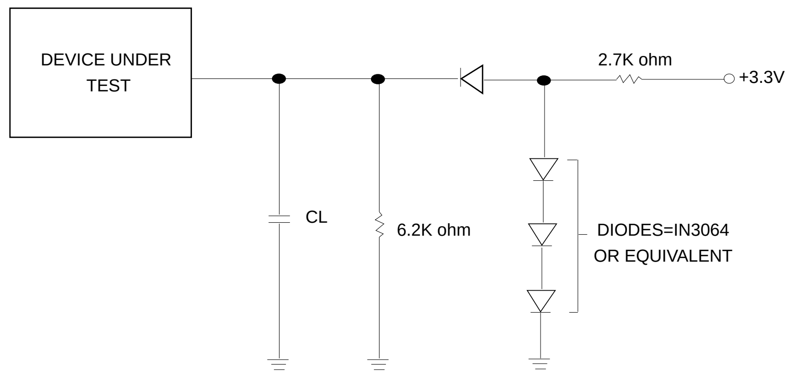
TEST CONDITIONS:

- Input pulse levels: 0V/3.0V.
- Input rise and fall times is equal to or less than 5ns.
- Output load: 1 TTL gate + 100pF (Including scope and jig), for 26LV004T/B-70. 1 TTL gate + 30pF (Including scope and jig) for 26LV004T/B-55.
- Reference levels for measuring timing: 1.5V.

NOTE:

1. Not 100% tested.
2. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

SWITCHING TEST CIRCUITS

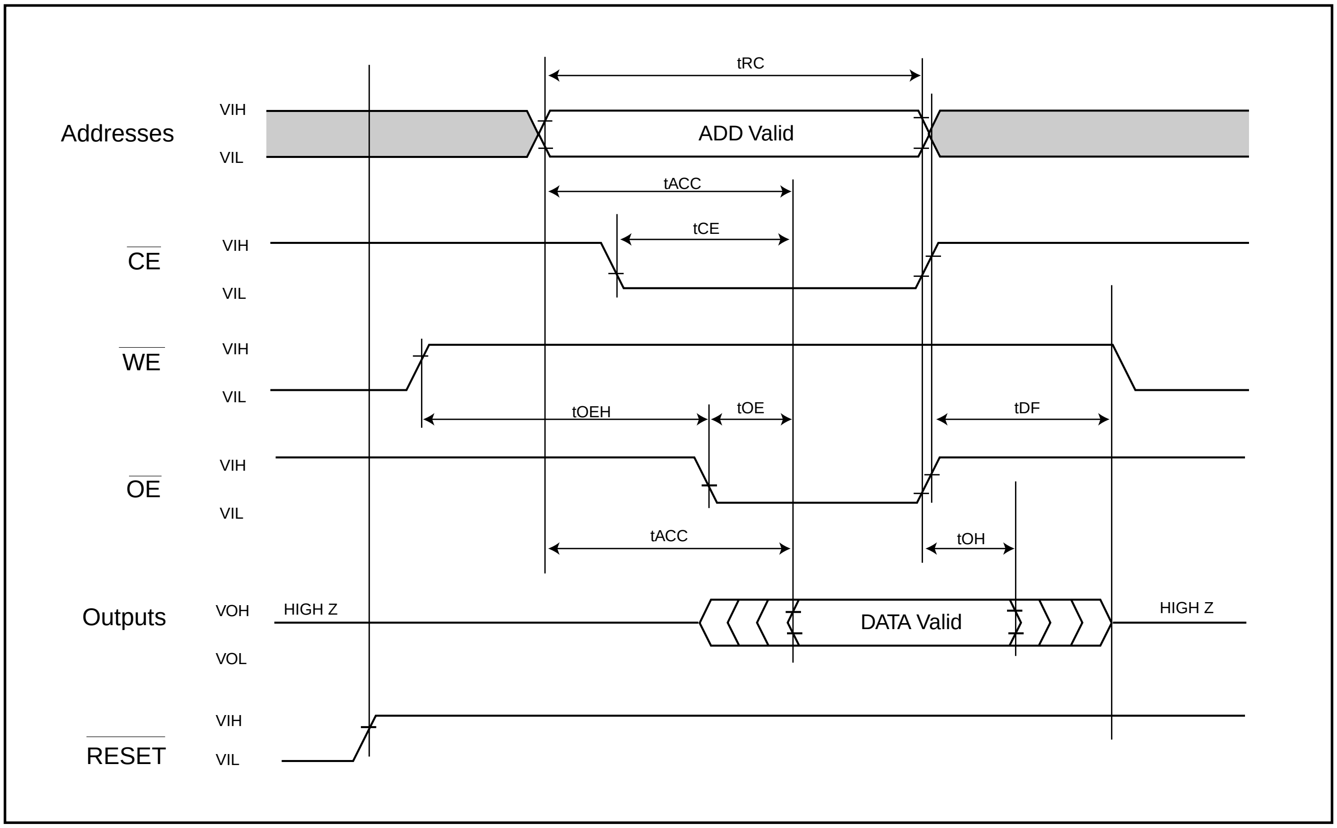


CL=100pF Including jig capacitance for MX26LV004T/B-70 (30pF for MX26LV004T/B-55)

SWITCHING TEST WAVEFORMS

AC TESTING: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are < 5ns.

Figure 1. READ TIMING WAVEFORMS



AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 3.0V~3.6V

Table 10. Erase/Program Operations

		26LV004T/B-55		26LV004T/B-70		
SYMBOL	**PARAMETER**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**
tWC	Write Cycle Time (Note 1)	55		70		ns
tAS	Address Setup Time	0		0		ns
tAH	Address Hold Time	45		45		ns
tDS	Data Setup Time	35		35		ns
tDH	Data Hold Time	0		0		ns
tOES	Output Enable Setup Time	0		0		ns
tGHWL	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)	0		0		ns
tCS	$\overline{CE}$ Setup Time	0		0		ns
tCH	$\overline{CE}$ Hold Time	0		0		ns
tWP	Write Pulse Width	35		35		ns
tWPH	Write Pulse Width High	30		30		ns
tWHWH1	Programming Operation (Note 2)	55 (typ.)		55 (typ.)		us
tWHWH2	Sector Erase Operation (Note 2)	2.4 (typ.)		2.4 (typ.)		sec
tVCS	VCC Setup Time (Note 1)	50		50		us
tRB	Recovery Time from RY/$\overline{BY}$	0		0		ns
tBUSY	Program/Erase Valid to RY/$\overline{BY}$ Delay	90		90		ns
tBAL	Sector Address Load Time		50		50	us

NOTES:

1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

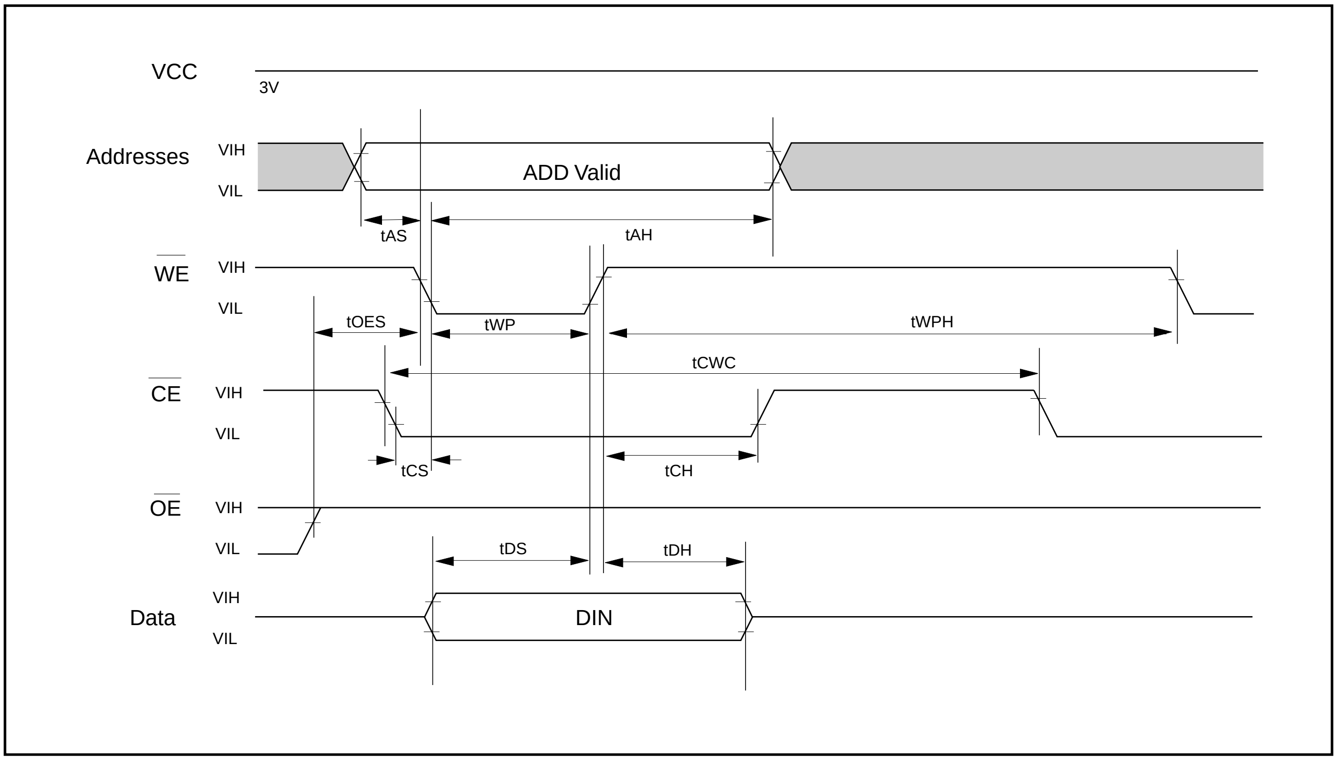
AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 3.0V~3.6V

Table 11. Alternate CE Controlled Erase/Program Operations

		26LV004T/B-55		26LV004T/B-70		
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	UNIT
tWC	Write Cycle Time (Note 1)	55		70		ns
tAS	Address Setup Time	0		0		ns
tAH	Address Hold Time	45		45		ns
tDS	Data Setup Time	35		45		ns
tDH	Data Hold Time	0		0		ns
tOES	Output Enable Setup Time	0		0		ns
tGHEL	Read Recovery Time Before Write	0		0		ns
tWS	WE Setup Time	0		0		ns
tWH	WE Hold Time	0		0		ns
tCP	CE Pulse Width	35		35		ns
tCPH	CE Pulse Width High	30		30		ns
tWHWH1	Programming Operation(note2)	55(Typ.)		55(Typ.)		us
tWHWH2	Sector Erase Operation (note2)	2.4(Typ.)		2.4(Typ.)		sec

NOTE:
1. Not 100% tested.
2. See the "Erase and Programming Performance" section for more information.

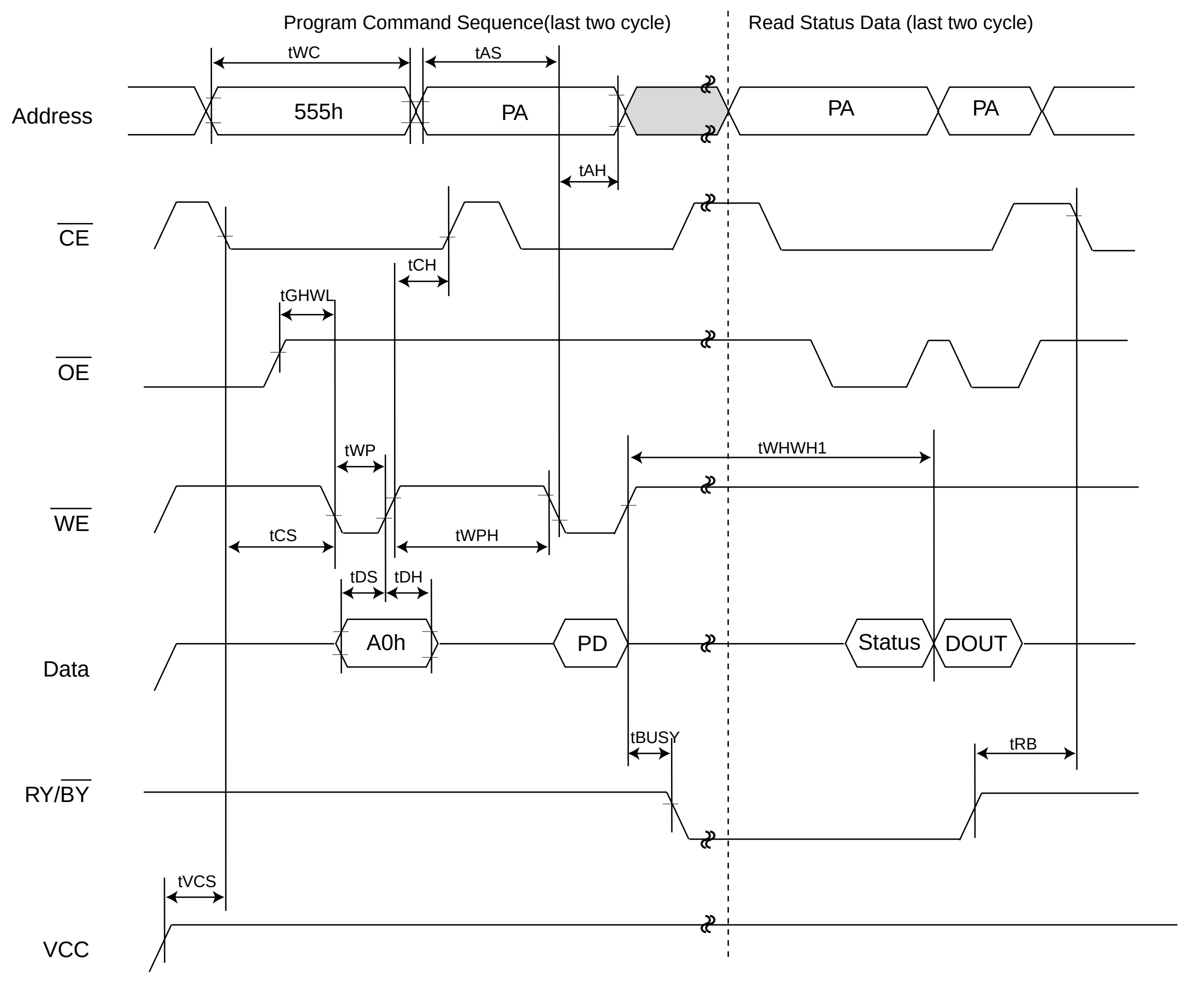
Figure 2. COMMAND WRITE TIMING WAVEFORM



AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional verification by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by $\overline{\text{DATA}}$ polling and toggle bit checking after automatic programming starts. Device outputs $\overline{\text{DATA}}$ during programming and DATA after programming on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{\text{DATA}}$ polling, timing waveform)

Figure 3. AUTOMATIC PROGRAMMING TIMING WAVEFORM



NOTES:
1.PA=Program Address, PD=Program Data, DOUT is the true data the program address

Figure 4. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART

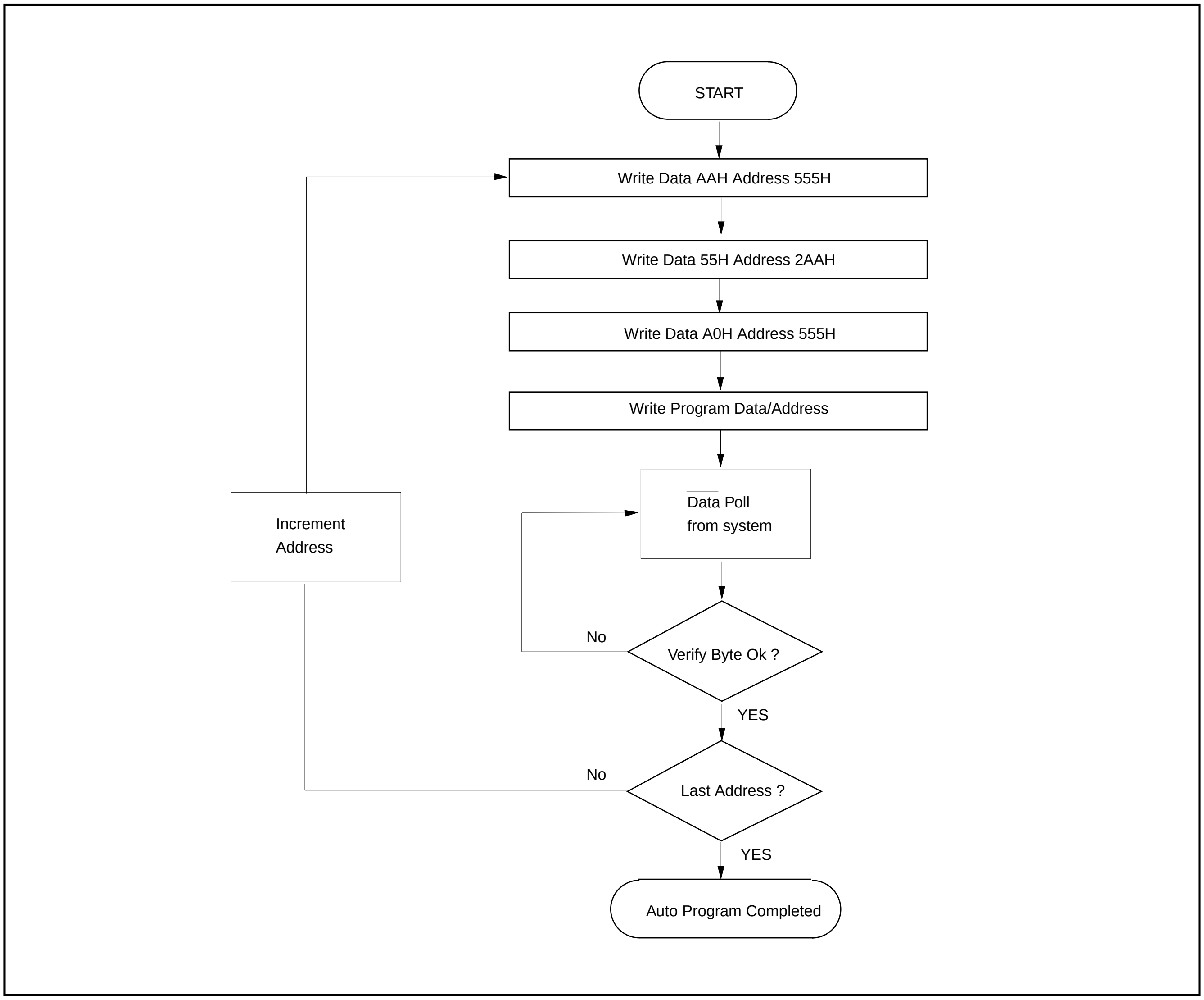
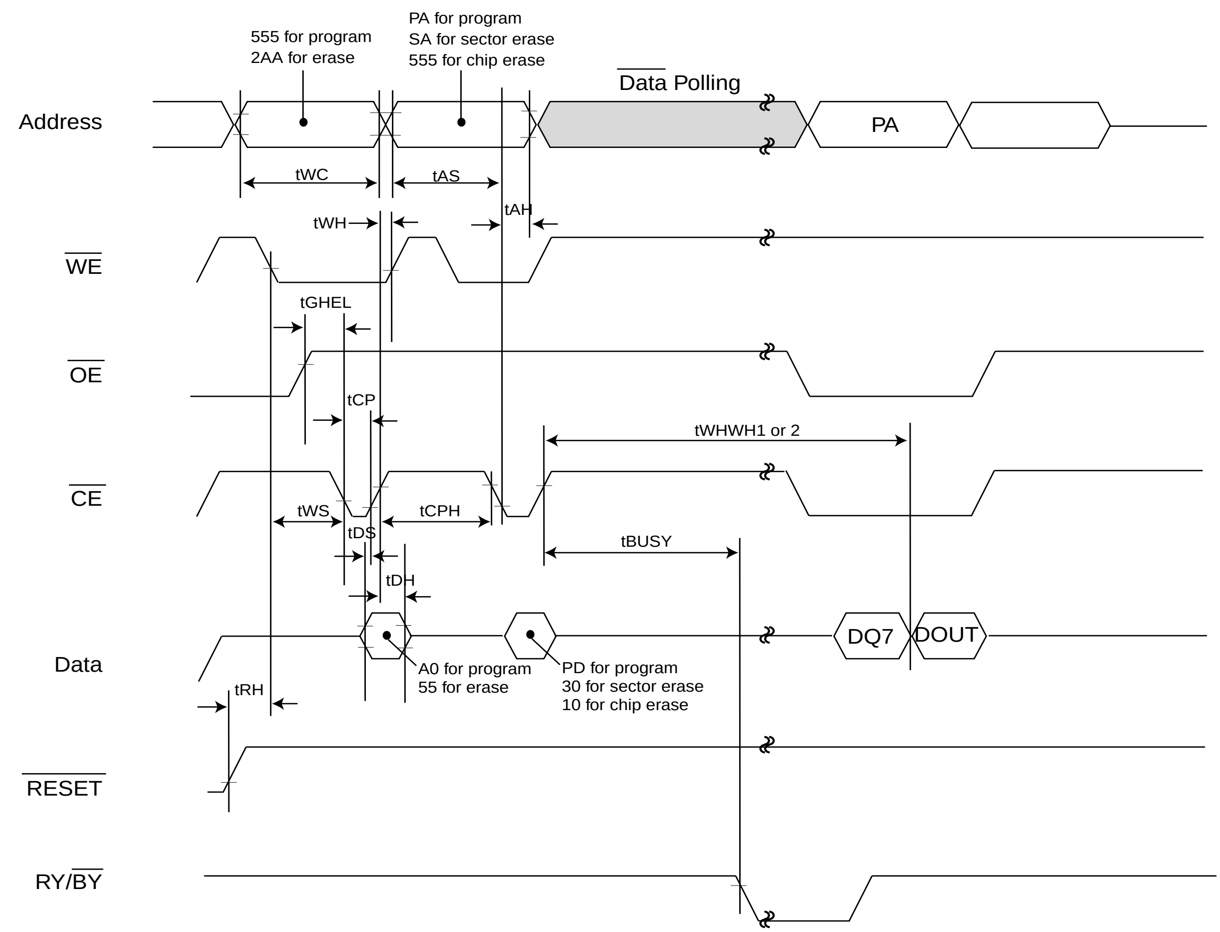


Figure 5. $\overline{CE}$ CONTROLLED PROGRAM TIMING WAVEFORM



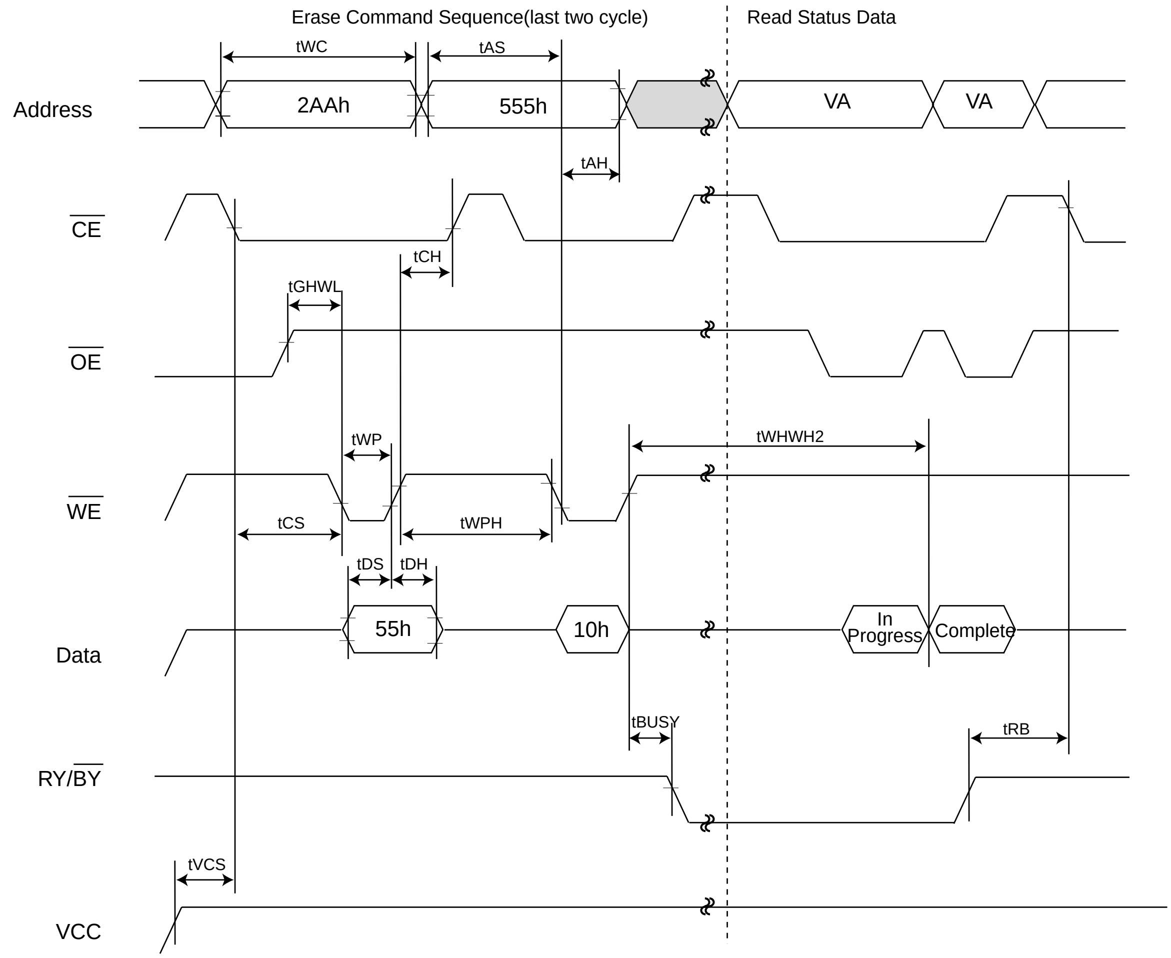
NOTES:

1.PA=Program Address, PD=Program Data, DOUT=Data Out, DQ7=complement of data written to device.
2.Figure indicates the last two bus cycles of the command sequence.

AUTOMATIC CHIP ERASE TIMING WAVEFORM

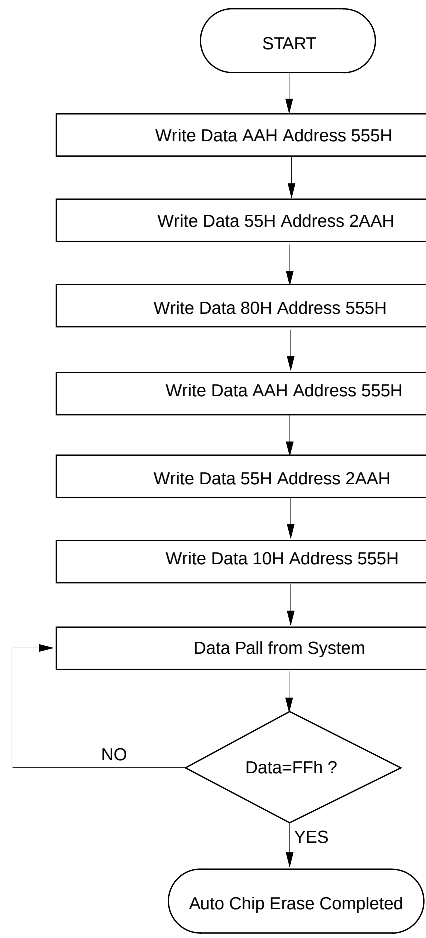
All data in chip are erased. External erase verification is not required because data is verified automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

Figure 6. AUTOMATIC CHIP ERASE TIMING WAVEFORM



NOTES:
SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

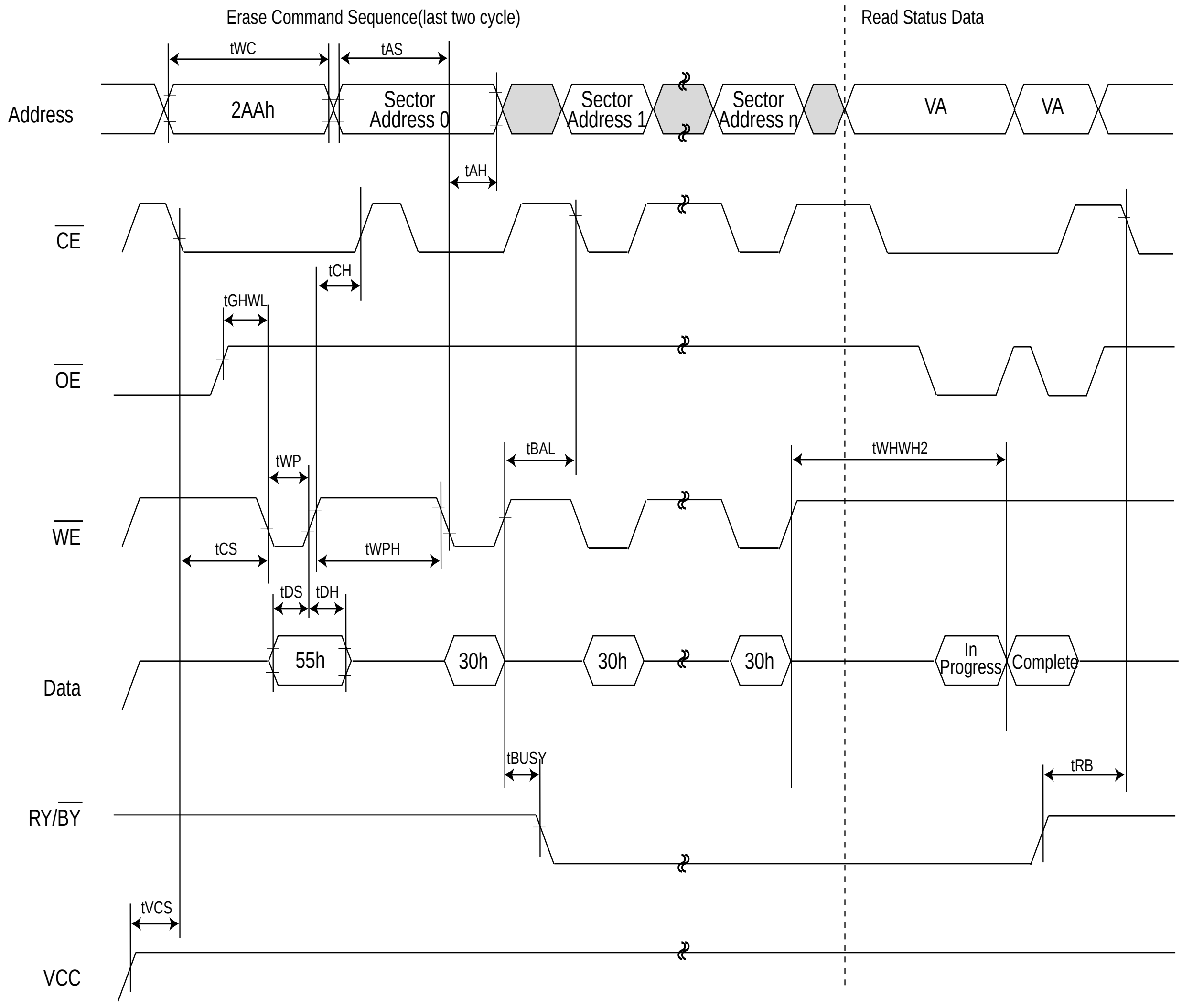
Figure 7. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART



AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Sector indicated by A12 to A18 are erased. External erase verify is not required because data are verified automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

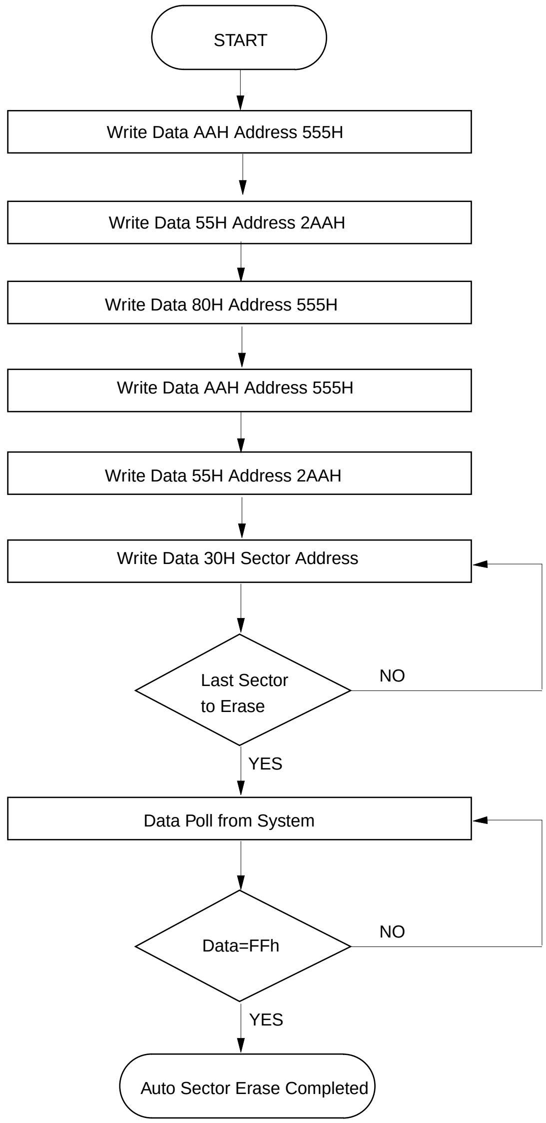
Figure 8. AUTOMATIC SECTOR ERASE TIMING WAVEFORM



NOTES:

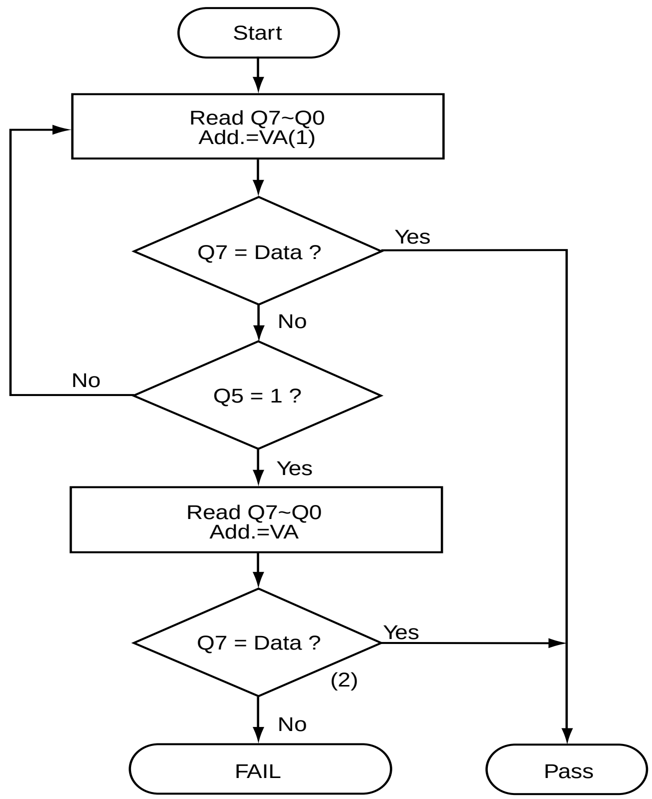
SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

Figure 9. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART



WRITE OPERATION STATUS

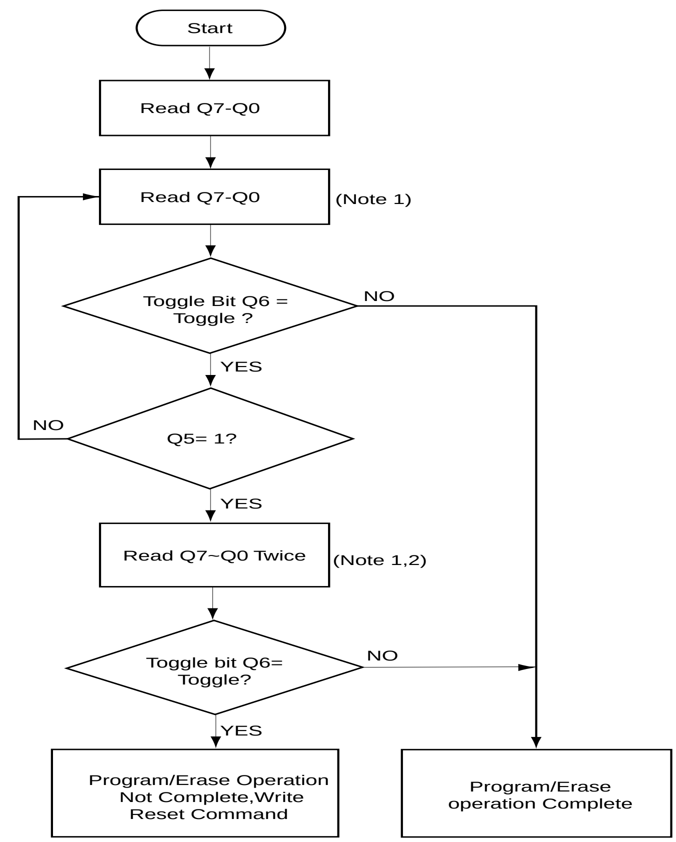
Figure 10. $\overline{\text{DATA}}$ POLLING ALGORITHM



NOTE : 1.VA=Valid address for programming

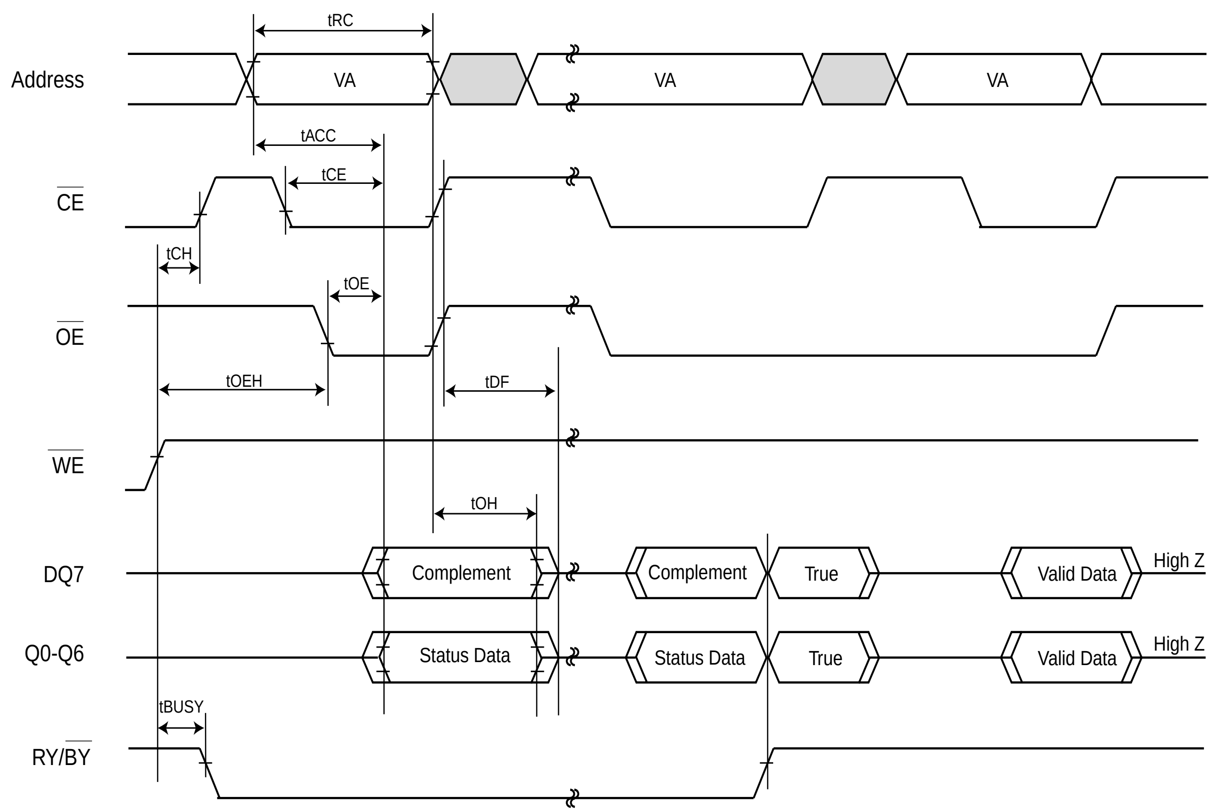
2.Q7 should be re-checked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 11. TOGGLE BIT ALGORITHM



Note:1.Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 change to "1".

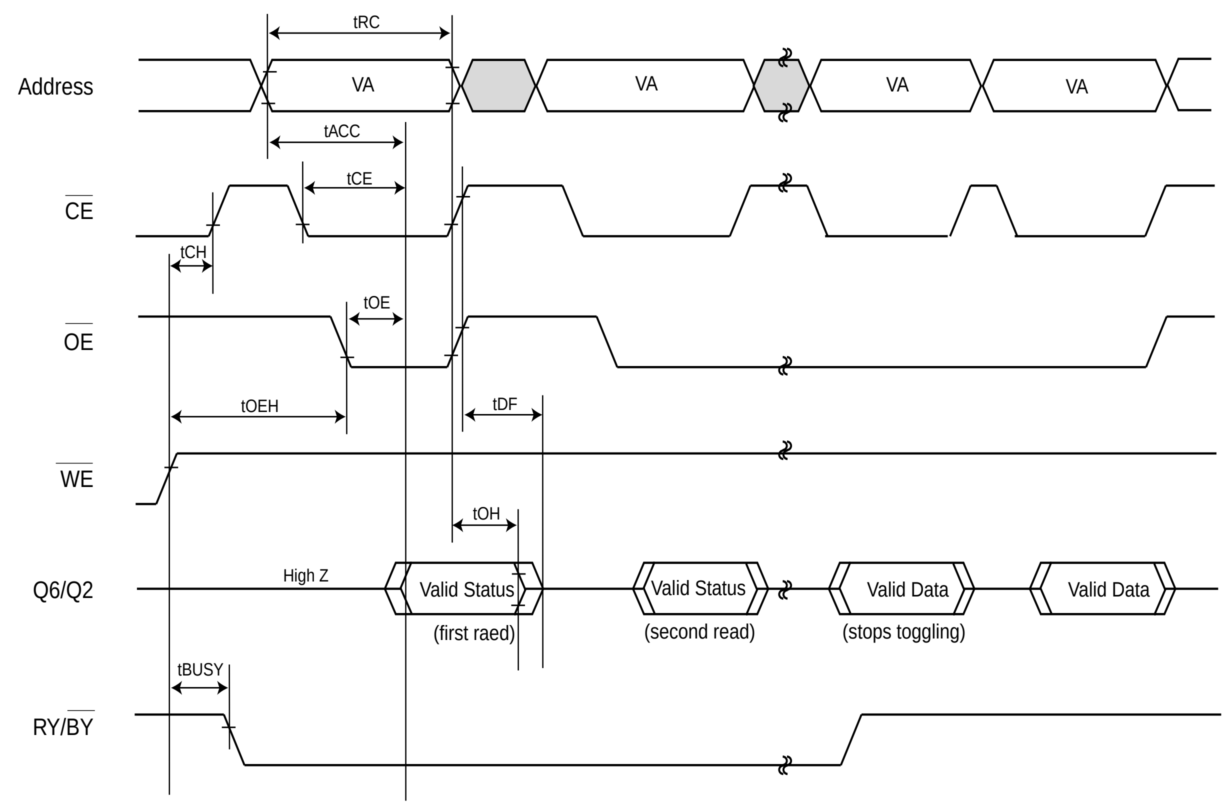
Figure 12. $\overline{DATA}$ POLLING TIMINGS (During Automatic Algorithms)



NOTES:

1. VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data read cycle.
2. $\overline{CE}$ must be toggled when $\overline{DATA}$ polling.

Figure 13. TOGGLE BIT TIMINGS (During Automatic Algorithms)



NOTES:

1. VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.
2. CE must be toggled when toggle bit toggling.

Table 11. AC CHARACTERISTICS

Parameter Std	Description	Test Setup	All Speed Options	Unit
tREADY1	RESET PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	RESET PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP	RESET Pulse Width (During Automatic Algorithms)	MIN	500	ns
tRH	RESET High Time Before Read(See Note)	MIN	50	ns
tRB	RY/BY Recovery Time(to CE, OE go low)	MIN	0	ns

Note:Not 100% tested

Figure 14. RESET TIMING WAVEFORM

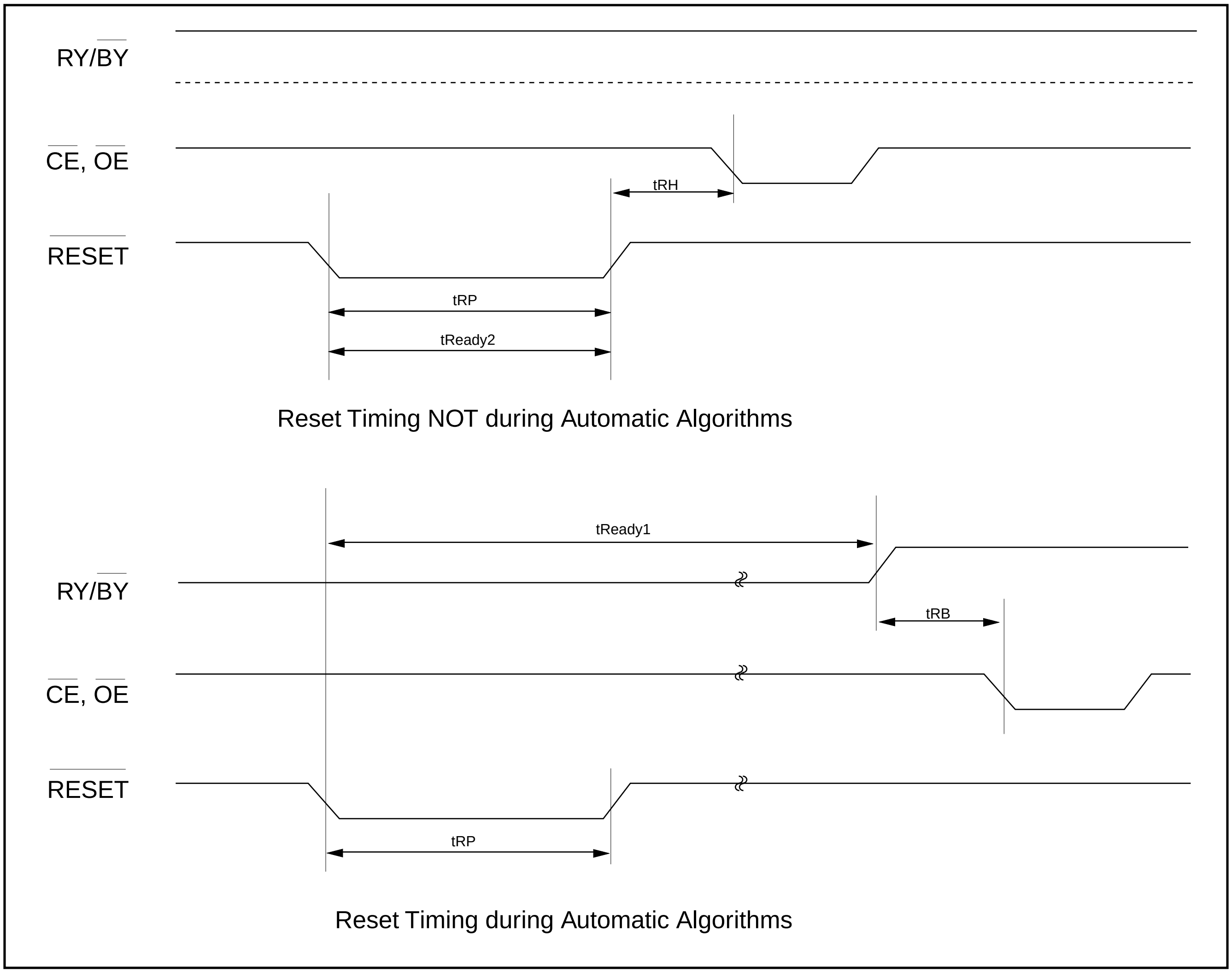
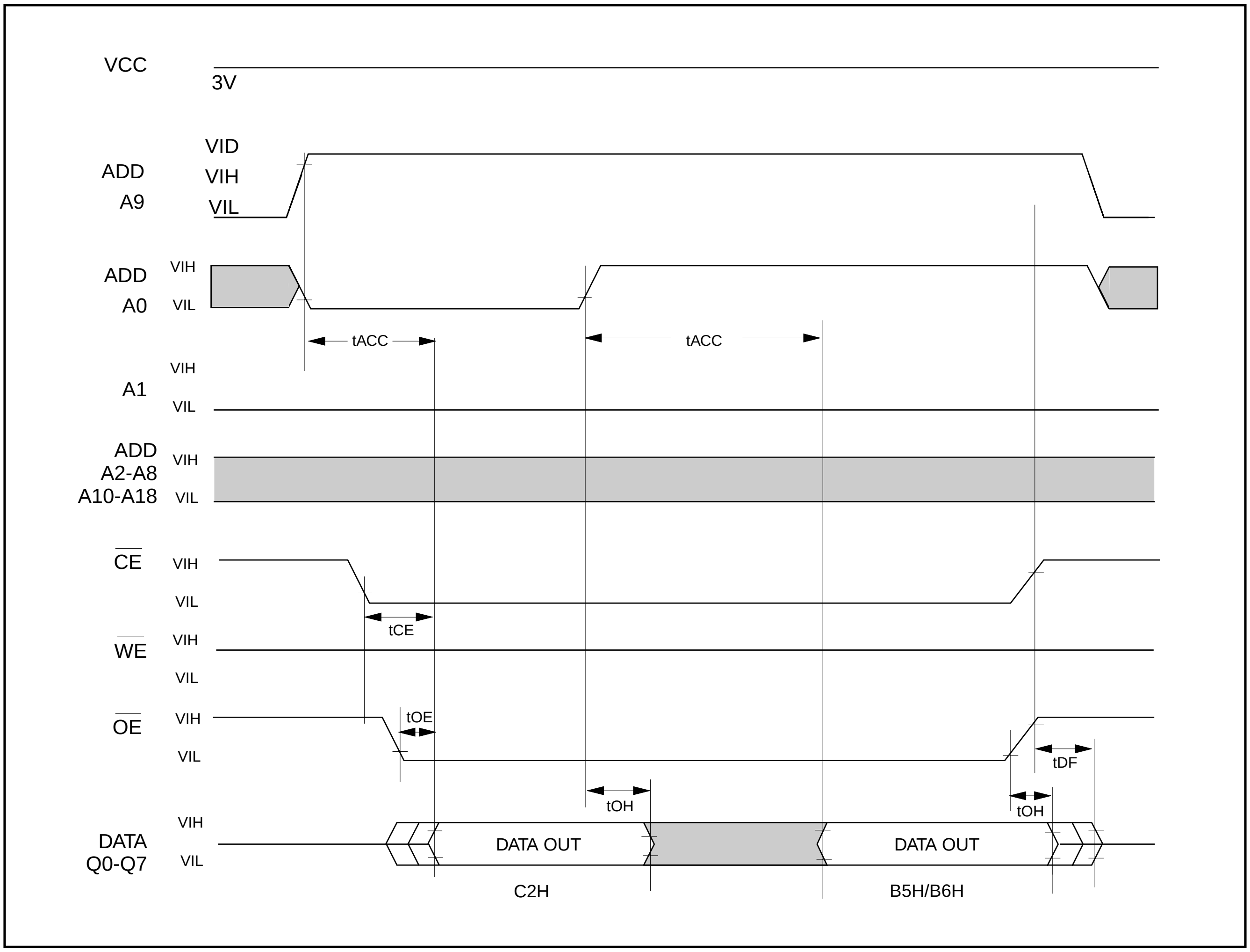


Figure 15. ID CODE READ TIMING WAVEFORM



ERASE AND PROGRAMMING PERFORMANCE(1)

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.(3)	
Sector Erase Time		2.4	15	sec
Chip Erase Time		20	80	sec
Byte Programming Time		55	220	us
Chip Programming Time		18	36	sec
Erase/Program Cycles	2K (6)			Cycles

Note:
1. Not 100% tested.
2. Typical program and erase times assume the following conditions : 25° C, 3.3V VCC. Programming spec. assume that all bits are programmed to checkerboard pattern.
3. Maximum values are measured at VCC=3.0V, worst case temperature. Maximum values are up to including 2K program/erase cycles.
4. System-level overhead is the time required to execute the command sequences for the all program command.
5. Excludes 00H programming prior to erasure. (In the pre-programming step of the embedded erase algorithm, all bits are programmed to 00H before erasure)
6. Min. erase/program cycles is under : 3.3V VCC, 25° C, checkerboard pattern conditions, and without baking process.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on ACC, $\overline{OE}$, $\overline{RESET}$, A9	-1.0V	12V
Input Voltage with respect to GND on all power pins, Address pins, $\overline{CE}$ and $\overline{WE}$	-1.0V	VCC + 1.0V
Input Voltage with respect to GND on all I/O pins	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

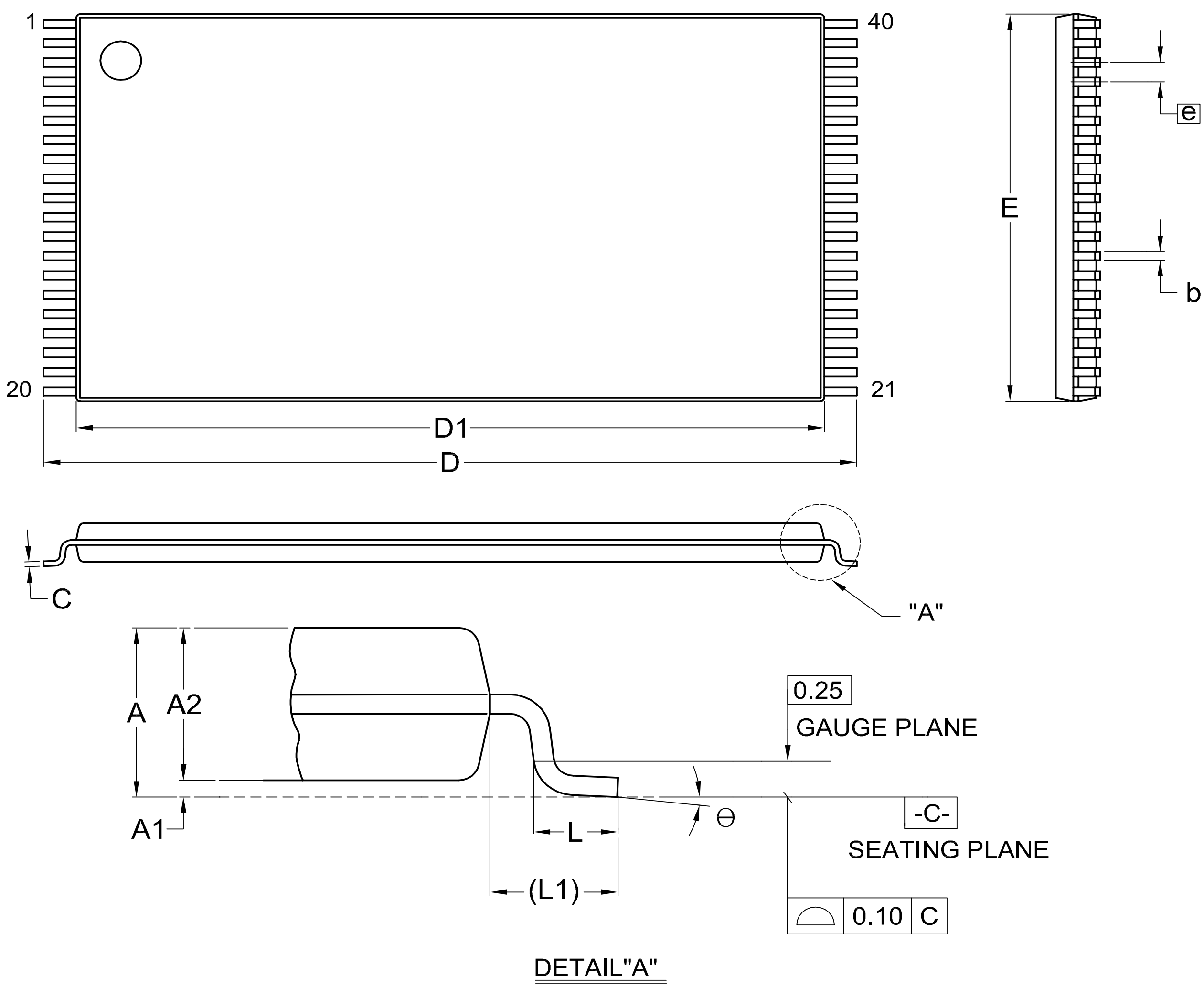
ORDERING INFORMATION

PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX26LV004TTC-55	55	30	100	40 Pin TSOP
MX26LV004TTC-70	70	30	100	40 Pin TSOP
MX26LV004BTC-55	55	30	100	40 Pin TSOP
MX26LV004BTC-70	70	30	100	40 Pin TSOP
MX26LV004TQC-55	55	30	100	32 Pin PLCC
MX26LV004TQC-70	70	30	100	32 Pin PLCC
MX26LV004BQC-55	55	30	100	32 Pin PLCC
MX26LV004BQC-70	70	30	100	32 Pin PLCC

PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 40L (10X20mm)

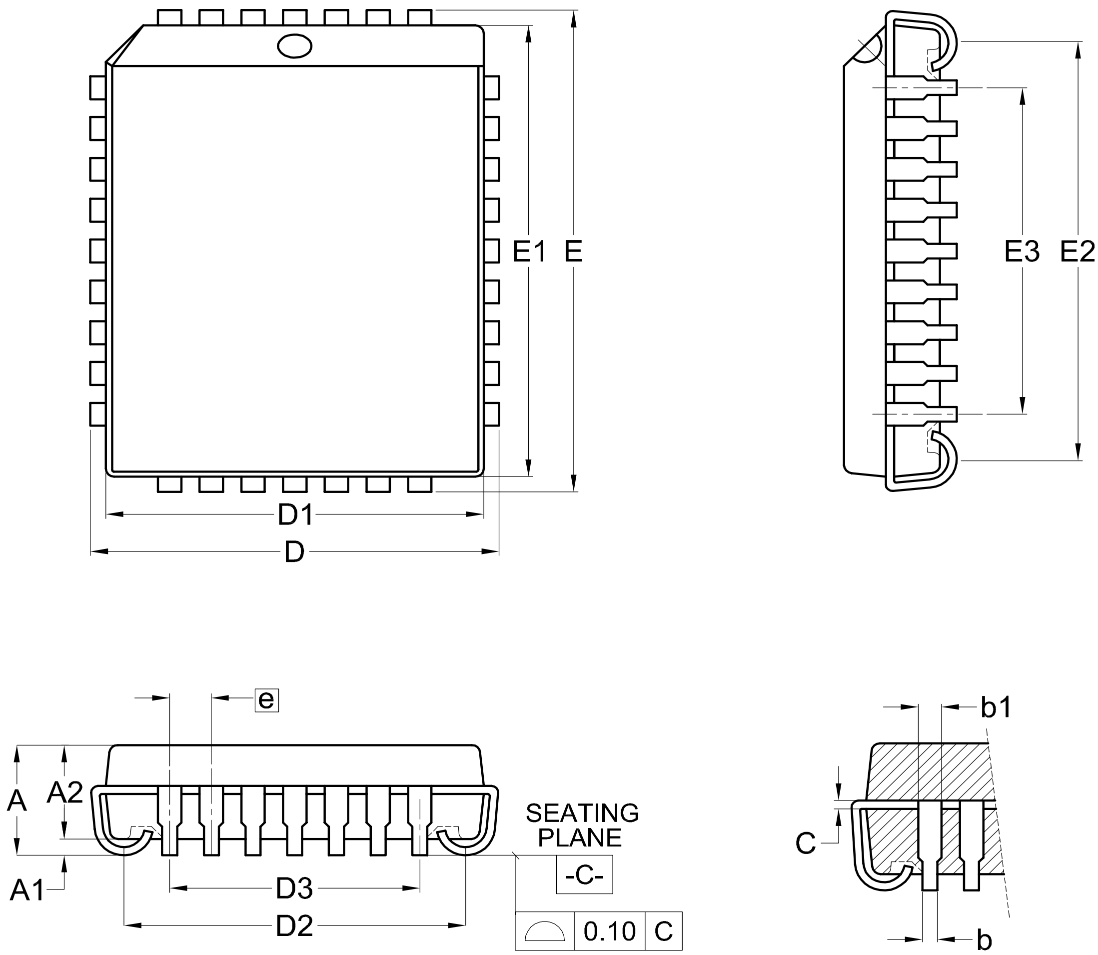


Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	9.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	10.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	10.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.390		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.394	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.398		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1606	6	MO-142			12-01-'03

Title: **Package Outline for 32L PLCC**



Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	---	0.38	2.69	0.38	0.61	0.20	12.32	11.36	10.11		14.86	13.98	12.65		
	Nom.	---	0.58	2.79	0.46	0.71	0.25	12.45	11.43	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.81	2.89	0.54	0.81	0.30	12.58	11.50	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.447	0.398		0.585	0.550	0.498		
	Nom.	---	0.023	0.110	0.018	0.028	0.010	0.490	0.450	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.032	0.114	0.021	0.032	0.012	0.495	0.453	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	7	MS-016			12-10-'03

REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Modified the erase/program cycling to 2K cycles	P1,48	JUN/24/2004
	2. Removed data retention table	P48	
0.02	1. Modified the erase/program cycling to 2K cycles in General Description	P1	JUL/12/2004
	2. Removed Protect/unprotected information	All	
	3. To added 32-PLCC package information	P1,2,39,41	

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