



# MX26C512A

## 512K-BIT [64K x 8] CMOS MULTIPLE-TIME-PROGRAMMABLE EPROM

### FEATURES

- 64K x 8 organization
- +5V operating power supply
- +12.75V program/erase voltage
- Electric erase instead of UV light erase
- Fast access time: 70/90/100/120/150 ns
- Totally static operation
- Completely TTL compatible

- Operating current: 30mA
- Standby current: 100uA
- 100 minimum erase/program cycles
- Package type:
  - 28 pin plastic DIP
  - 28 pin SOP
  - 32 pin PLCC
  - 28 pin TSOP(I)

**PATENTED TECHNOLOGY**

### GENERAL DESCRIPTION

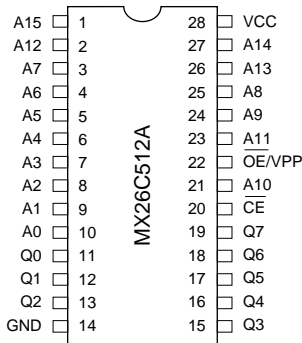
The MX26C512A is a 12.75V/5V, 512K-bit, MTP EPROM™ (Multiple Time Programmable Read Only Memory). It is organized as 64K words by 8 bits per word, operates from a + 5 volt supply, has a static standby mode, and features fast single address location programming. It is designed to be reprogrammed and erased by an EPROM programmer or on-board. All programming/erasing signals are TTL levels, requiring a single pulse.

The MX26C512A supports an intelligent quick pulse programming algorithm which can result in a programming time of less than 30 seconds.

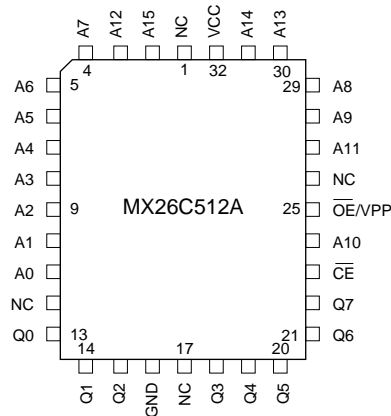
This MTP EPROM™ is packaged in industry standard 28 pin dual-in-line packages, 32 pin PLCC packages or 28 pin TSOP packages and 28 pin SOP packages.

### PIN CONFIGURATIONS

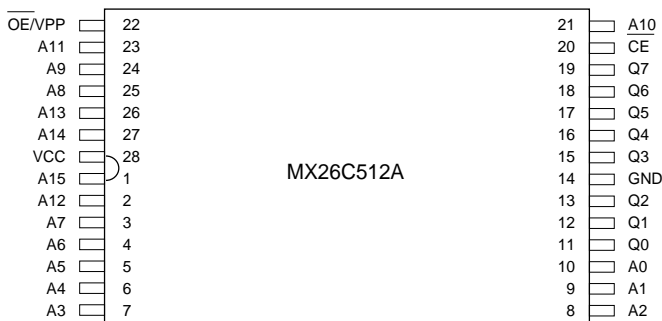
#### PDIP/SOP



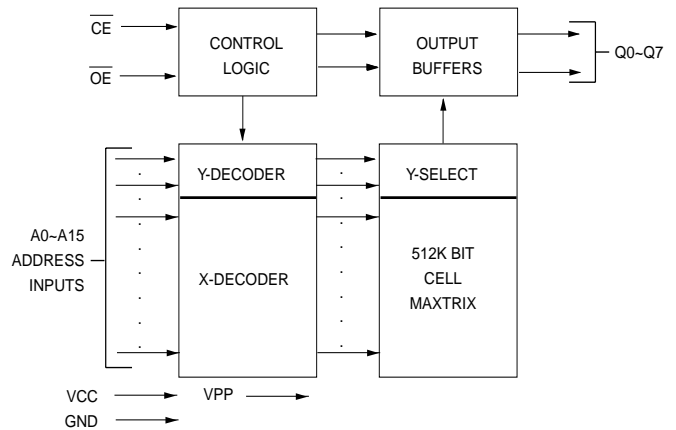
#### PLCC



#### TSOP



### BLOCK DIAGRAM



### PIN DESCRIPTION

| SYMBOL | PIN NAME               |
|--------|------------------------|
| A0~A15 | Address Input          |
| Q0~Q7  | Data Input/Output      |
| CE     | Chip Enable Input      |
| OE     | Output Enable Input    |
| VPP    | Program Supply Voltage |
| NC     | No Internal Connection |
| VCC    | Power Supply Pin (+5V) |
| GND    | Ground Pin             |

## FUNCTIONAL DESCRIPTION

When the MX26C512A is delivered, or it is erased, the chip has all 512K bits in the "ONE", or HIGH state. "ZEROS" are loaded into the MX26C512 through the procedure of programming.

## PROGRAMMING MODE

### PROGRAMMING ALGORITHM

The MX26C512A is programmed by an EPROM programmer or on-board. The device is set up in the programming mode when the programming voltage  $\overline{OE}/VPP = 12.75V$  is applied, with  $VCC = 5V$  (Algorithm shown in Figure 1). Programming is achieved by applying a single TTL low level 25us pulse to the  $\overline{CE}$  input after addresses and data lines are stable. If the data is not verified, additional pulses are applied for a maximum of 20 pulses. After the data is verified, one 25us pulse is applied to overprogram the byte so that program margin is assured. This process is repeated while sequencing through each address of the device. When programming is completed, the data at all the addresses are verified at  $VCC = 5V \pm 10\%$ .

The VCC supply of the MXIC On-Board Programming Algorithm is designed to be  $5V \pm 10\%$  particularly to facilitate the programming operation under the on-board application environment. But it can also be implemented in an industrial-standard EPROM programmer.

### COMPATIBILITY WITH MX27C512 FAST PROGRAMMING ALGORITHM

Besides the On-Board Programming Algorithm, the Fast Programming Algorithm of MX27C512 also applies to MX26C512A. MXIC Fast Algorithm is the conventional EPROM programming algorithm and is available in industrial-standard EPROM programmers. A user of industrial-standard EPROM programmer can choose either of the algorithms base on his preference.

The device is set up in the fast programming mode when the programming voltage  $\overline{OE}/VPP = 12.75V$  is applied, with  $VCC = 6.25V$ , (Algorithm is shown in Figure 2). The programming is achieved by applying a single TTL low level 25~100us pulse to the  $\overline{CE}$  input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at  $VCC = 5V \pm 10\%$ .

## ERASE MODE

The MX26C512A is erased by EPROM programmer or in-system. The device is set up in erase mode when  $A9 = \overline{OE}/VPP = 12.75V$  are applied, with  $VCC = 5V$ . (Algorithm is shown in Figure 3). The erase time is around 1sec. If the erase is not verified, an additional erase processes will be repeated for a maximum of 200 times.

## PROGRAM INHIBIT MODE

Programming of multiple MX26C512A in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for  $\overline{CE}$  and  $\overline{OE}$ , all like inputs of the parallel MX26C512 may be common. A TTL low-level program pulse applied to an MX26C512A  $\overline{CE}$  input with  $\overline{OE}/VPP = 12.75 \pm 0.25V$  will program that MX26C512A. A high-level  $\overline{CE}$  input inhibits the other MX26C512A from being programmed.

## PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with  $\overline{OE}/VPP$  and  $\overline{CE}$ , at  $VIL$ . Data should be verified tDV after the falling edge of  $\overline{CE}$ .

## ERASE VERIFY MODE

Verification should be performed on the erased chip to determine that whole chip(all bits) was correctly erased. Verification should be performed with  $\overline{OE}/VPP$  and  $\overline{CE}$  at  $VIL$  and  $VCC = 5V$ .

## AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from a MTP that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the  $25^{\circ}C \pm 5^{\circ}C$  ambient temperature range that is required when programming the MX26C512A.

To activate this mode, the programming equipment must force 12.75V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from  $VIL$  to  $VIH$ . All

other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX26C512A, these two identifier bytes are given in the Mode Select Table. All identifiers for the manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

### READ MODE

The MX26C512A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable (CE) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from CE to output (tCE). Data is available at the outputs tOE after the falling edge of OE, assuming that CE has been LOW and addresses have been stable for at least tACC - tOE.

### STANDBY MODE

The MX26C512A has a CMOS standby mode which reduces the maximum VCC current to 100 uA. It is placed in CMOS standby when CE is at VCC ± 0.3 V. The MX26C512A also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when CE is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the OE input.

### TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that  $\overline{\text{CE}}$  be decoded and used as the primary device-selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular

memory device.

### SYSTEM CONSIDERATIONS

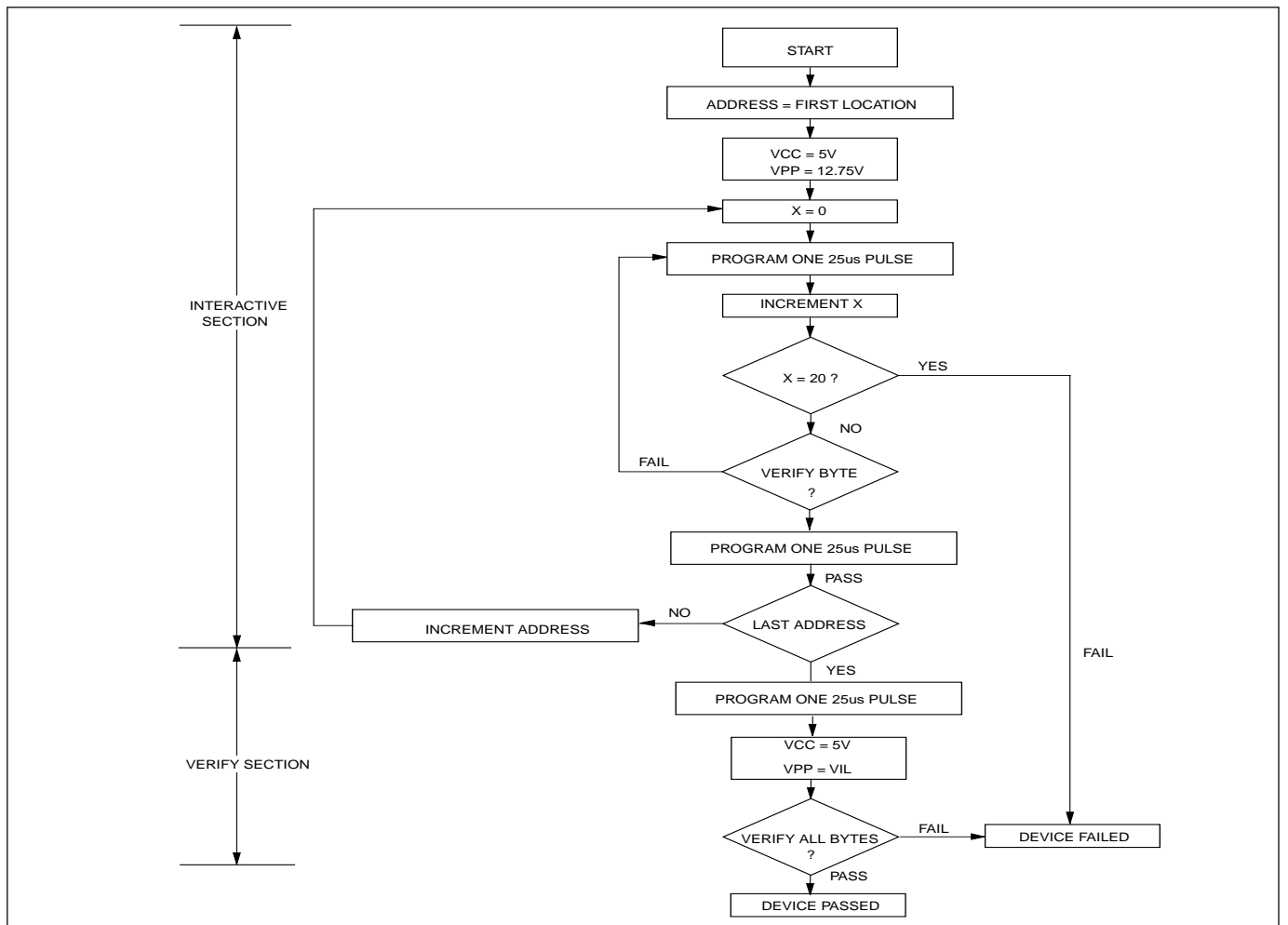
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 uF bulk electrolytic capacitor should be used between VCC and GND for each of the eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## MODE SELECT TABLE

| MODE                | PINS            |                     |     |     | OUTPUTS |
|---------------------|-----------------|---------------------|-----|-----|---------|
|                     | $\overline{CE}$ | $\overline{OE/VPP}$ | A0  | A9  |         |
| Read                | VIL             | VIL                 | X   | X   | DOUT    |
| Output Disable      | VIL             | VIH                 | X   | X   | High Z  |
| Standby (TTL)       | VIH             | X                   | X   | X   | High Z  |
| Standby (CMOS)      | VCC             | X                   | X   | X   | High Z  |
| Program             | VIL             | VPP                 | X   | X   | DIN     |
| Program Verify      | VIL             | VIL                 | X   | X   | DOUT    |
| Erase               | VIL             | VPP                 | X   | VPP | HIGH Z  |
| Erase Verify        | VIL             | VIL                 | X   | X   | DOUT    |
| Program Inhibit     | VIH             | X                   | X   | X   | High Z  |
| Manufacturer Code   | VIL             | VIL                 | VIL | VH  | C2H     |
| Device Code(26C512) | VIL             | VIL                 | VIH | VH  | D1H     |

- NOTES:**
- VH = 12.0V  $\pm$  0.5V
  - X = Either VIH or VIL(For auto select)
  - A1 - A8 = A10 - A15 = VIL(For auto select)
  - See DC Programming Characteristics for VPP voltage during programming.

**FIGURE 1. PROGRAMMING FLOW CHART**



**FIGURE 2. COMPATIBILITY WITH MX27C512 FAST PROGRAMMING FLOW CHART**

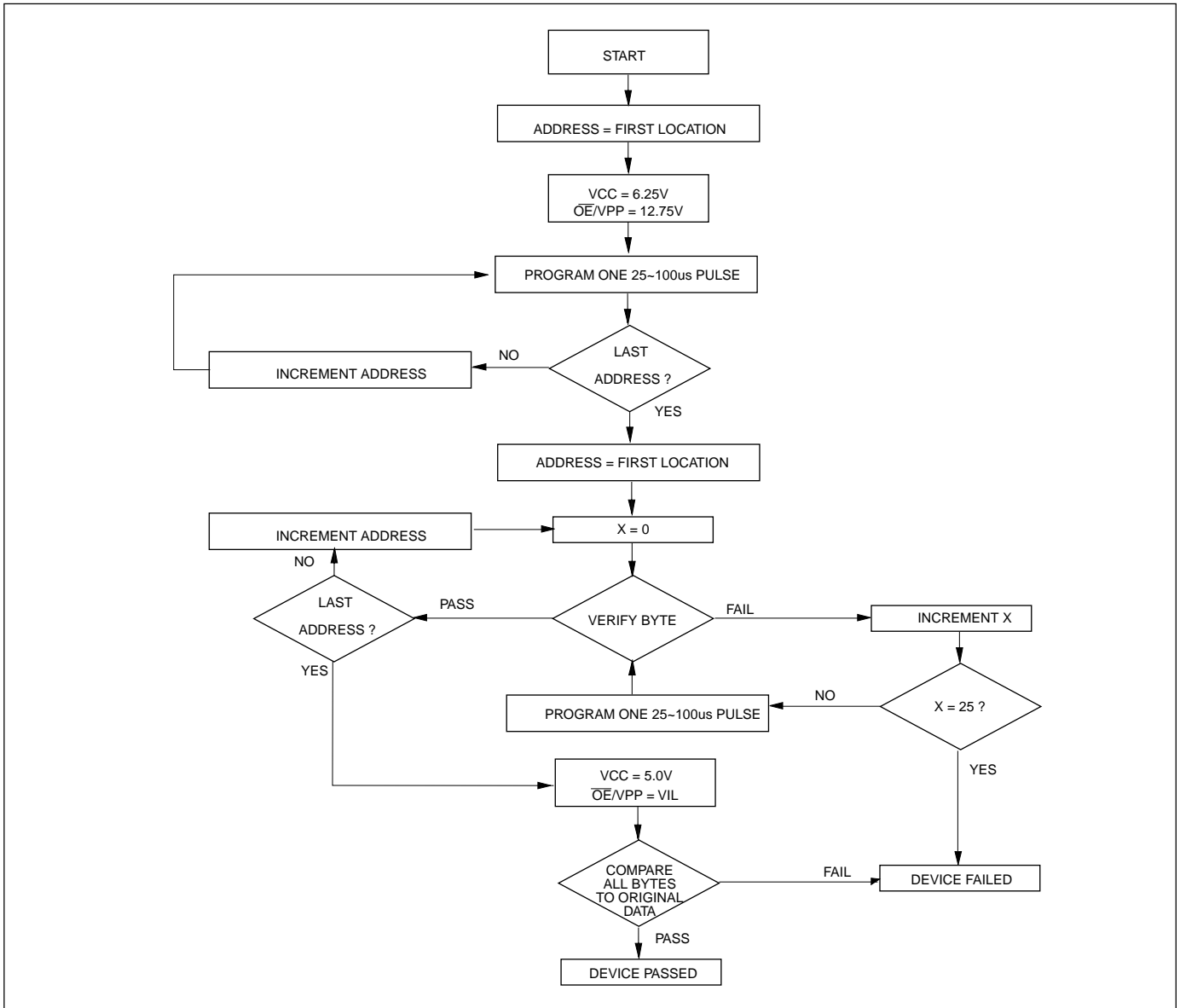
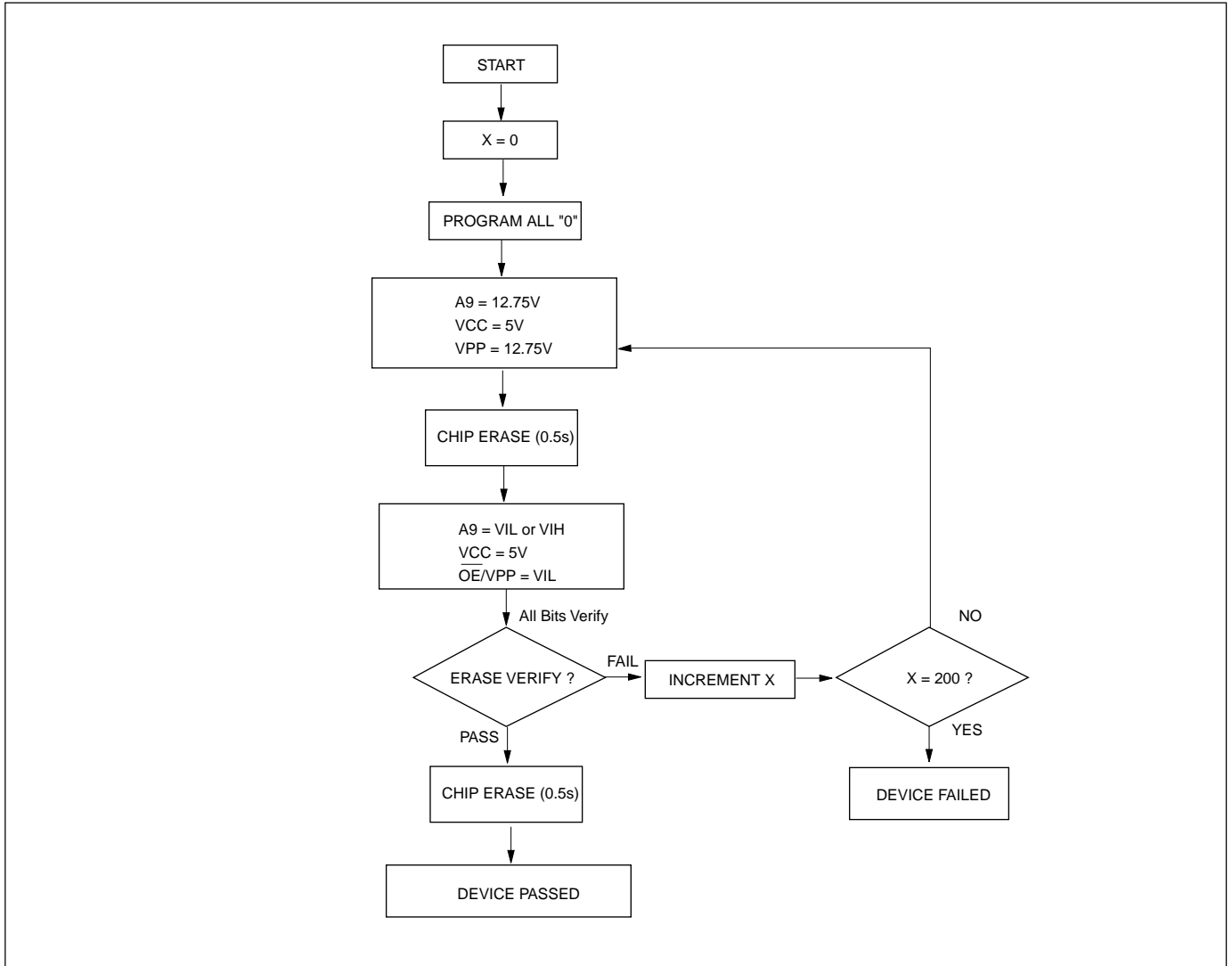
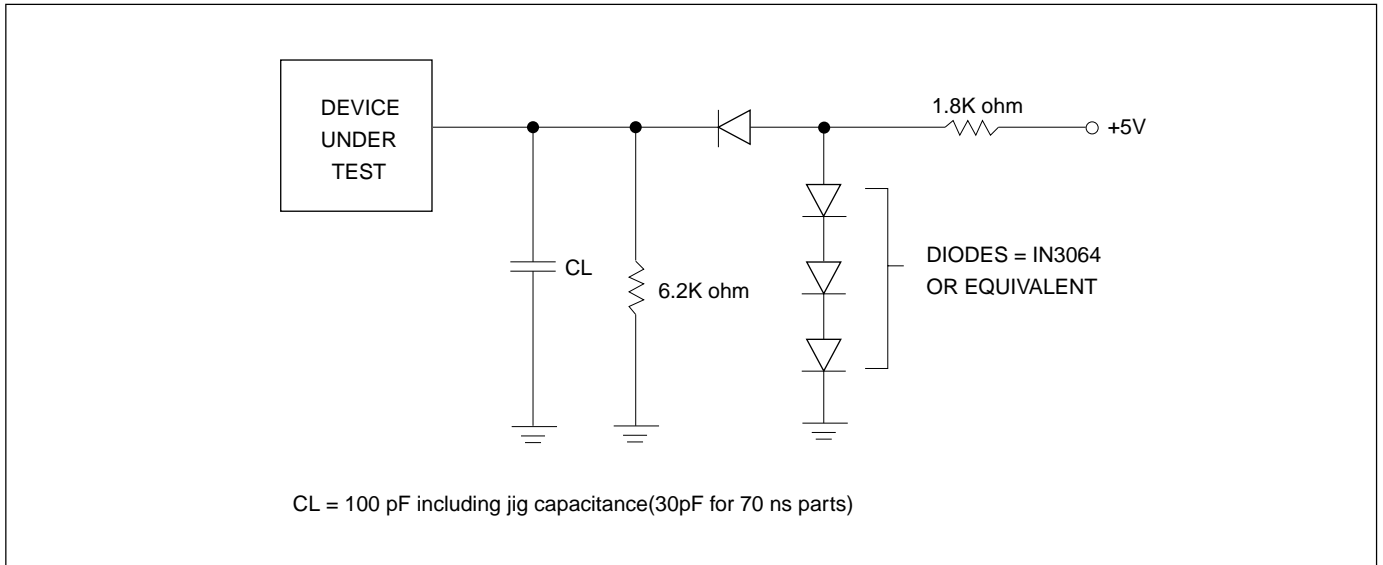


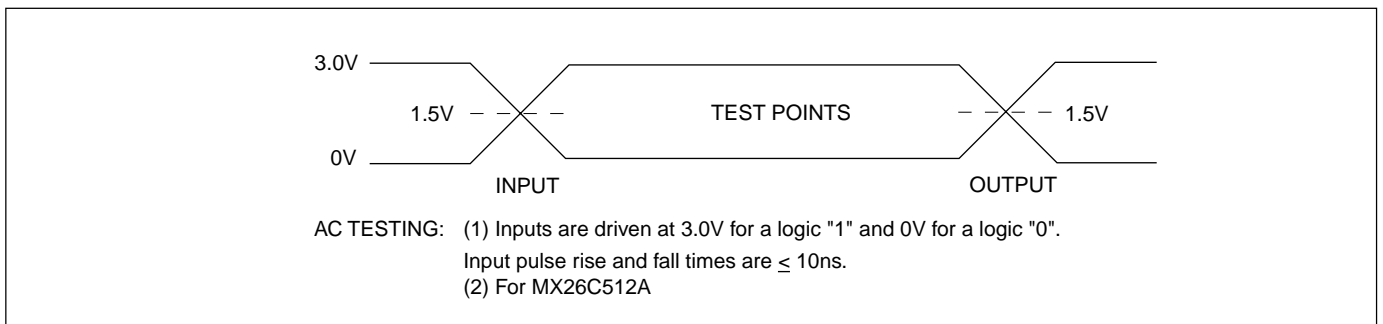
FIGURE 3. ERASING MODE FLOW CHART



## SWITCHING TEST CIRCUITS



## SWITCHING TEST WAVEFORMS





## ABSOLUTE MAXIMUM RATINGS

| RATING                        | VALUE               |
|-------------------------------|---------------------|
| Ambient Operating Temperature | 0°C to 70°C         |
| Storage Temperature           | -65°C to 125°C      |
| Applied Input Voltage         | -0.5V to 7.0V       |
| Applied Output Voltage        | -0.5V to VCC + 0.5V |
| VCC to Ground Potential       | -0.5V to 7.0V       |
| A9 & Vpp                      | -0.5V to 13.5V      |

### NOTICE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

### NOTICE:

Specifications contained within the following tables are subject to change.

## DC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

| SYMBOL | PARAMETER              | MIN. | MAX.      | UNIT | CONDITIONS                                |
|--------|------------------------|------|-----------|------|---|
| VOH    | Output High Voltage    | 2.4  |           | V    | IOH = -0.4mA                              |
| VOL    | Output Low Voltage     |      | 0.4       | V    | IOL = 2.1mA                               |
| VIH    | Input High Voltage     | 2.0  | VCC + 0.5 | V    |   |
| VIL    | Input Low Voltage      | -0.3 | 0.8       | V    |   |
| ILI    | Input Leakage Current  | -10  | 10        | uA   | VIN = 0 to 5.5V                           |
| ILO    | Output Leakage Current | -10  | 10        | uA   | VOUT = 0 to 5.5V                          |
| ICC3   | VCC Power-Down Current |      | 100       | uA   | $\overline{CE} = VCC \pm 0.3V$            |
| ICC2   | VCC Standby Current    |      | 1.5       | mA   | $\overline{CE} = VIH$                     |
| ICC1   | VCC Active Current     |      | 30        | mA   | $\overline{CE} = VIL, f=5MHz, Iout = 0mA$ |

## CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

| SYMBOL | PARAMETER          | TYP. | MAX. | UNIT | CONDITIONS |
|--------|--------------------|------|------|------|------------|
| CIN    | Input Capacitance  | 8    | 8    | pF   | VIN = 0V   |
| COUT   | Output Capacitance | 8    | 12   | pF   | VOUT = 0V  |
| CVPP   | VPP Capacitance    | 18   | 25   | pF   | VPP = 0V   |





## AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

| SYMBOL | PARAMETER  | 26C512A |      | 26C512A |      | UNIT | CONDITIONS                            |
|--------|--|---------|------|---------|------|------|---------------------------------------|
|        |  | -70     |      | -90     |      |      |                                       |
|        |  | MIN.    | MAX. | MIN.    | MAX. |      |                                       |
| tACC   | Address to Output Delay  |         | 70   |         | 90   | ns   | $\overline{CE} = \overline{OE} = VIL$ |
| tCE    | Chip Enable to Output Delay  |         | 70   |         | 90   | ns   | $\overline{OE} = VIL$                 |
| tOE    | Output Enable to Output Delay  |         | 35   |         | 40   | ns   | $\overline{CE} = VIL$                 |
| tDF    | $\overline{OE}$ High to Output Float,<br>or $\overline{CE}$ High to Output Float | 0       | 20   | 0       | 25   | ns   |                                       |
| tOH    | Output Hold from Address,<br>CE or OE which ever occurred first                  | 0       |      | 0       |      | ns   |                                       |

| SYMBOL | PARAMETER  | 26C512A |      | 26C512A |      | 26C512A |      | UNIT | CONDITIONS                            |
|--------|--|---------|------|---------|------|---------|------|------|---------------------------------------|
|        |  | -10     |      | -12     |      | -15     |      |      |                                       |
|        |  | MIN.    | MAX. | MIN.    | MAX. | MIN.    | MAX. |      |                                       |
| tACC   | Address to Output Delay  |         | 100  |         | 120  |         | 150  | ns   | $\overline{CE} = \overline{OE} = VIL$ |
| tCE    | Chip Enable to Output Delay  |         | 100  |         | 120  |         | 150  | ns   | $\overline{OE} = VIL$                 |
| tOE    | Output Enable to Output Delay  |         | 45   |         | 50   |         | 65   | ns   | $\overline{CE} = VIL$                 |
| tDF    | $\overline{OE}$ High to Output Float,<br>or $\overline{CE}$ High to Output Float | 0       | 30   | 0       | 35   | 0       | 50   | ns   |                                       |
| tOH    | Output Hold from Address,<br>CE or OE which ever occurred first                  | 0       |      | 0       |      | 0       |      | ns   |                                       |

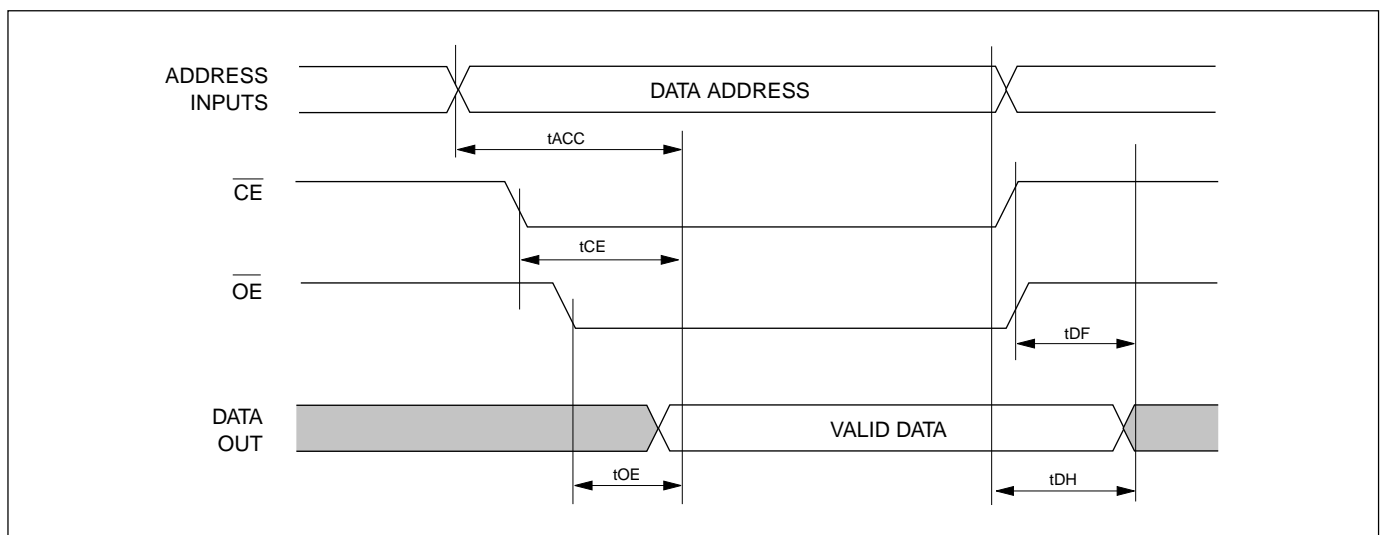
## DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

| SYMBOL | PARAMETER                                   | MIN. | MAX.      | UNIT | CONDITIONS  |
|--------|---|------|-----------|------|---|
| VOH    | Output High Voltage                         | 2.4  |           | V    | IOH = -0.40mA   |
| VOL    | Output Low Voltage                          |      | 0.4       | V    | IOL = 2.1mA   |
| VIH    | Input High Voltage                          | 2.0  | VCC + 0.5 | V    |   |
| VIL    | Input Low Voltage                           | -0.3 | 0.8       | V    |   |
| ILI    | Input Leakage Current                       | -10  | 10        | uA   | VIN = 0 to 5.5V                                       |
| VH     | A9 Auto Select Voltage                      | 11.5 | 12.5      | V    |   |
| ICC3   | VCC Supply Current (Program/Erase & Verify) |      | 50        | mA   |   |
| IPP2   | VPP Supply Current(Program)/Erase           |      | 50        | mA   | $\overline{CE} = PGM = VIL,$<br>$\overline{OE} = VIH$ |
| VCC2   | Programming & Erase Supply Voltage          | 4.5  | 6.5       | V    |   |
| VPP2   | Programming & Erase Voltage                 | 12.5 | 13.0      | V    |   |
| IPP A9 | A9 Auto Select Current /Erase               |      | 1         | mA   | $\overline{CE} = PGM = VIL,$<br>$\overline{OE} = VIH$ |

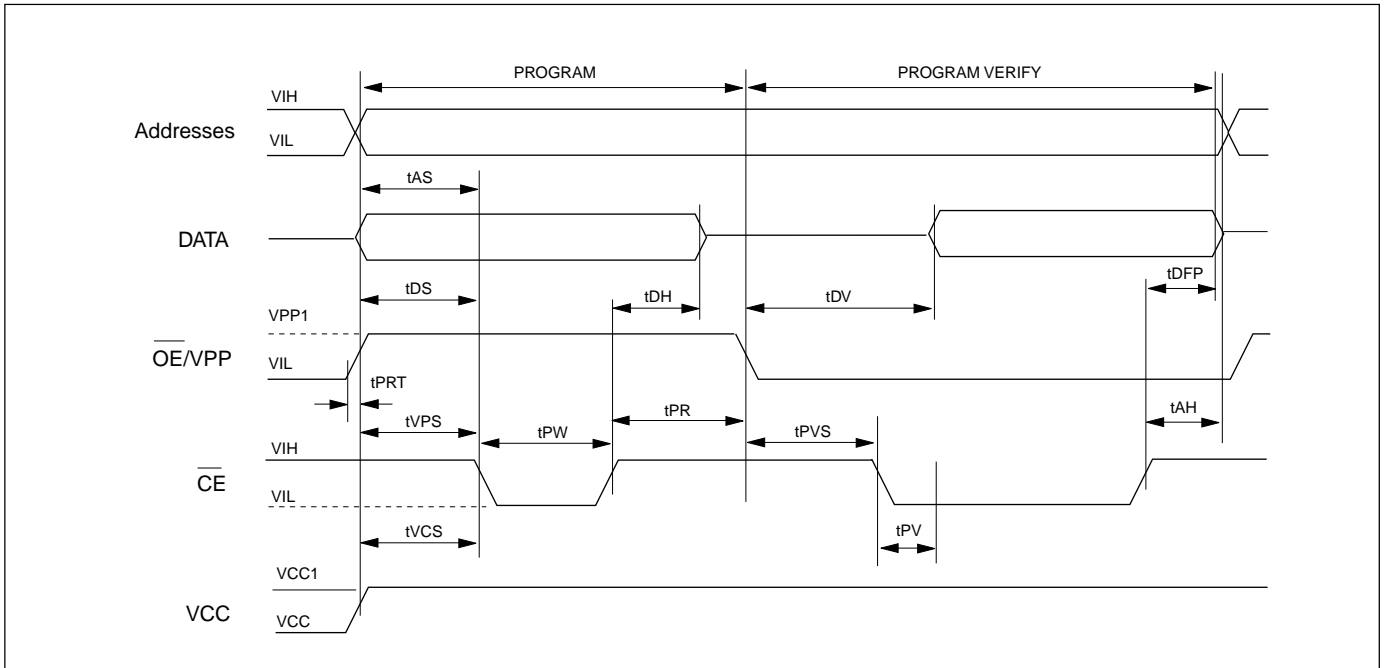
## AC PROGRAMMING CHARACTERISTICS $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$

| SYMBOL | PARAMETER                                    | MIN. | MAX. | UNIT | CONDITIONS |
|--------|--|------|------|------|------------|
| tAS    | Address Setup Time                           | 2.0  |      | us   |            |
| tOES   | $\overline{\text{OE}}$ Setup Time            | 2.0  |      | us   |            |
| tDS    | Data Setup Time                              | 2.0  |      | us   |            |
| tAH    | Address Hold Time                            | 0    |      | us   |            |
| tDH    | Data Hold Time                               | 2.0  |      | us   |            |
| tDFP   | $\overline{\text{CE}}$ to Output Float Delay | 0    | 130  | ns   |            |
| tVPS   | VPP Setup Time                               | 2.0  |      | us   |            |
| tPW    | Program Pulse Width                          | 20   | 105  | us   |            |
| tVCS   | VCC Setup Time                               | 2.0  |      | us   |            |
| tDV    | Data Valid from $\overline{\text{CE}}$       |      | 250  | ns   |            |
| tCES   | CE Setup Time                                | 2.0  |      | us   |            |
| tOE    | Data valid from $\overline{\text{OE}}$       |      | 150  | ns   |            |
| tER    | Erase Recovery Time                          | 0.5  |      | s    |            |
| tEW    | Erase Pulse Width                            | 0.5  |      | s    |            |
| tEV    | Erase Verify Time                            |      | 200  | ns   |            |
| tPV    | Program Verify Time                          |      | 200  | ns   |            |
| tA9S   | A9 Setup Time                                | 2.0  |      | us   |            |
| tPVS   | Program Verify Setup                         | 2    |      | us   |            |
| tEVS   | Erase Verify Setup                           | 0.5  |      | s    |            |

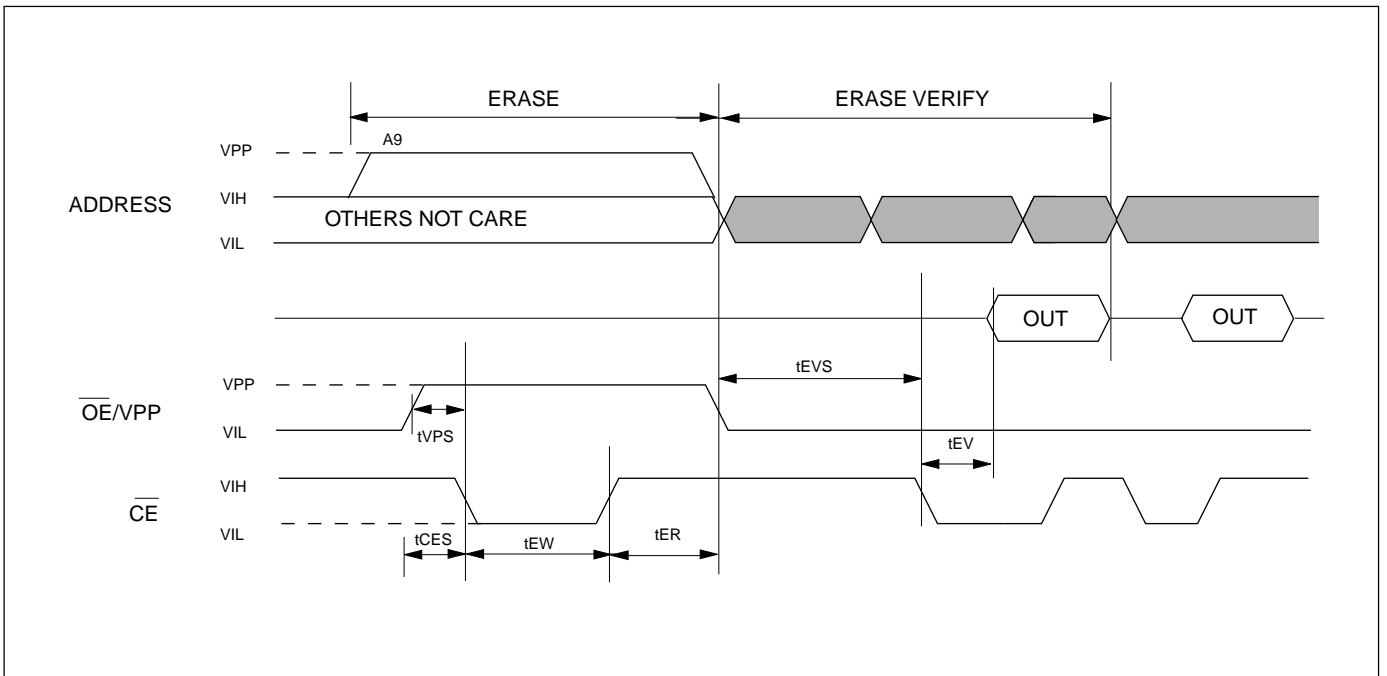
## WAVEFORMS READ CYCLE



## PROGRAMMING WAVEFORMS



## ERASE WAVEFORMS





## ORDERING INFORMATION

### PLASTIC PACKAGE

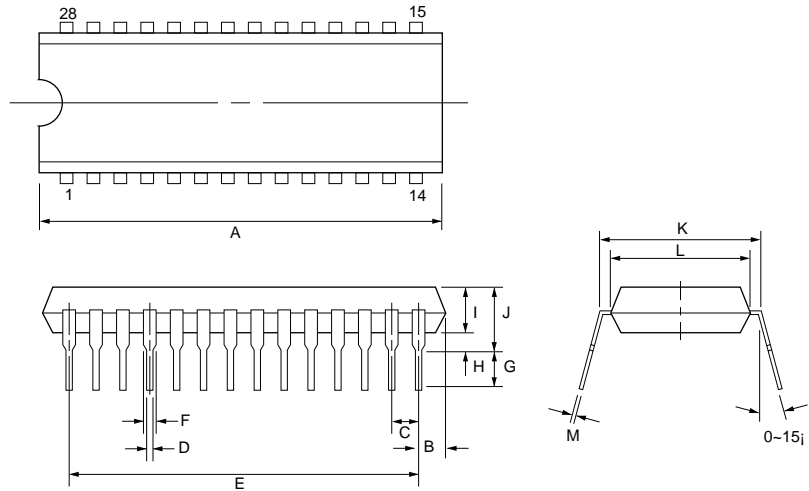
| PART NO.        | ACCESS TIME(ns) | OPERATING CURRENT MAX.(mA) | STANDBY CURRENT MAX.(uA) | PACKAGE        |
|-----------------|-----------------|----------------------------|--------------------------|----------------|
| MX26C512APC-70  | 70              | 30                         | 100                      | 28 Pin DIP     |
| MX26C512AMC-70  | 70              | 30                         | 100                      | 28 Pin SOP     |
| MX26C512AQC-70  | 70              | 30                         | 100                      | 32 Pin PLCC    |
| MX26C512ATC-70  | 70              | 30                         | 100                      | 28 Pin TSOP(I) |
| MX26C512APC-90  | 90              | 30                         | 100                      | 28 Pin DIP     |
| MX26C512AMC-90  | 90              | 30                         | 100                      | 28 Pin SOP     |
| MX26C512AQC-90  | 90              | 30                         | 100                      | 32 Pin PLCC    |
| MX26C512ATC-90  | 90              | 30                         | 100                      | 28 Pin TSOP(I) |
| MX26C512APC-100 | 100             | 30                         | 100                      | 28 Pin DIP     |
| MX26C512AMC-100 | 100             | 30                         | 100                      | 28 Pin SOP     |
| MX26C512AQC-100 | 100             | 30                         | 100                      | 32 Pin PLCC    |
| MX26C512ATC-100 | 100             | 30                         | 100                      | 28 Pin TSOP(I) |
| MX26C512APC-120 | 120             | 30                         | 100                      | 28 Pin DIP     |
| MX26C512AMC-120 | 120             | 30                         | 100                      | 28 Pin SOP     |
| MX26C512AQC-120 | 120             | 30                         | 100                      | 32 Pin PLCC    |
| MX26C512ATC-120 | 120             | 30                         | 100                      | 28 Pin TSOP(I) |
| MX26C512APC-150 | 150             | 30                         | 100                      | 28 Pin DIP     |
| MX26C512AMC-150 | 150             | 30                         | 100                      | 28 Pin SOP     |
| MX26C512AQC-150 | 150             | 30                         | 100                      | 32 Pin PLCC    |
| MX26C512AC-150  | 150             | 30                         | 100                      | 28 Pin TSOP(I) |

## PACKAGE INFORMATION

### 28-PIN PLASTIC DIP (600 mil)

| ITEM | MILLIMETERS | INCHES      |
|------|-------------|-------------|
| A    | 37.34 max   | 1.470 max   |
| B    | 2.03 [REF]  | .080 [REF]  |
| C    | 2.54 [TP]   | .100 [TP]   |
| D    | .46 [Typ.]  | .018 [Typ.] |
| E    | 32.99       | 1.300       |
| F    | 1.52 [Typ.] | .060 [Typ.] |
| G    | 3.30 ± .25  | .130 ± .010 |
| H    | .51 [REF]   | .020 [REF]  |
| I    | 3.94 ± .25  | .155 ± .010 |
| J    | 5.33 max.   | .210 max.   |
| K    | 15.22 ± .25 | .600 ± .010 |
| L    | 13.84 ± .25 | .545 ± .010 |
| M    | .25 [Typ.]  | .010 [Typ.] |

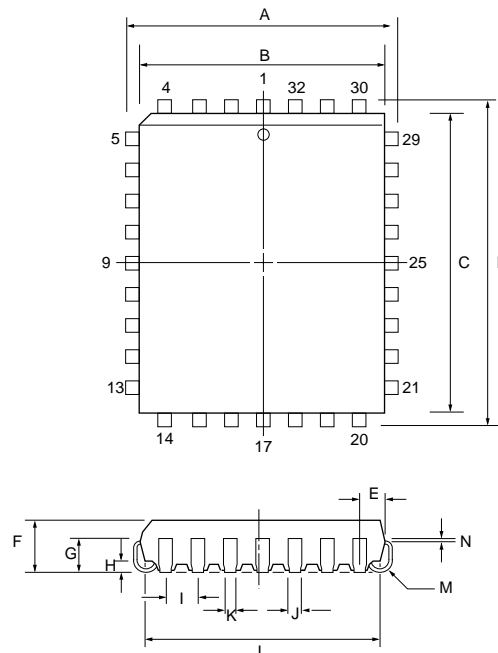
**NOTE:** Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



### 32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

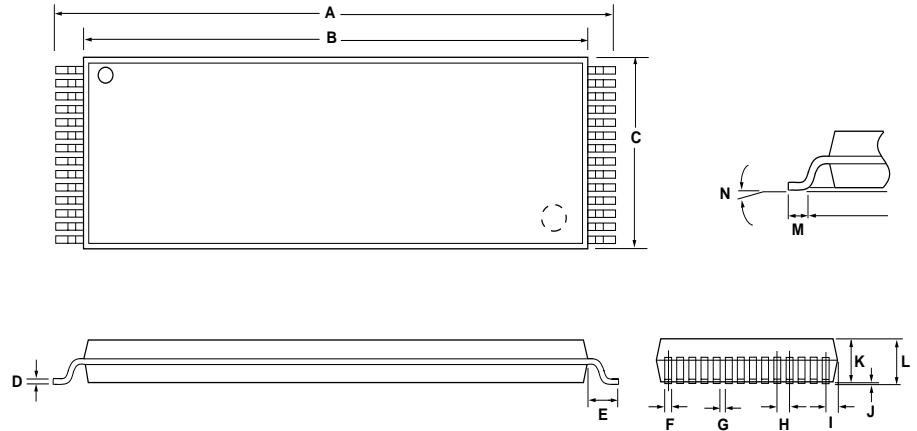
| ITEM | MILLIMETERS | INCHES      |
|------|-------------|-------------|
| A    | 12.44 ± .13 | .490 ± .005 |
| B    | 11.50 ± .13 | .453 ± .005 |
| C    | 14.04 ± .13 | .553 ± .005 |
| D    | 14.98 ± .13 | .590 ± .005 |
| E    | 1.93        | .076        |
| F    | 3.30 ± .25  | .130 ± .010 |
| G    | 2.03 ± .13  | .080 ± .005 |
| H    | .51 ± .13   | .020 ± .005 |
| I    | 1.27 [Typ.] | .050 [Typ.] |
| J    | .71 [REF]   | .028 [REF]  |
| K    | .46 [REF]   | .018 [REF]  |
| L    | 10.40/12.94 | .410/.510   |
|      | (W) (L)     | (W) (L)     |
| M    | .89 R       | .035 R      |
| N    | .25 (TYP.)  | .010 (TYP.) |

**NOTE:** Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



## 28-PIN PLASTIC TSOP

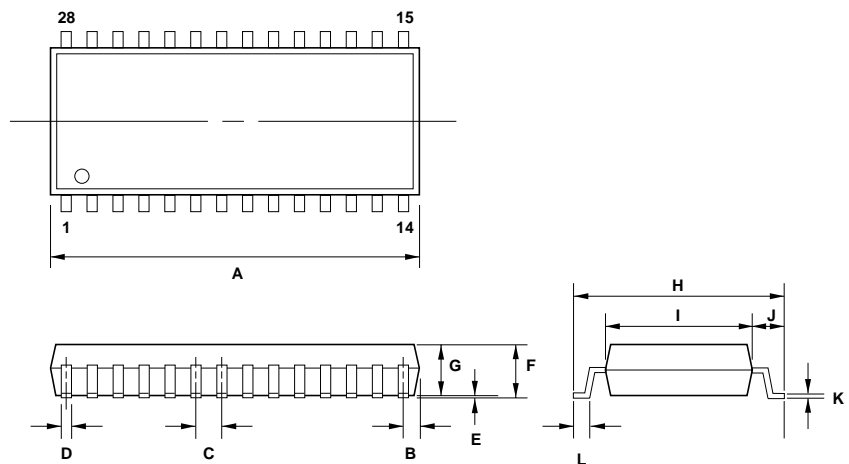
| ITEM | MILLIMETERS |
|------|-------------|
| A    | 13.4 ± .2   |
| B    | 11.8 ± .1   |
| C    | 8.0 ± .1    |
| D    | .15 ± .01   |
| F    | .2 ± .03    |
| H    | .55 [Typ.]  |
| I    | .425 [Typ.] |
| J    | .05 [Min.]  |
| K    | 1.00 ± .05  |
| L    | 1.25 [Max.] |
| M    | .05 ± .20   |
| N    | 0° ~ 5°     |



**NOTE:** Each lead centerline is located within .25 mm of its true position [TP] at maximum material condition.

## 28-PIN PLASTIC SOP(330 mil)

| ITEM | MILLIMETERS | INCHES      |
|------|-------------|-------------|
| A    | 18.62 max.  | .733 max.   |
| B    | 1.194 max   | .047 max    |
| C    | 1.27 [TP]   | .050 [TP]   |
| D    | .41 [Typ.]  | .016 [Typ.] |
| E    | .10 min.    | .004 min.   |
| F    | 2.85 max.   | .110 max.   |
| G    | 2.49 ± .13  | .098 ± .005 |
| H    | 11.81 ± .31 | .465 ± .012 |
| I    | 8.41 ± .13  | .331 ± .005 |
| J    | 1.70 ± .20  | .067 ± .008 |
| K    | .25 [Typ.]  | .010 [Typ.] |
| L    | .91 ± .20   | .036 ± .008 |



**NOTE:** Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



**Revision History**

| <b>Revision#</b> | <b>Description</b>   | <b>Date</b> |
|------------------|--|-------------|
| 1.2              | Add 28 pin TSOP and SOP packages.  | 3/28/1997   |
| 1.3              | Erasing mode flow chart: Chip erase (5s)----> (1s).<br>Programming waveforms: CE changed.  | 4/10/1997   |
| 1.4              | MTP ROM--->MTP EPROM<br>Chip erase(1s)--->0.5s. X = 60?--->200?<br>Switching Test Waveforms revise.<br>tEW Erase Pulse Width 1 sec---> 0.5 sec.<br>Programming/erase waveforms modification.<br>VPP:from 12.0~13V to 12.5V ~13V. | 5/30/1997   |
| 1.5              | Erase Verify Time: 60 ---->200.  | 7/25/1997   |
| 1.6              | Change Part Name: 26C512 ---> 26C512A  | 11/05/1997  |
| 1.7              | Change tPW:Min. 95us -->Min. 20us.<br>Programming flow chart revised.<br>Mode Select Table, Erase Mode A9=VH-->A9=Vpp.<br>Erase flow chart revised.  | 2/10/1998   |
| 1.8              | Delete IPP in DC CHARACTERISTICS   | 7/13/1998   |



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