



# MX23L8100

## 8M-BIT MASK ROM(8/16 BIT OUTPUT)

### FEATURES

- Bit organization
  - 1M x 8 (byte mode)
  - 512K x 16 (word mode)
- Fast access time
  - Random access: 100ns (max.)
- Current
  - Operating: 20mA
  - Standby: 5uA
- Supply voltage
  - 3.3V±10%
- Package
  - 44 pin SOP (500mil)
  - 42 pin PDIP (600mil)
  - 48 pin TSOP (type 1)
  - 44 pin TSOP (type 2)

### ORDER INFORMATION

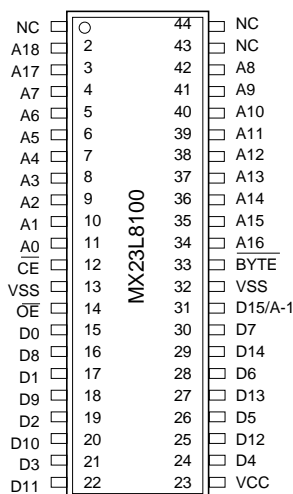
Part No.	Access Time	Package
MX23L8100MC-10	100ns	44 pin SOP
MX23L8100MC-12	120ns	44 pin SOP
MX23L8100MC-15	150ns	44 pin SOP
MX23L8100PC-10	100ns	42 pin PDIP
MX23L8100PC-12	120ns	42 pin PDIP
MX23L8100PC-15	150ns	42 pin PDIP
MX23L8100TC-10	100ns	48 pin TSOP*
MX23L8100TC-12	120ns	48 pin TSOP
MX23L8100TC-15	150ns	48 pin TSOP
MX23L8100RC-10	100ns	48 pin RTSOP*
MX23L8100RC-12	120ns	48 pin RTSOP
MX23L8100RC-15	150ns	48 pin RTSOP
MX23L8100YC-10	100ns	44 pin TSOP
MX23L8100YC-12	120ns	44 pin TSOP
MX23L8100TI-10	100ns	48 pin TSOP*

Note: 1.48-TSOP and 48-RTSOP support word mode only, not for byte mode.

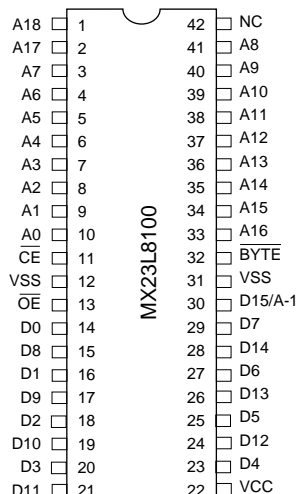
2.MX23L8100TI-10 is for industrial grade, temperature -40~85°C

### PIN CONFIGURATION

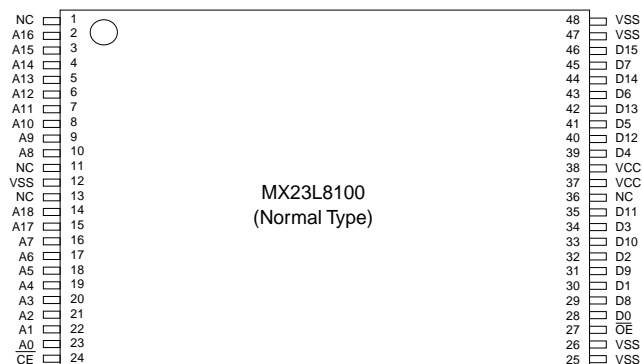
#### 44 SOP/44TSOP



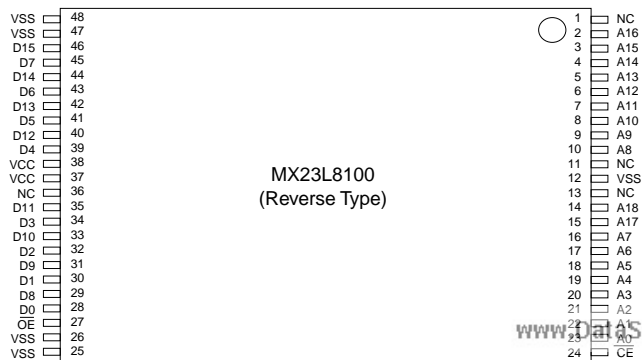
#### 42 PDIP



#### 48 TSOP (for word mode only)



#### 48 Reverse TSOP (for word mode only)





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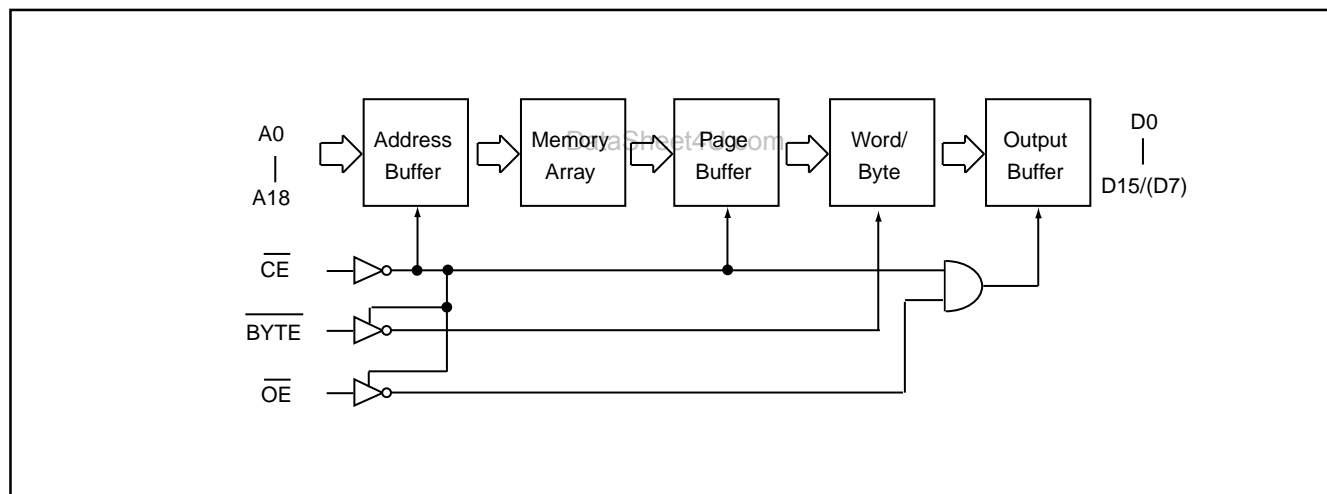
## PIN DESCRIPTION

Symbol	Pin Function
A0~A18	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15(Word Mode)/LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
Byte	Word/Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

## MODE SELECTION

$\overline{CE}$	$\overline{OE}$	Byte	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

## BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to VCC+2.0V (Note)
Ambient Operating Temperature	T <sub>opr</sub>	0°C to 70°C
Storage Temperature	T <sub>stg</sub>	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.



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## DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	24V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	20mA	f=10MHz, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$ =VIH
Standby Current (CMOS)	ISTB2	-	5uA	$\overline{CE}$ > VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

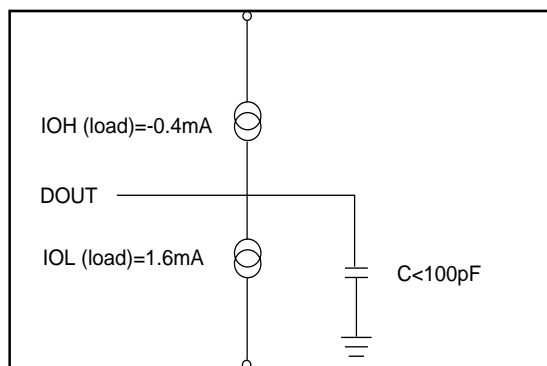
## AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	23L8100-10		23L8100-12		23L8100-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

## AC Test Conditions

Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note: No output loading is present in tester load board.

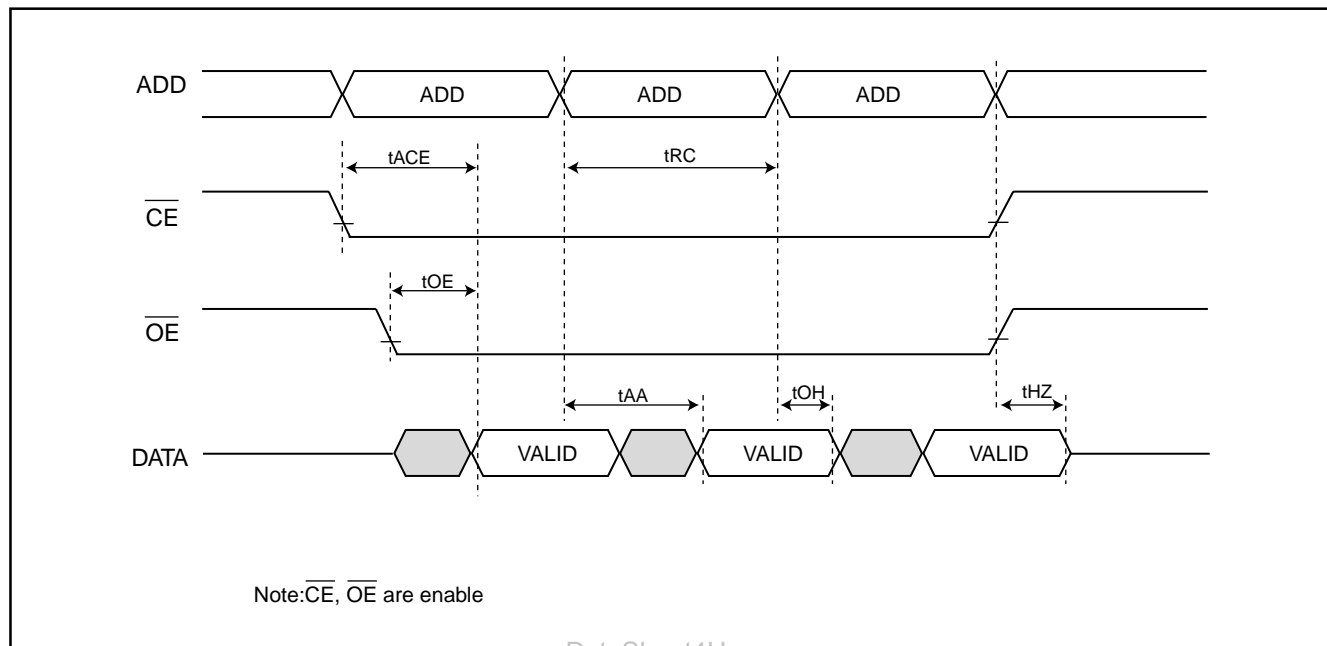
Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.



## TIMING DIAGRAM

## RANDOM READ



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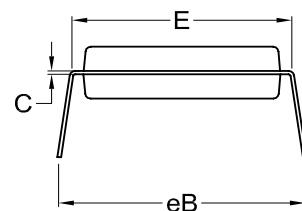
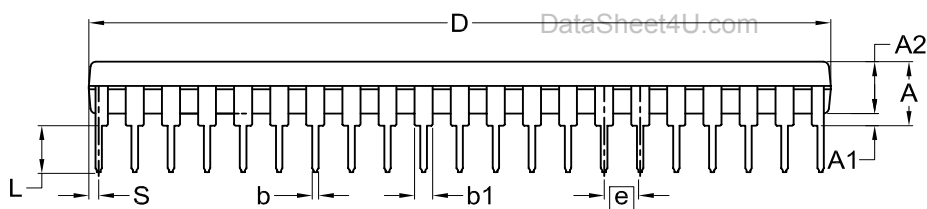
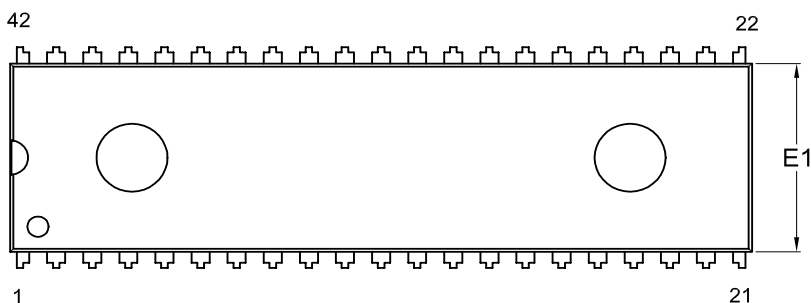
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**PACKAGE INFORMATION**

**Title:** Package Outline for PDIP 42L (600MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

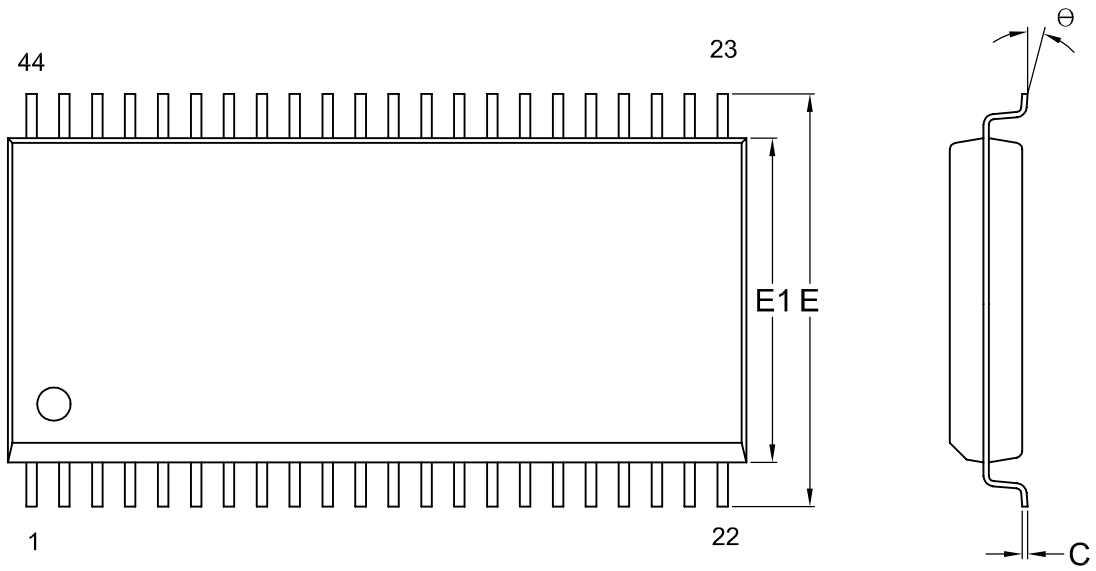
SYMBOL		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
UNIT														
mm	Min.	---	0.25	3.73	0.38	1.14	0.20	51.31	15.11	13.84		15.75	2.92	0.38
	Nom.	---	---	3.94	0.46	1.27	0.25	51.94	15.24	13.97	2.54	16.51	3.30	0.64
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	52.57	15.37	14.10		17.27	3.68	0.89
Inch	Min.	—	0.010	0.147	0.015	0.045	0.008	2.020	0.595	0.545		0.620	0.115	0.015
	Nom.	—	—	0.155	0.018	0.050	0.010	2.045	0.600	0.550	0.100	0.650	0.130	0.025
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	2.070	0.605	0.555		0.680	0.145	0.035

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.5	7				01-20-03

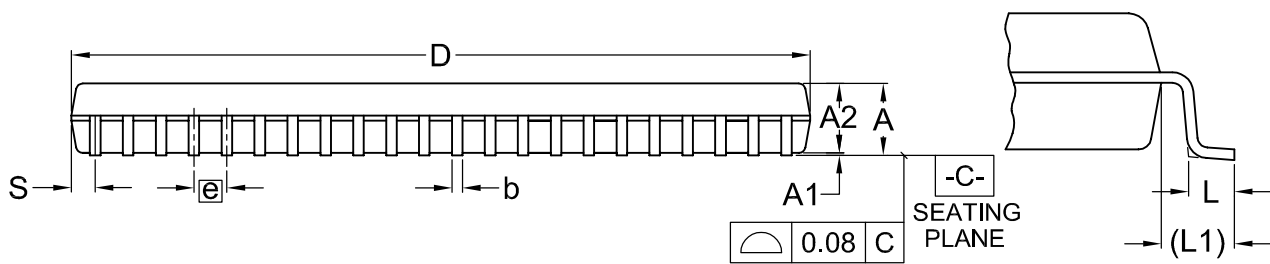


# MX23L8100

**Title: Package Outline for SOP 44L (500MIL)**



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Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	$\theta$
UNIT														
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47		0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73		0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491		0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501		0.038	0.075	0.041	10

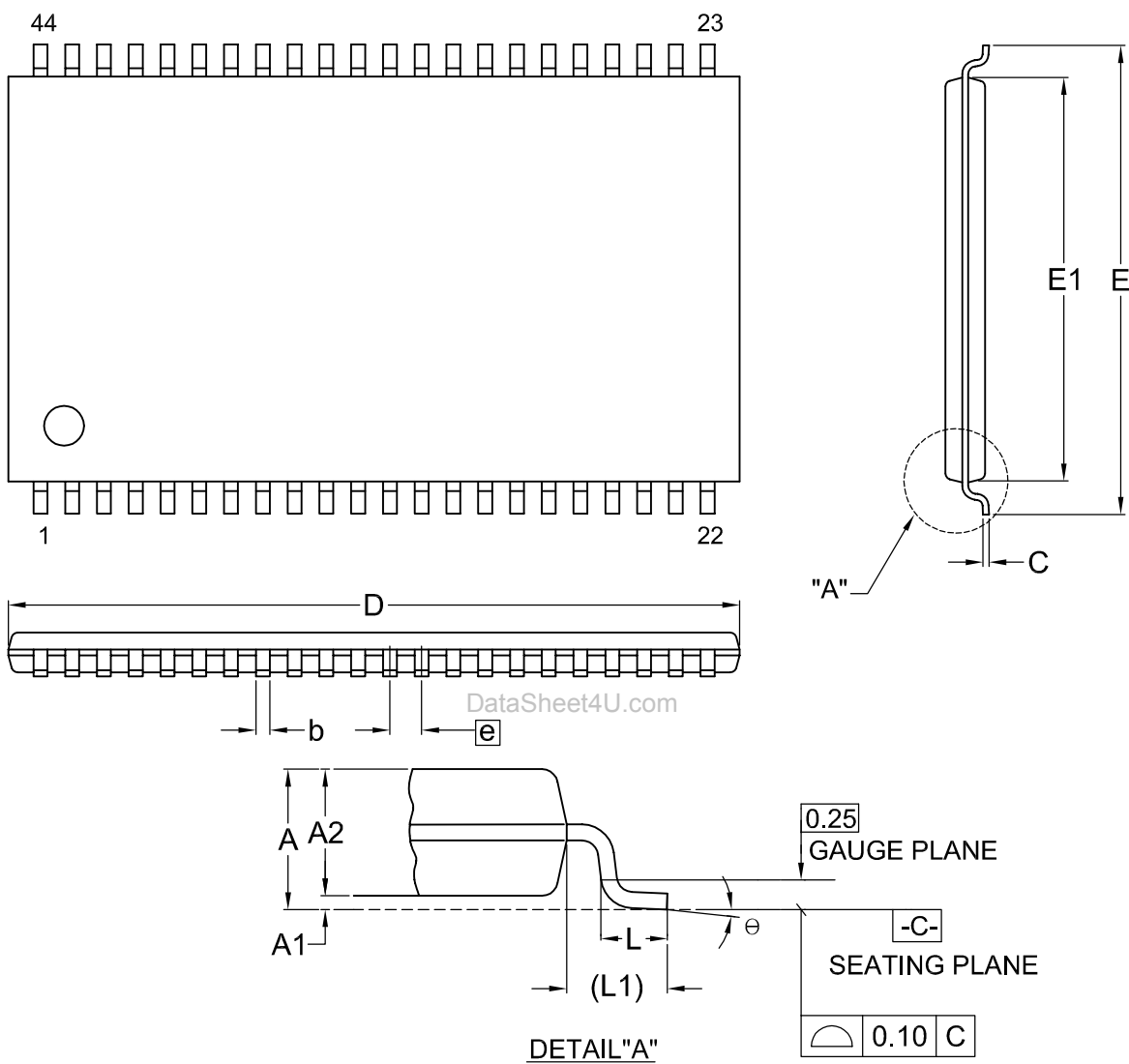
DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	5	MO-175			09-24-'02

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# MX23L8100

**Title: Package Outline for TSOP(II) 44L (400MIL)**



Dimensions (inch dimensions are derived from the original mm dimensions)

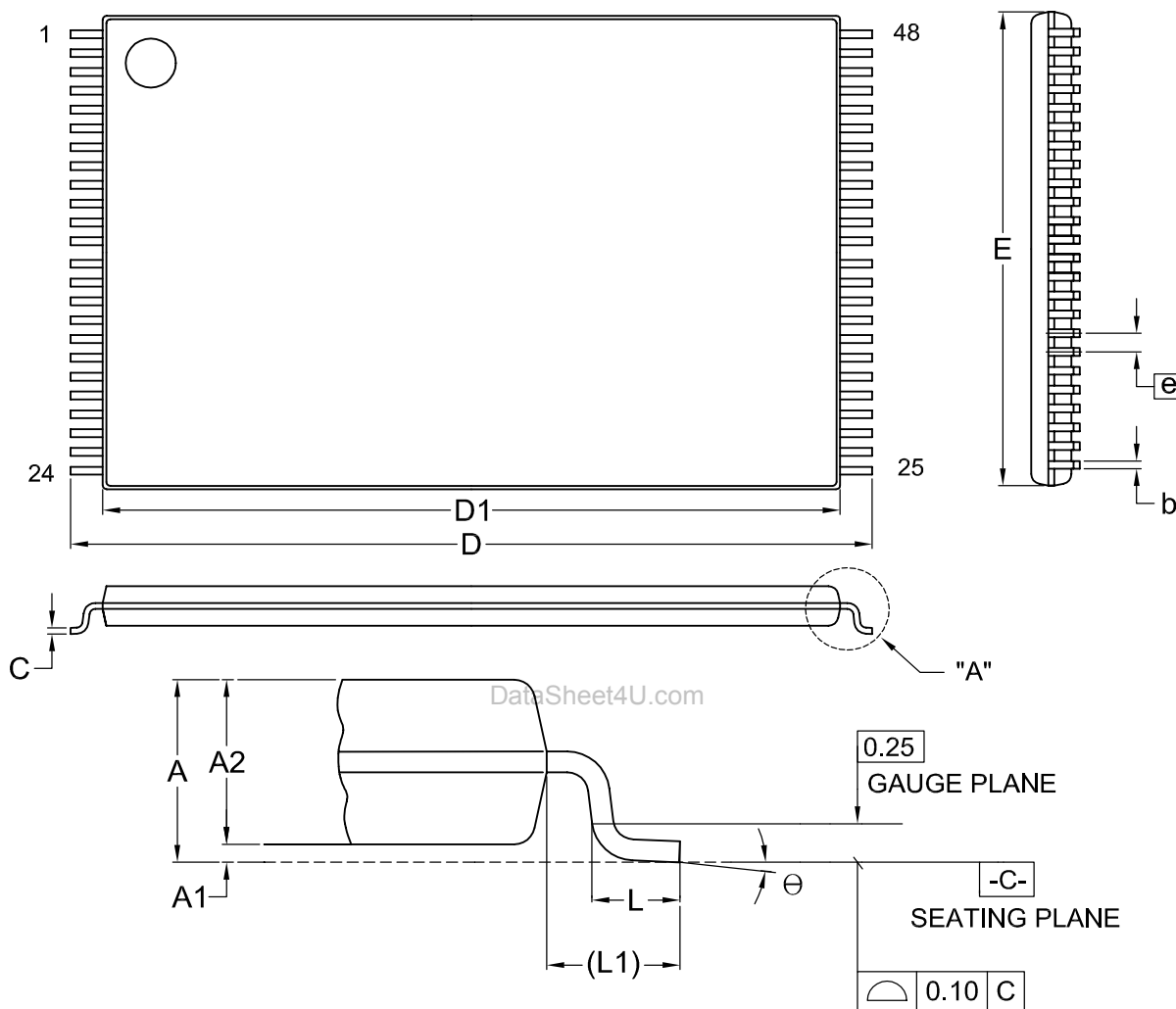
SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
UNIT													
mm	Min.	---	0.05	0.95	0.30	0.12	18.31	11.56	10.06		0.40	0.70	0
	Nom.	---	0.10	1.00	0.35	0.15	18.41	11.76	10.16	0.80	0.50	0.80	5
	Max.	1.20	0.15	1.05	0.45	0.21	18.51	11.96	10.26		0.60	0.90	8
Inch	Min.	---	0.002	0.037	0.012	0.005	0.721	0.455	0.396		0.016	0.028	0
	Nom.	---	0.004	0.039	0.014	0.006	0.725	0.463	0.400	0.031	0.020	0.031	5
	Max.	0.047	0.006	0.041	0.018	0.008	0.729	0.471	0.404		0.024	0.035	8

DWG.NO.	REVISION	REFERENCE		ISSUE DATE
		JEDEC	EIAJ	
6110-1701	5	MS-024		09-24-02



# MX23L8100

**Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM**



**DETAIL "A"**

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

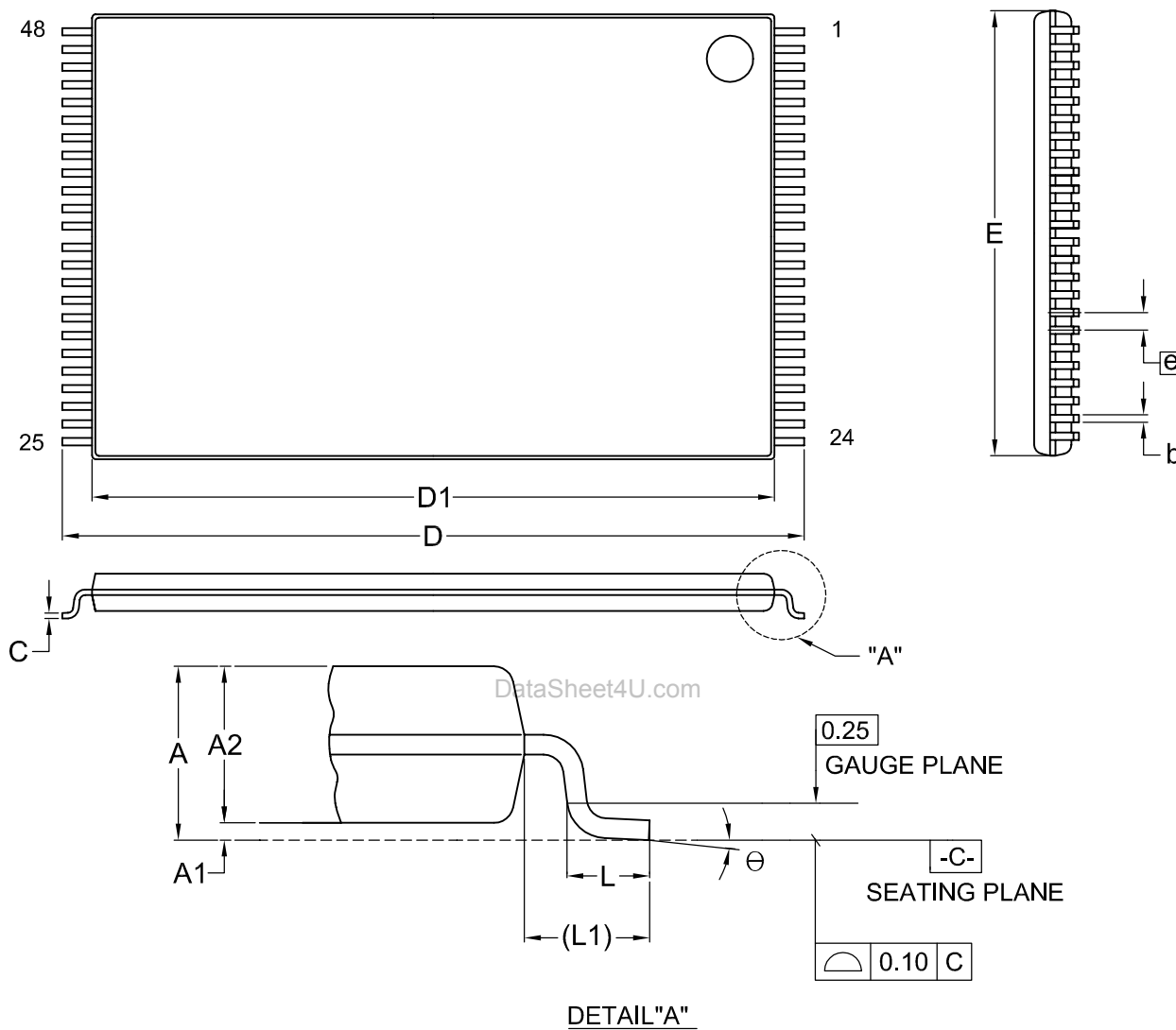
DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	6	MO-142			09-24-'02





# MX23L8100

**Title: Package Outline for TSOP(I) 48L (12X20mm)REVERSE FORM**



DETAIL "A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	θ
UNIT													
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607.1	6	MO-142			09-24-02



## REVISION HISTORY

Revision	Description	Page	Date
1.4	Add new 44pin TSOP (type 2)		Jul/17/1998
1.5	AC CHARACTERISTICS tOH 10ns-->0ns	P3	FEB/01/1999
1.6	Correct Typing error	P1	JUL/16/2001
	Modify Package Information	P5~7	
1.7	Added MX23L8100TI-10 in Order Information	P1	AUG/20/2001
1.8	Modify Package Information	P5~9	NOV/21/2002
1.9	Modify 42-PDIP Package Information	P5	JUN/19/2003

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