



PRELIMINARY MX23L6430

64M-Bit Synchronous Mask ROM

FEATURES

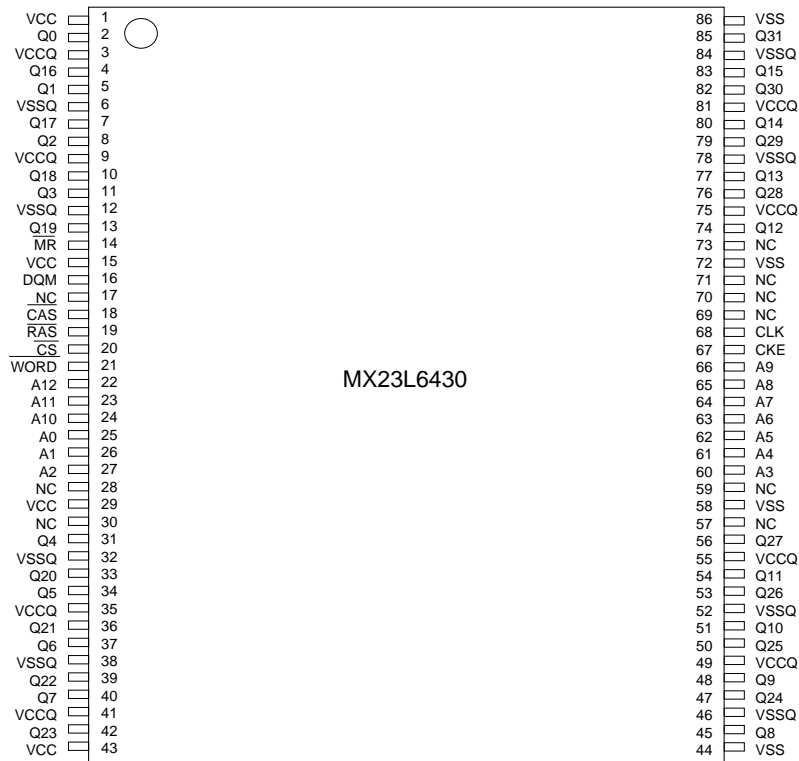
- Switchable organization : 4M x 16 (word mode) or 2M x 32 (double word mode)
- Power supply 3.0V ~ 3.6V
- TTL compatible with multiplexed address
- All inputs are sampled at rising edge of system clock
- Read performance :
 - 4-1-1-1@33MHz(RAS Latency=1, CAS Latency=3)
 - 5-1-1-1@50MHz(RAS Latency=1, CAS Latency=4)
 - 7-1-1-1@66MHz(RAS Latency=2, CAS Latency=5)
- - 7-1-1-1@100MHz(RAS Latency=2, CAS Latency=5)
- - Clock to valid output delay (tSAC) : 6ns(Max.)
- MRS cycle with address key programs :
 - RAS Latency : 1 & 2
 - CAS Latency : 2 ~ 8
 - Burst Length : 8 double word
 - Burst Type : Sequential or Interleaved
- DQM for data-out masking
- Package : 86 pin TSOP(II)

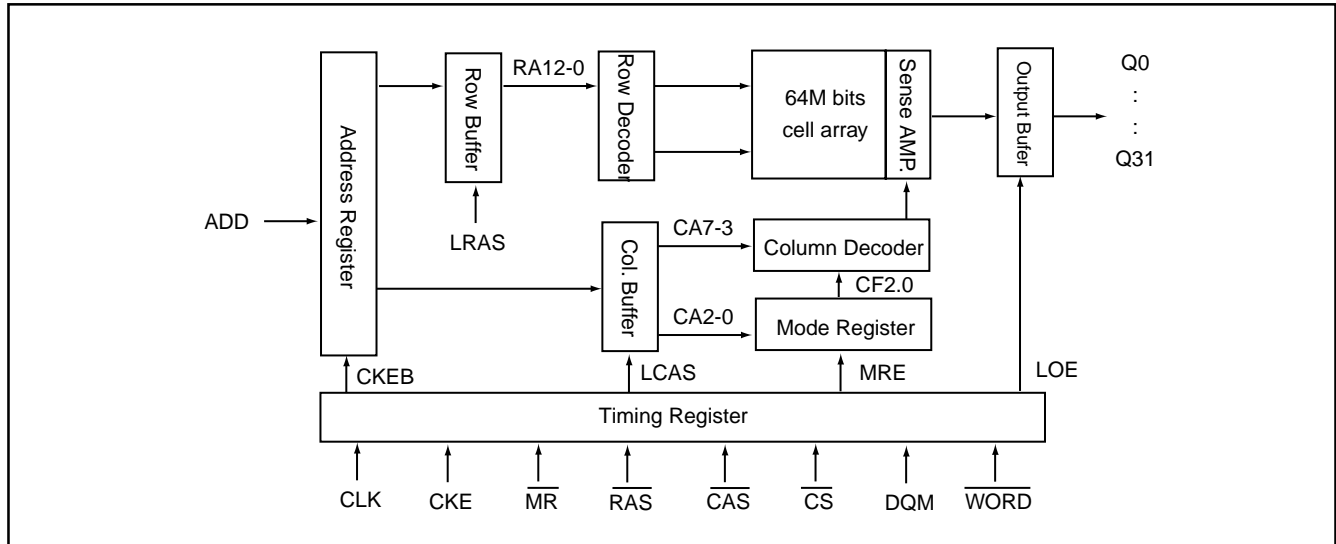
GENERAL DESCRIPTION

The 64M synch. MROM is a synchronous high bandwidth mask programmable ROM with MXIC's high performance CMOS process technology and is organized either as 4M x 16 bits or 2M x 32 bits depending on polarity of WORD pin. Synchronous design allows precise cycle control , with the use of system clock, I/O

transaction are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system application.

PIN CONFIGURATION



BLOCK DIAGRAM

PIN DESCRIPTION

| Symbol | Name | Function |
|-----------|---------------------------|--|
| CLK | System Clock | Active on the rising edge to sample all inputs |
| CS | Chip Select | Disable or enable device operation by masking or enabling all inputs except CLK and CKE |
| CKE | Clock Enable | Mask system clock to freeze operation from next clock cycle and disable input buffers for power down in standby. |
| A0 ~ A12 | Address | Row/Column addresses are multiplexed on the same pins. Row address : RA0~RA12 , Col. address : CA0~CA7(x32) or CA0~CA8(x16) |
| RAS | Row address Strobe | Latch row addresses on the rising edge of the CLK with RAS low and enable row access |
| CAS | Column address Strobe | Latch column addresses on the rising edge of the CLK with CAS low and enable column access |
| MR | Mode Register Set | Enable mode register set with MR low (simultaneously CS , RAS and CAS are low) |
| Q0 ~ Q31 | Data Output | Data output according to the rising edge of CLK |
| VDD/VSS | Power Supply / Ground | Power and ground for the input buffers and the core logic |
| VDDQ/VSSQ | Data Output Power/ Ground | Power and ground for the output buffers to provide improved noise immunity |
| WORD | x32/x16 Mode Selection | Double word mode / word mode, depending on polarity of WORD pin. Should be set before CAS enabling |
| DQM | Data Out Masking | It works similar to OE during read operation |
| NC | No Connection | |



ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings |
|-------------------------------|--------|---------------------|
| Power Supply Voltage | VCC | -0.5V to 4.6V |
| Input Voltage | VI | -0.5V to VCC + 0.5V |
| Output Voltage | VO | -0.5V to VCC + 0.5V |
| Ambient Operating Temperature | Topr | 0°C to 70°C |
| Storage Temperature | Tstg | -55°C to 125°C |

DC CHARACTERISTIC (Ta=0°C~70°C, VCC=3.3V±0.3V)

| Item | Symbol | MIN. | MAX. | Conditions |
|---------------------------|--------|-------|----------|--|
| Standby Current | ICC3P | - | 1mA | CKE=VIL, tCC=Min. |
| | ICC3PS | - | 100uA | CKE=0, tCC=Min. |
| Active standby Current | ICC3N | - | 50mA | CS=VIH, tCC=Min., All outputs open (Note 1) |
| Burst Operating Current | ICC4 | - | 150mA | tCC=Min., All outputs open |
| Input Leakage Current | IIL | -10uA | 10uA | 0≤VIN≤VDD+0.3V |
| Output Leakage Current | IOL | -10uA | 10uA | 0≤VOUT≤VDD+0.3V |
| Input High Voltage | VIH | 2.0V | VDD+0.3V | |
| Input Low Voltage | VIL | -0.3V | 0.8V | |
| Output High Voltage Level | VOH | 2.4V | - | IOH=-2mA |
| Output Low Voltage Level | VOL | - | 0.4V | IOL=2mA |

Note 1: The active standby current is also for clock suspend mode.

AC CHARACTERISTIC (Ta=0°C~70°C, VCC=3.3V±0.3V)

| Item | Symbol | up to 100MHz | | up to 66MHz | | up to 50MHz | | up to 33MHz | |
|---|--------|--------------|------|-------------|------|-------------|------|---------------------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |
| CLK Cycle Time | tCC | 10ns | - | 15ns | - | 20ns | - | 30ns | - |
| CLK to Valid Output Delay | tSAC | - | 6ns | - | 6ns | - | 6ns | - | 6ns |
| Data Output Hold Time | tOH | 4ns | - | 4ns | - | 4ns | - | 4ns | - |
| CLK High Pulse Width | tCH | 3ns | - | 4ns | - | 6.5ns | - | 11.5ns | - |
| CLK Low Pulse Width | tCL | 3ns | - | 4ns | - | 6.5ns | - | 11.5ns | - |
| Input Setup Time | tSS | 4ns | - | 4ns | - | 4ns | - | 4ns | - |
| Input Hold Time | tSH | 2ns | - | 2ns | - | 2ns | - | 2ns | - |
| CLK to Output in Low-Z | tSLZ | 0ns | - | 0ns | - | 0ns | - | 0ns | - |
| CLK to Output in High-Z | tSHZ | - | 6ns | - | 10ns | - | 15ns | - | 25ns |
| Power Down Exit Setup Time | tPDE | tSS+tCC- | | tSS+tCC - | | tSS+tCC - | | tSS+tCC - | |
| Row Active to Row Active | tRC | 6 cycles - | | 6 cycles - | | 4 cycles - | | 4 cycles - (Note 1) | |
| CAS Enable to Row Active | tCR | 4 cycles - | | 4 cycles - | | 3 cycles - | | 3 cycles - (Note 2) | |
| Valid CAS Enable to Valid CAS Enable | tCCD | 4 cycles - | | 4 cycles - | | 3 cycles - | | 3 cycles - (Note 2) | |

Note 1: (RAS latency+CAS latency)@33MHz, (RAS latency+CAS latency-1)@50MHz, 66MHz,100MHz

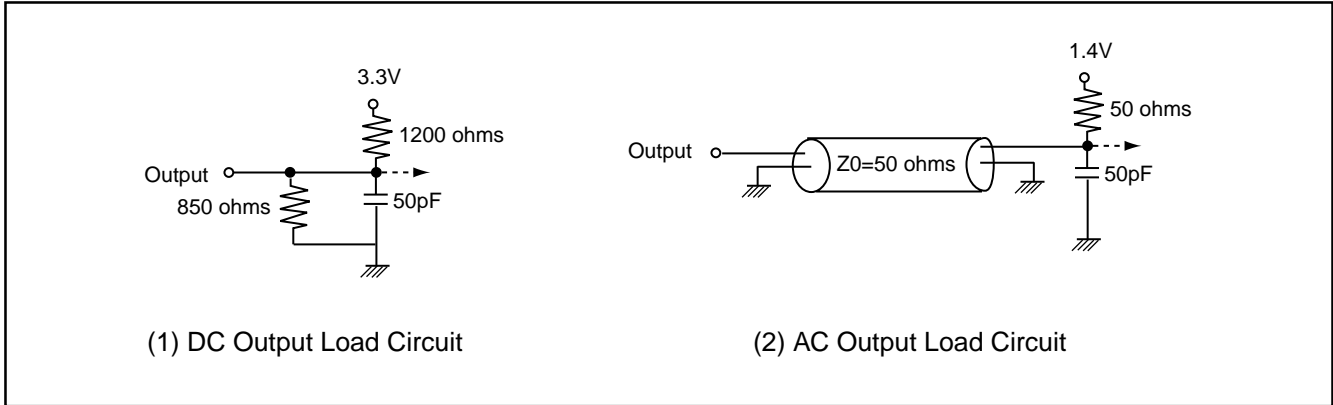
Note 2: Equal to (CAS latency)@33MHz, (CAS latency-1)@50MHz, 66MHz, 100MHz

AC TEST CONDITION

| | |
|--------------------------------|-------------------|
| Input Pulse levels | VIH/VIL=2.4V/0.4V |
| Input and Output Timing Levels | 1.4V |
| Input Rise and Fall Times | tR/tF=1ns/1ns |
| Output Load | LVTTL |

*Note: If CLK transition time is longer than 1ns, timing parameters should be compensated. Add (tR+tF)/2-1ns for transition time longer than 1ns. Transitions time is measured between VIL(Max.) and VIH(Min.)

*LVTTTL:



CAPACITANCE

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT |
|--------------------|------------------|------|------|------|
| Input Capacitance | C _{in} | - | 5 | pF |
| Output capacitance | C _{out} | - | 7 | pF |

FUNCTION TRUTH TABLE (V=valid, X=don't care, H=Logic High, L=Logic Low)

| COMMAND | | CKE _{n-1} | CKE _n | CS | RAS | CAS | MR | DQM | Add. | WORD | NOTES |
|-------------------------------|---------------------|--------------------|------------------|----|-----|-----|----|-----|------|------|-------|
| Register | Mode Register Set | H | x | L | L | L | L | x | Code | x | 1 |
| Row Active | Row Access & Latch | H | x | L | L | H | H | x | RA | x | |
| Read | Col. Access & Latch | H | x | L | H | L | H | x | CA | x | |
| Burst Stop | | H | x | L | H | H | L | x | x | x | |
| | Precharge on DRAM | H | x | L | L | H | L | x | x | x | |
| Power Down & Clock Suspend | Standby Entry | H | L | x | x | x | x | x | x | x | 2 |
| | Standby Exit | L | H | x | x | x | x | x | x | x | |
| DQM | | H | x | x | x | x | x | V | x | x | 3 |
| No Operation | | H | x | H | x | x | x | x | x | x | 4 |
| | | H | x | L | H | H | H | x | x | x | 4 |
| | | H | x | L | H | L | L | x | x | x | 4 |
| | | H | x | L | L | L | H | x | x | x | 4 |
| Organization Control | | H | x | L | H | L | H | x | CA | H | 5 |
| | | H | x | L | H | L | H | x | CA | L | 5 |

Notes :

- A0~A6 : Program keys. After power up, mode register set should be set before entering other input command, After the mode register set command is completed, no new commands can be issued for 3 CLK cycles, and MR state must be defined "H" within 3 CLK cycles.
- In the case CKE is low, two standby modes are possible. Those are standby mode in power-down and active standby mode in clock suspend.
 Power Down : CKE=L (at all parts except the range of sensing and data out operation)
 Clock Suspend : CKE=L (at the range of sensing and data out operation)
- DQM sampled at rising edge of a CLK makes a Hi-Z state or data output state, delayed by 2 CLK cycles.
- NOP(No Operation) state on syn. MROM includes not only NOP but also precharge, refresh and write state on syn. DRAM .
- Organization mode selection control is decided simultaneously with column access start, and according to the polarity of WORD pin.

MODE REGISTER FIELD TABLE (programmed with MRS)

| RAS Latency | | CAS Latency | | | | Burst Type | | Burst Length | | |
|-------------|--------|-------------|----|----|----------|------------|------------|--------------|----|----------|
| A6 | Length | A5 | A4 | A3 | Length | A2 | Type | A1 | A0 | Length |
| 0 | 1 | 0 | 0 | 0 | reserved | 0 | sequential | 0 | 0 | reserved |
| 1 | 2 | 0 | 0 | 1 | 2 | 1 | interleave | 0 | 1 | 4 |
| | | 0 | 1 | 0 | 3 | | | 1 | 0 | 8 |
| | | 0 | 1 | 1 | 4 | | | 1 | 1 | reserved |
| | | 1 | 0 | 0 | 5 | | | | | |
| | | 1 | 0 | 1 | 6 | | | | | |
| | | 1 | 1 | 0 | 7 | | | | | |
| | | 1 | 1 | 1 | 8 | | | | | |

Notes :

1. After power up, mode register set should be completed at one time and fixed to "H" within 3 CLK cycles.
2. After power up, when user wants to change mode register, user must exit from power down mode and start mode register set before entering normal operation mode .
3. The power-up default mode register field : RAS latency -> 2, CAS latency ->5, Burst type -> sequential, Burst length -> 4
4. The default mode register field is ROM Code changeable.

BURST SEQUENCE
Burst Length = 4 (x32)

| Initial Col. Addr. | | Sequential | | | | Interleave | | | |
|--------------------|-----|------------|---|---|---|------------|---|---|---|
| CA1 | CA0 | ® | ® | | | ® | ® | | |
| 0 | 0 | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 |
| 0 | 1 | 1 | 2 | 3 | 0 | 1 | 0 | 3 | 2 |
| 1 | 0 | 2 | 3 | 0 | 1 | 2 | 3 | 0 | 1 |
| 1 | 1 | 3 | 0 | 1 | 2 | 3 | 2 | 1 | 0 |

Burst Length = 8 (x32)

| Initial Col. Addr. | | | Sequential | | | | | | | | Interleave | | | | | | | |
|--------------------|-----|-----|------------|---|---|---|---|---|---|---|------------|---|---|---|---|---|---|---|
| CA2 | CA1 | CA0 | ® | ® | | | | | | | ® | ® | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 1 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0 | 1 | 0 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0 | 1 | 1 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1 | 0 | 0 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1 | 0 | 1 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1 | 1 | 0 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1 | 1 | 1 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

DEVICE OPERATION

CLOCK (CLK)

The clock input (CLK) is used as the reference for SMROM synchronous operation with square wave signal applied externally at cycle time t_{CC} . All operations are synchronized to the rising edge of the clock. The clock transition must be monotonic between VIL and VIH. During operation with CKE high, all inputs are assumed to be in valid state for the duration of set-up and hold time around positive edge of the clock.

CLOCK ENABLE (CKE)

The clock enable (CKE) gates the clock into the SMROM and is asserted high during all cycles, except power down, and clock suspend mode. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled t_{PDE} prior to valid command. In power down or clock suspend mode, if the CKE goes low synchronously with clock (set-up and hold time), the internal clock is suspended from the next clock cycle. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least " t_{PDE} " before the positive edge of CLK, the chip becomes active from the same clock edge to accept all the input commands.

NOP (No Operation)

When \overline{RAS} , \overline{CAS} and \overline{MR} are high, the SMROM performs no operation (NOP) and does not initiate any new command. The device deselect is also a NOP and is entered by asserting \overline{CS} high. \overline{CS} high disables the command decoder so that \overline{RAS} , \overline{CAS} , \overline{MR} and all the address inputs are ignored. NOP of SMROM includes precharge, refresh, and write state of SDRAM. In addition, when mode register set command is entered in the middle of normal operation, for SMROM, it's an illegal state.

MODE REGISTER SET (\overline{MR})

The mode register stores the data for controlling the various operating modes of SMROM including \overline{RAS} latency, \overline{CAS} latency, burst type and burst length. The default value of the mode register can be defined by ROM code option. The mode register is programmed by asserting low on \overline{CS} , \overline{RAS} , \overline{CAS} , and \overline{MR} and the states of the address pins A0 ~ A6 is the data written in the mode register. After mode register set command is completed, no new command can be issued for 3 clocks cycles.

WORD MODE SELECTION CONTROL

Mode selection control is decided simultaneously with column access according to \overline{WORD} pin voltage level, high level for double word mode (X32) and low level for word mode (X16).

ADDRESS DECODING

The address pins are latched by externally applying two commands. The first command, \overline{RAS} asserted low, latches the row address into the device. A second command, \overline{CAS} asserted low, subsequently latches the column address.

DQM OPERATION

The DQM is used to mask output operation and works similar to OE. The DQM masking occurs two cycles later in the read cycle, and operates synchronously with clock.

LATENCY

There is latency between when a read command is given and when data is available on the I/O buffers. The \overline{RAS} to \overline{CAS} delay is defined as the \overline{RAS} latency, and the \overline{CAS} to data delay is the \overline{CAS} latency.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row state. The burst read command is issued by asserting low on \overline{CS} and \overline{CAS} with \overline{RAS} and \overline{MR} high on the positive edge of the clock, after \overline{RAS} latency number of clock cycles from row active command. The first output appears in \overline{CAS} latency number of clock cycles after the issue of burst read command. The output goes into high-impedance at the end of the burst, unless a new burst read is initiated to keep data gapless. The burst stop command is valid during burst data out or between read command and data out. The data bus goes to Hi-Z after the \overline{CAS} latency from the burst stop command is satisfied. The burst stop command is asserted \overline{CS} , \overline{MR} low and \overline{CAS} , \overline{RAS} high or the same state as pre-charge on SDRAM. The interval between read command (column address presented) and burst stop command is one cycle minimum. The interval between the burst stop command and the next row active command is also one cycle minimum.

POWER-UP

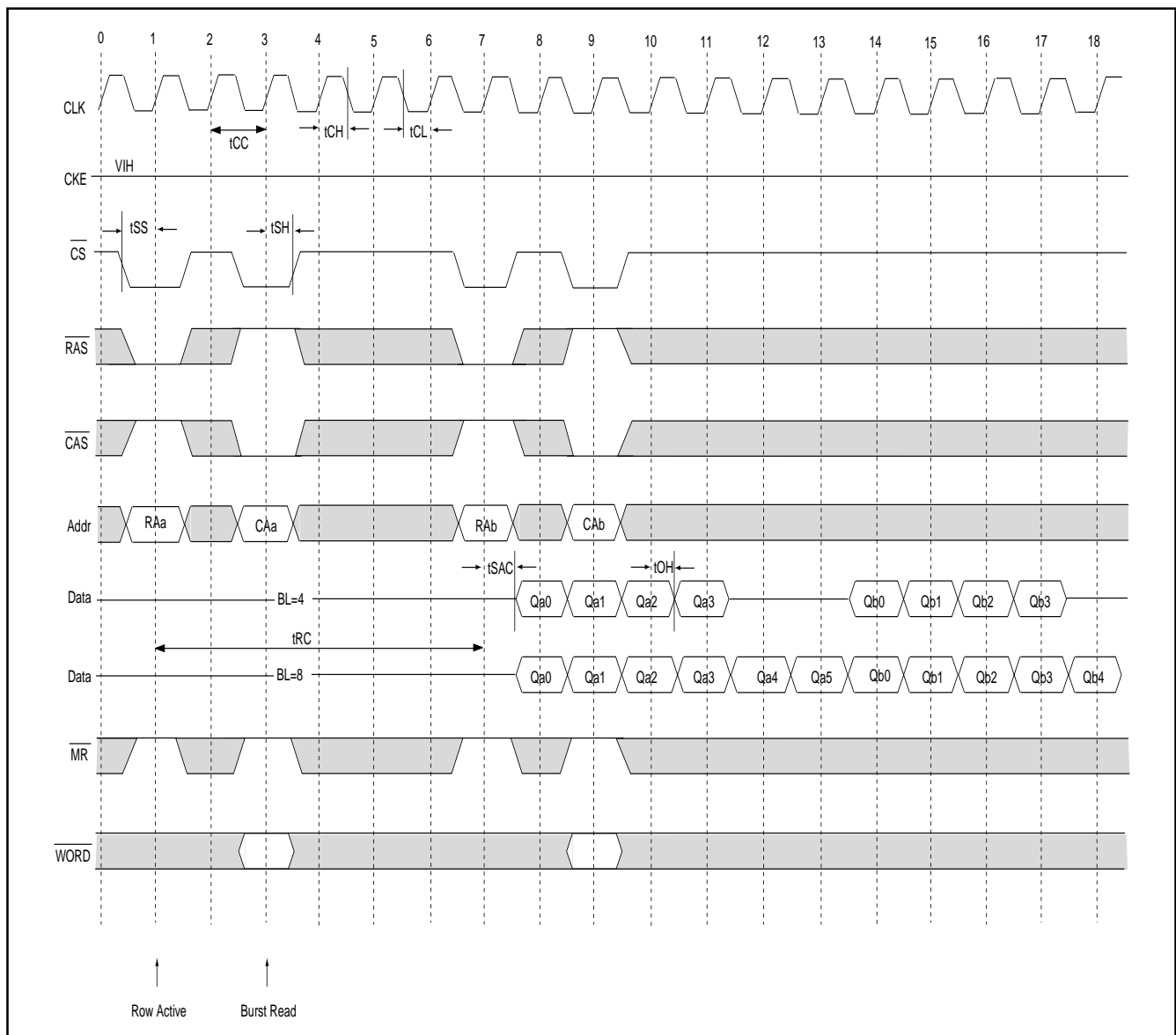
The following power-up sequence is recommended :

1. Power must be applied to either CKE and DQM inputs to pull them high and the other pins are NOP condition at the inputs to pull them high and the other pins are NOP condition at the inputs before or along with VDD and VDDQ supply .

2. Perform a mode register set cycle to program the mode value or use the default value.
3. At the end of three clock cycles from the mode register set cycle, if mode register set is active , the device is ready for power-up, all outputs will be in high impedance state. The high impedance of outputs is not guaranteed in any other power-up sequence.

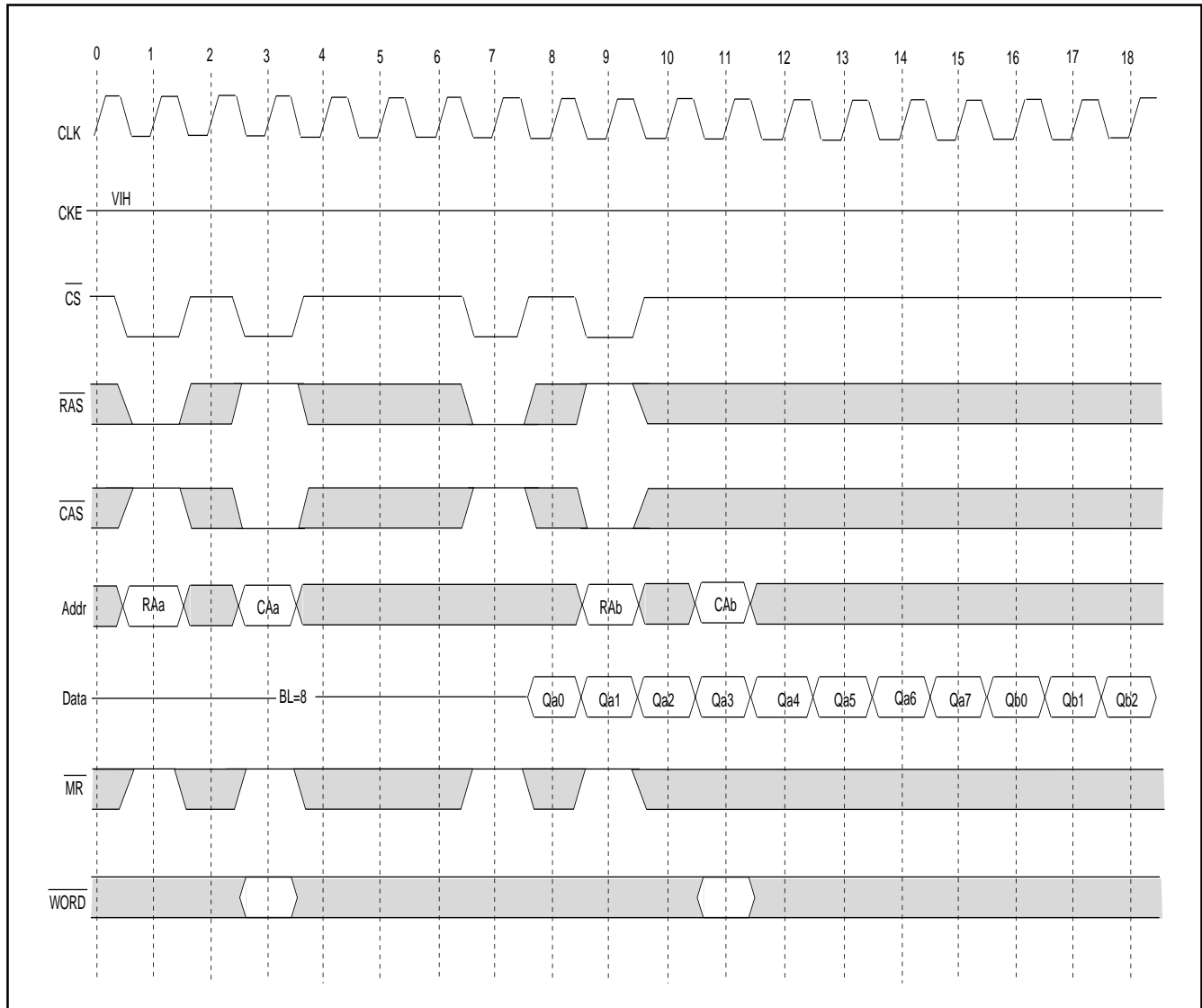
READ CYCLE 1: Normal

@RAS Latency=2, CAS Latency=5, 100MHz



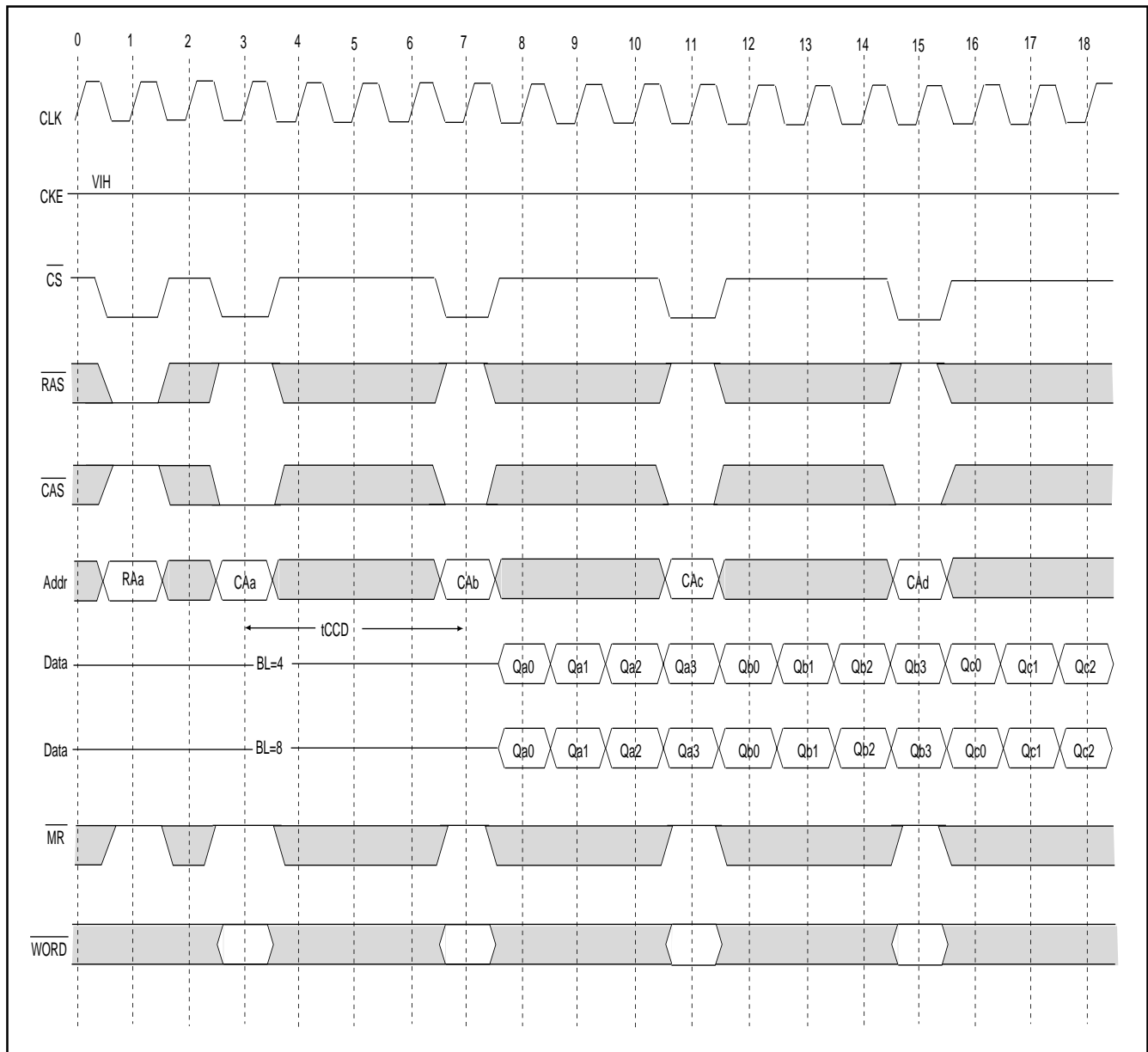
READ CYCLE 2: Normal with complete data out in BL=8

@RAS Latency=2, CAS Latency=5, 100MHz



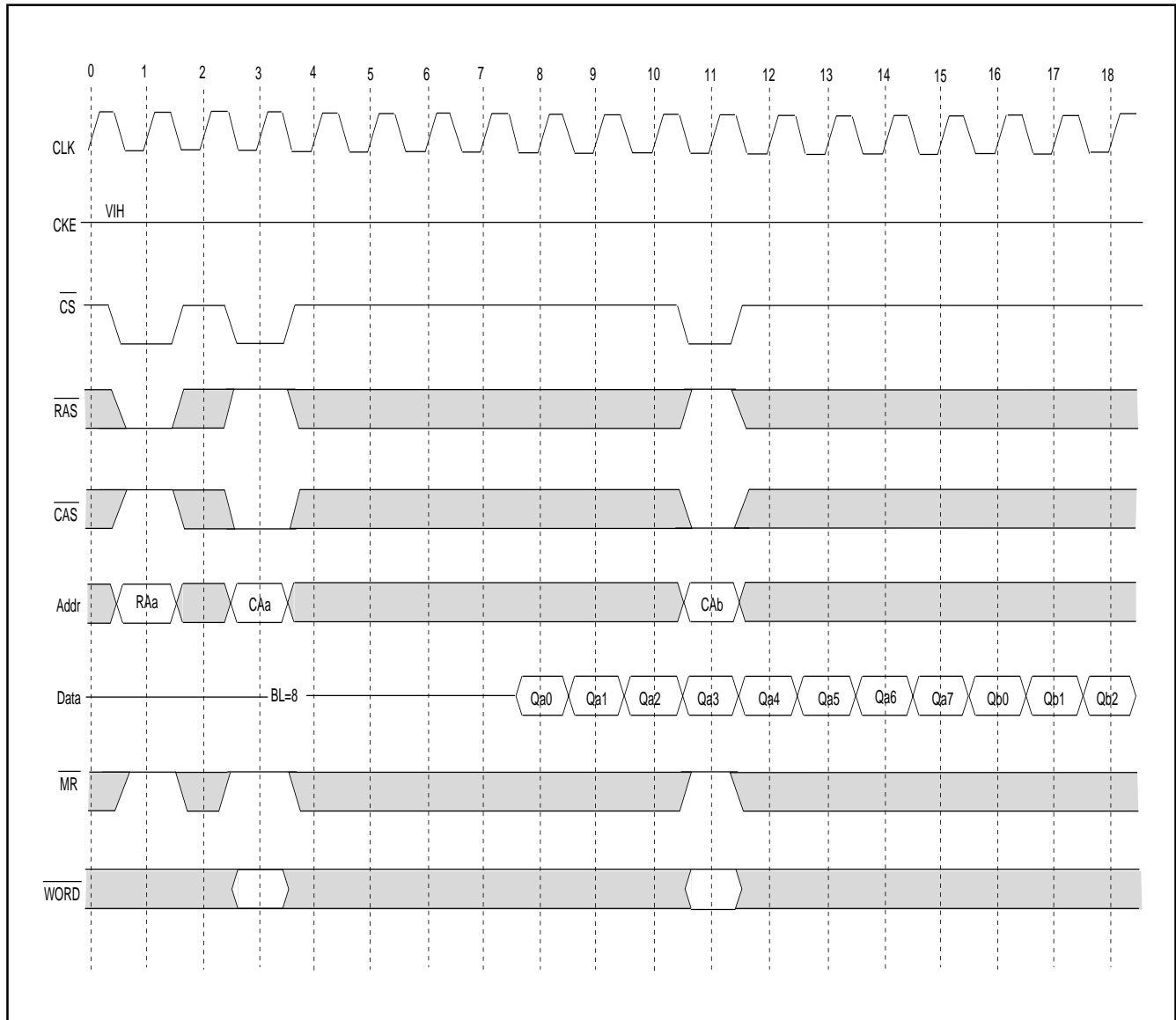
READ CYCLE 3: Consecutive Column Access

@RAS Latency=2, CAS Latency=5, 100MHz



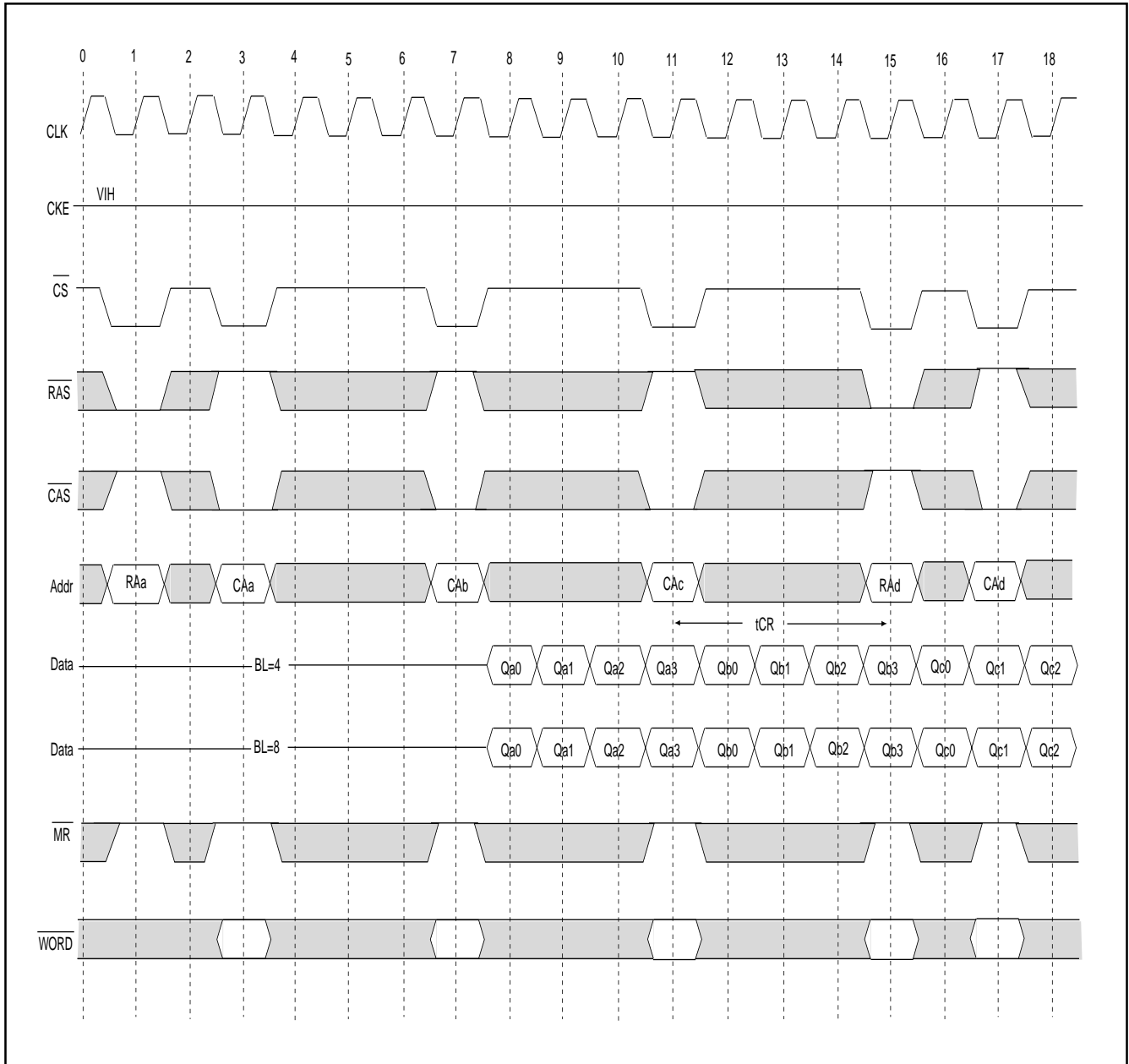
READ CYCLE 4: Consecutive Column Access with complete data out in BL=8

@RAS Latency=2, CAS Latency=5, 100MHz

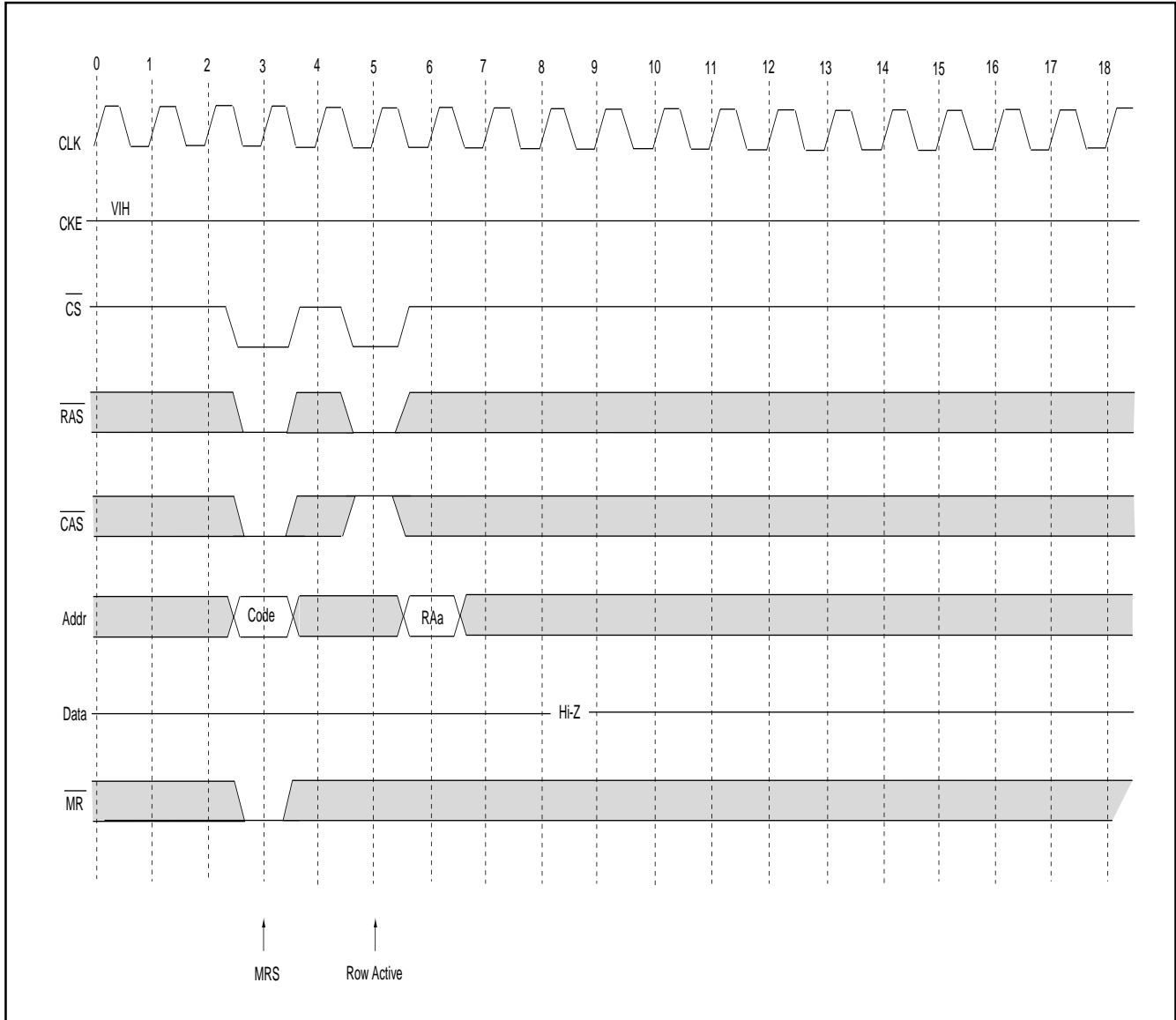


READ CYCLE 5: Consecutive Column Access to Normal Read

@RAS Latency=2, CAS Latency=5, 100MHz

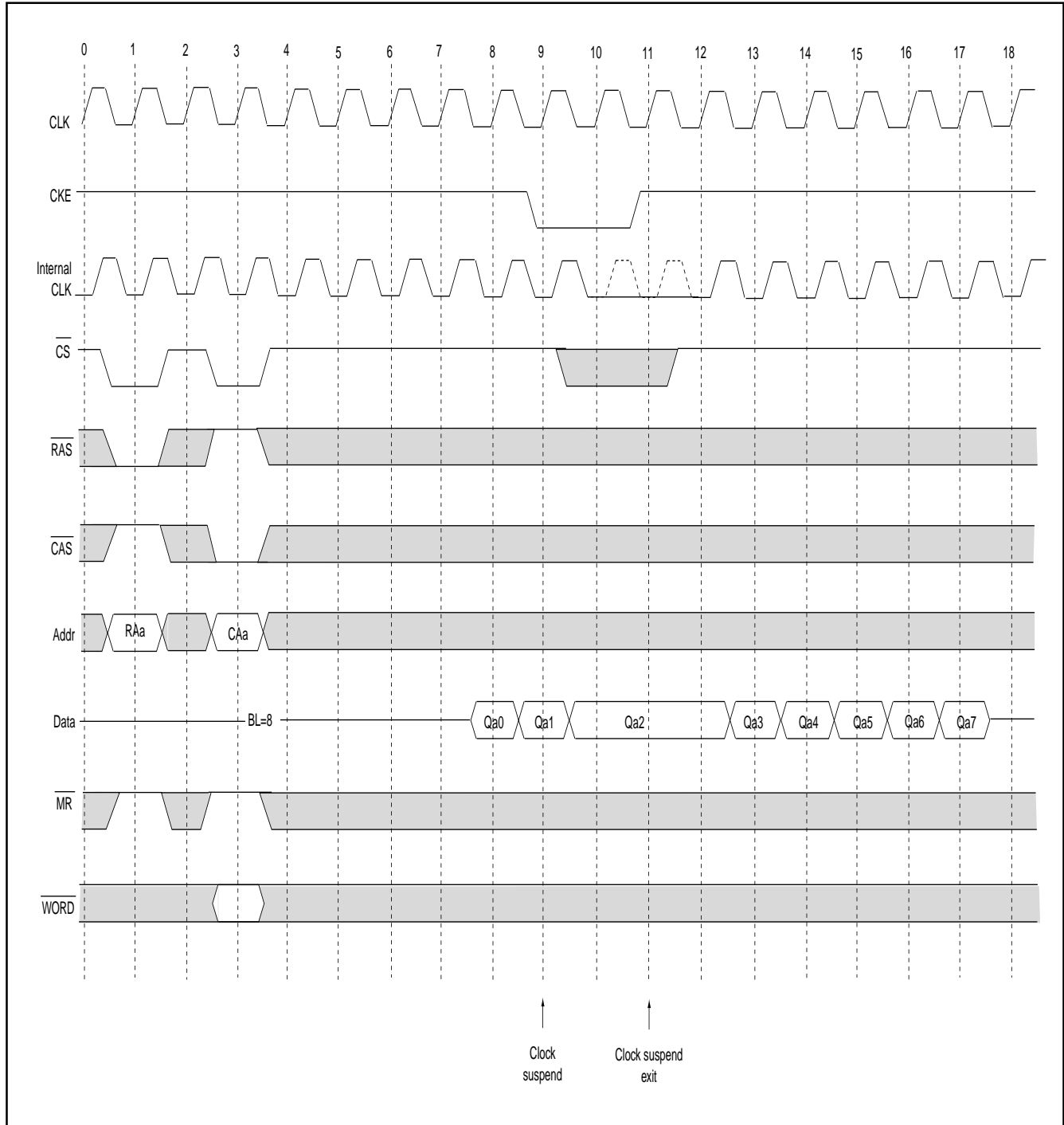


READ CYCLE 6: Mode Register Set



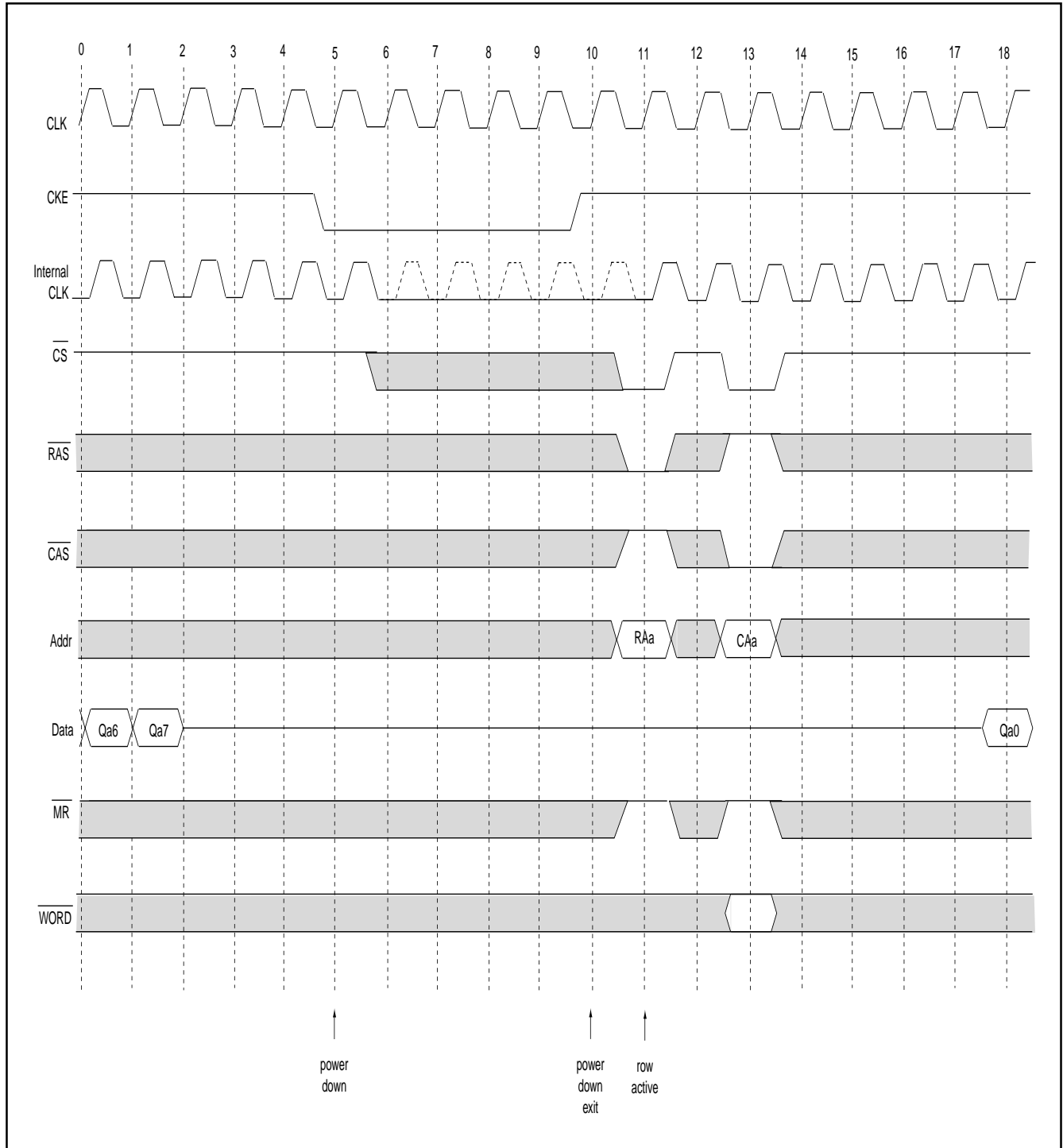
READ CYCLE 7: Clock Suspend & Clock Suspend Exit

@RAS Latency=2, CAS Latency=5, 100MHz



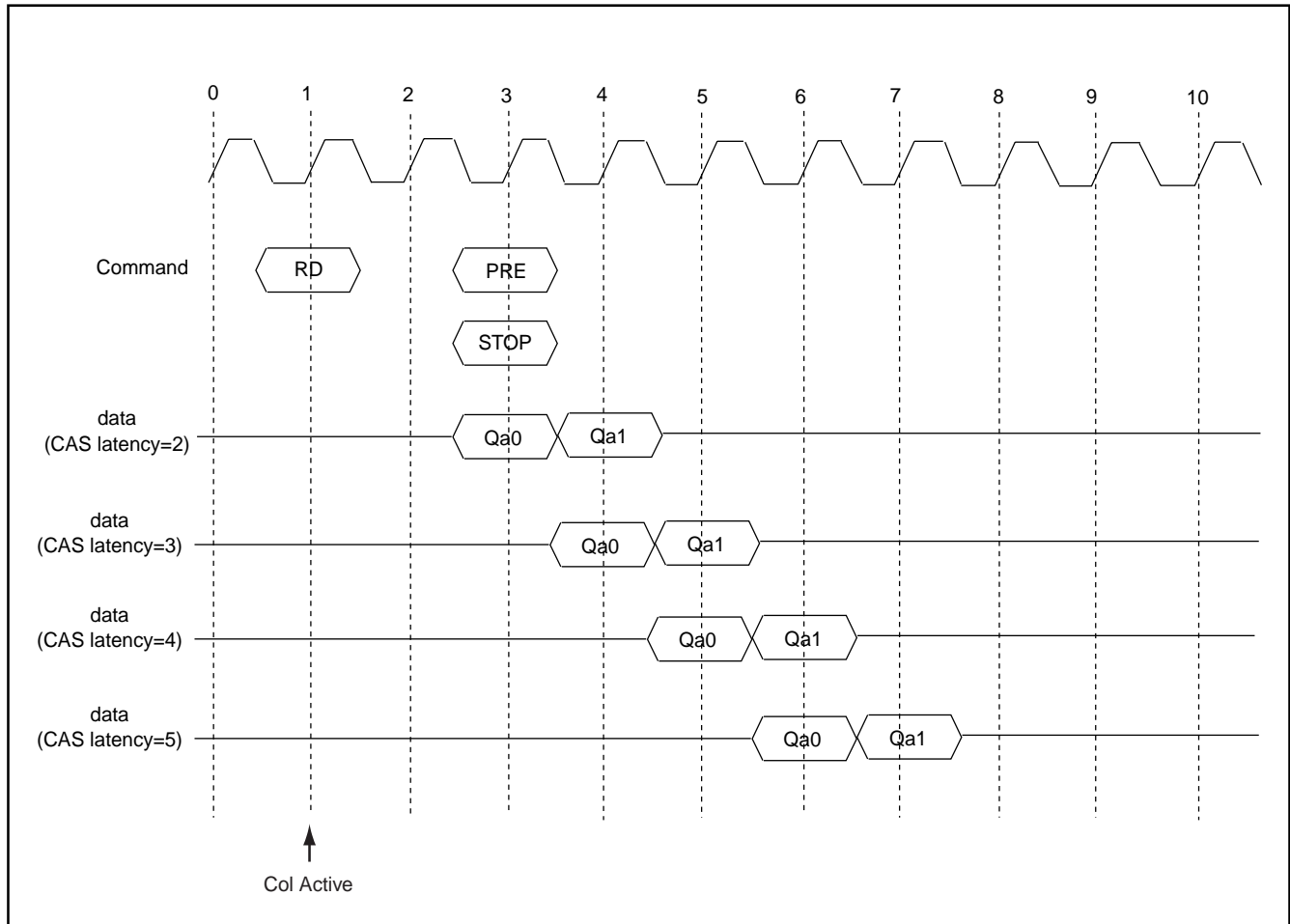
READ CYCLE 8: Power Down & Power Down Exit

@RAS Latency=2, CAS Latency=5, 100MHz

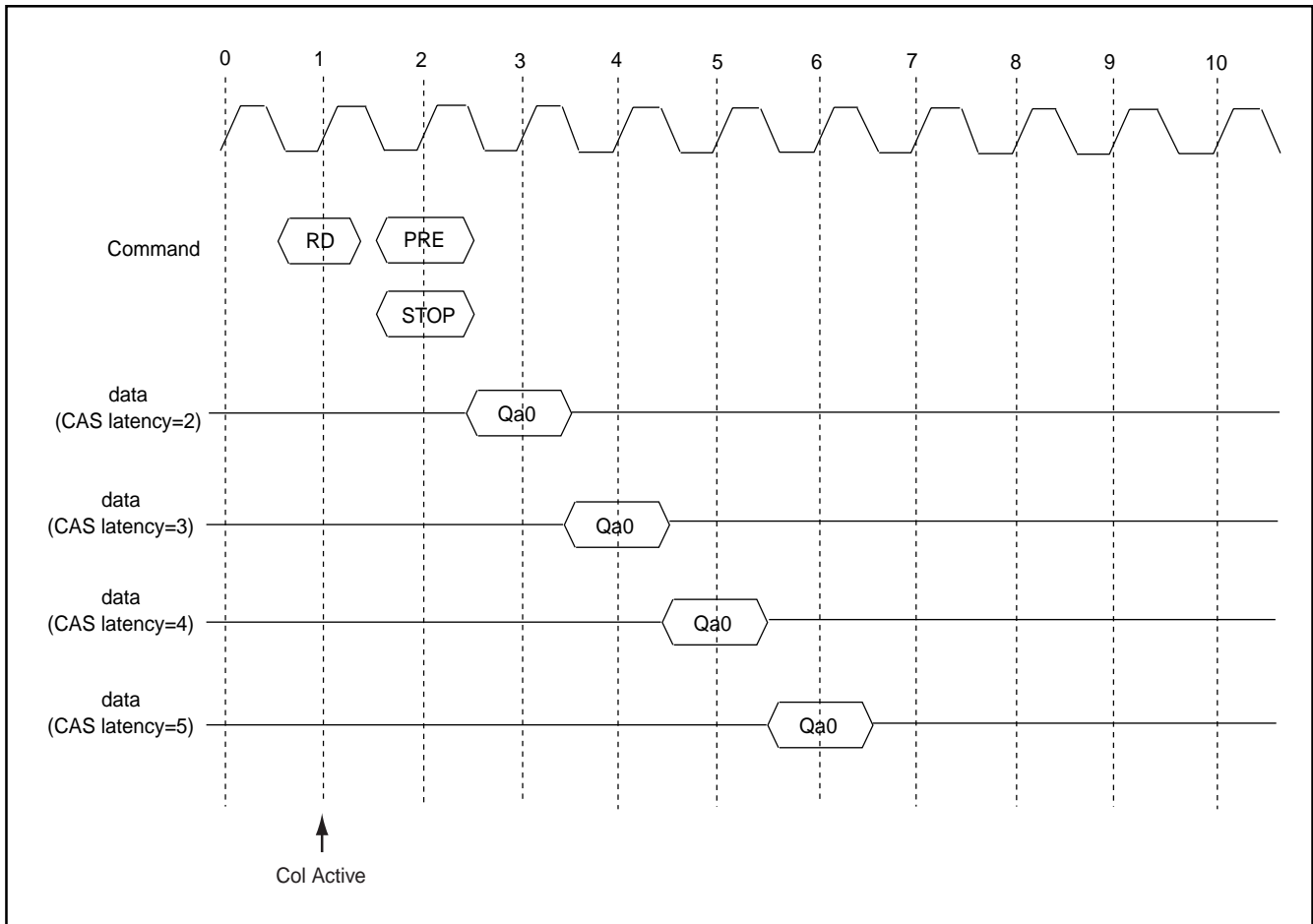


READ CYCLE 9: Burst Stop or Interrupted by Precharge

Case 1) during burst read operation

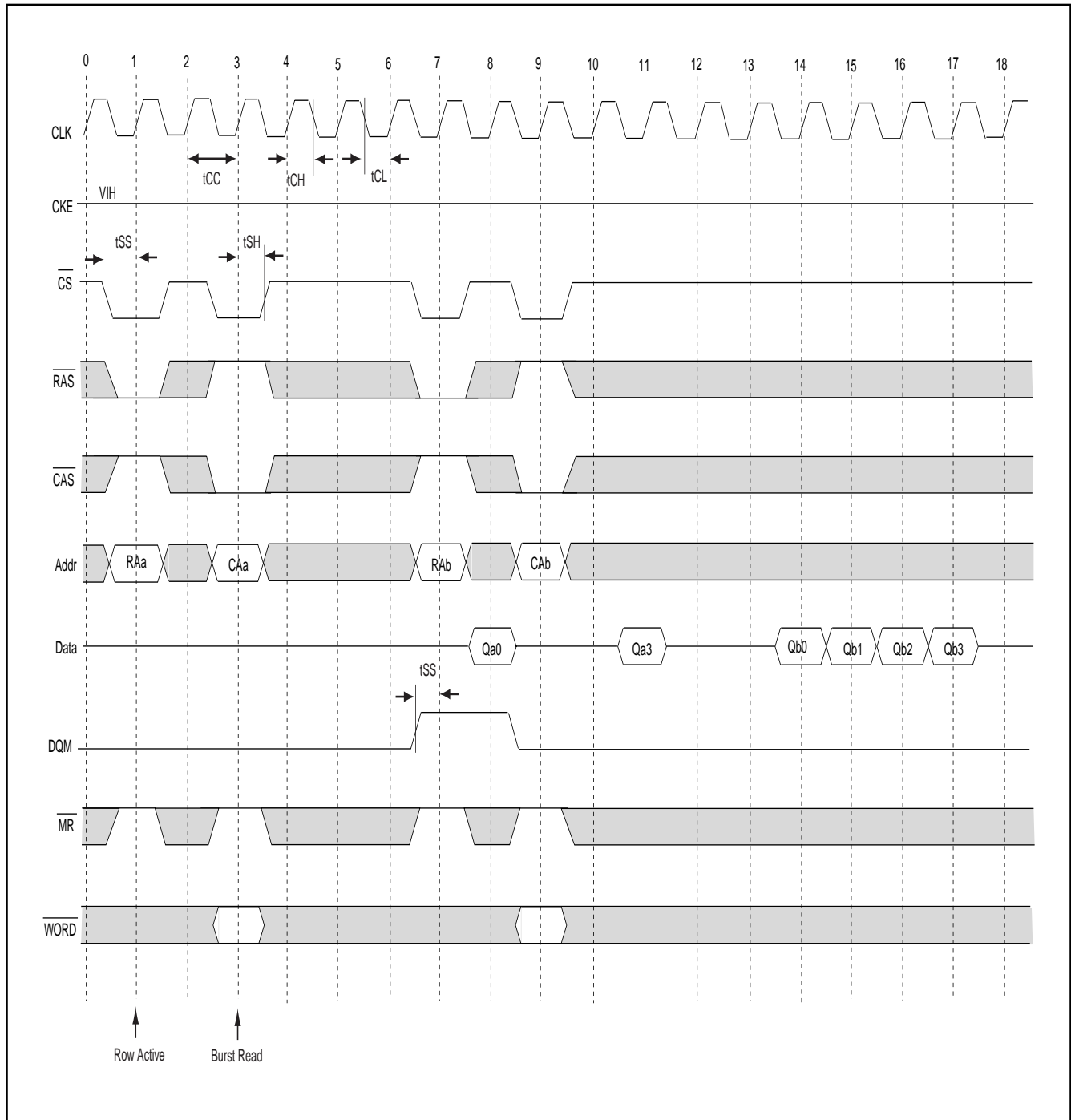


Case 2) between read command and data out



READ CYCLE 10: Normal with data masking

@ RAS Latency=2, CAS Latency=5, 100MHz





REVISION HISTORY

| REVISION | DESCRIPTION | PAGE | DATE |
|----------|---------------------------|------|-------------|
| 1.1 | To Add 100MHz Speed Grade | P1,4 | Feb/09/1999 |



MX23L6430

MACRONIX INTERNATIONAL Co., LTD.

HEADQUARTERS:

TEL:+886-3-578-8888

FAX:+886-3-578-8887

EUROPE OFFICE:

TEL:+32-2-456-8020

FAX:+32-2-456-8021

JAPAN OFFICE:

TEL:+81-44-246-9100

FAX:+81-44-246-9105

SINGAPORE OFFICE:

TEL:+65-747-2309

FAX:+65-748-4090

TAIPEI OFFICE:

TEL:+886-3-509-3300

FAX:+886-3-509-2200

MACRONIX AMERICA, INC.

TEL:+1-408-453-8088

FAX:+1-408-453-8488

CHICAGO OFFICE:

TEL:+1-847-963-1900

FAX:+1-847-963-1909

[http : //www.macronix.com](http://www.macronix.com)