



MX23L25611

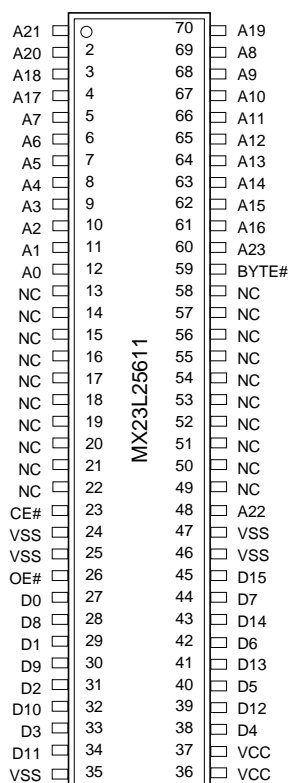
256M-BIT (16M x 16/32M x 8) MASK ROM WITH PAGE MODE (SSOP ONLY)

FEATURES

- Bit organization
 - 32M x 8 (byte mode)
 - 16M x 16 (word mode)
- Fast access time
 - Random access: 100ns (max.)
 - Page access: 30ns (max.)
- Page Size
 - 8 words per page
- Current
 - Operating: 30mA (max.) @ 5MHz
 - Standby: 15uA (max.)
- Supply voltage
 - 3.0V ~ 3.6V
- Package
 - 70 pin SSOP
- Temperature
 - 0~70°C

PIN CONFIGURATION

70 PIN SSOP



PIN DESCRIPTION

Symbol	Pin Function
A0~A23	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode) / LSB Address (Byte Mode)
CE#	Chip Enable Input
OE#	Output Enable Input
BYTE#	Word/Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

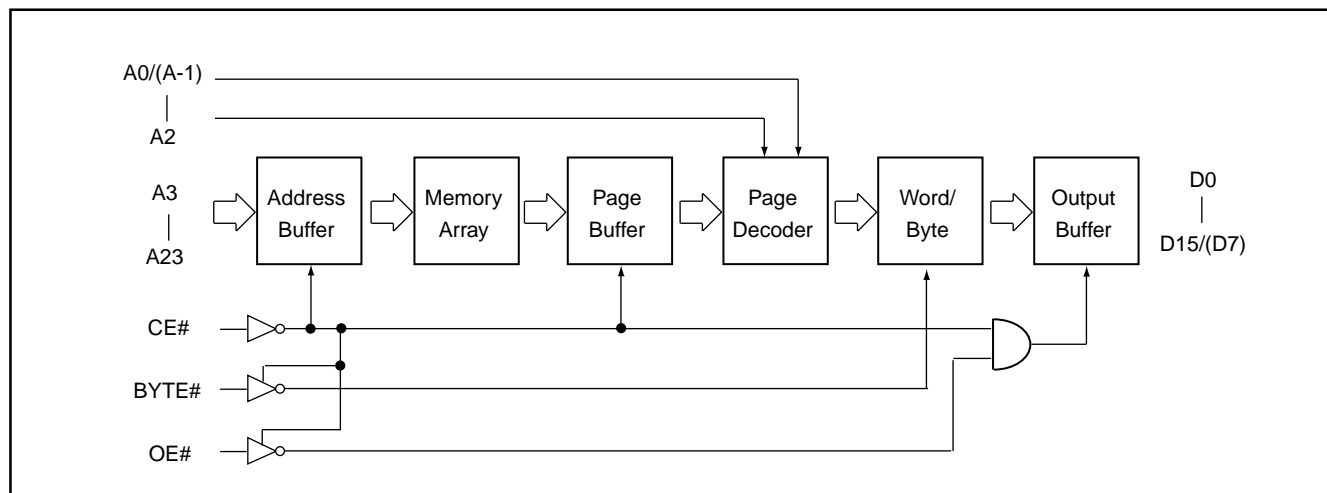
MODE SELECTION

CE#	OE#	BYTE#	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active



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BLOCK DIAGRAM



ORDER INFORMATION

Part No.	Access Time	Package	VCC
MX23L25611MC-10	100ns	70 pin SSOP	3.0V~3.6V (under development)
MX23L25611MC-12	120ns	70 pin SSOP	3.0V~3.6V (under development)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C



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DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.0V ~ 3.6V)

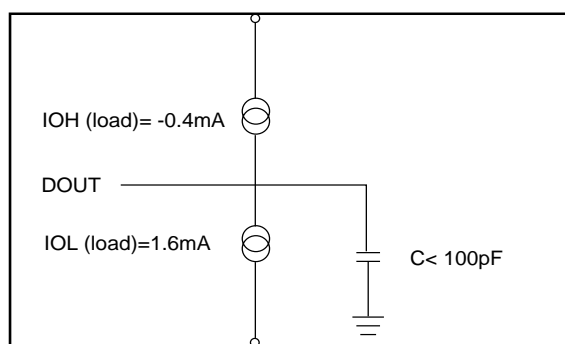
Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.2xVCC	
Input Leakage Current	ILI	-	10uA	0V, VCC
Output Leakage Current	ILO	-	10uA	0V, VCC
Operating Current	ICC	-	30mA	f=5MHz, all output open CE#=VIL(Chip Enable) OE#=VIH(Output Disabled)
Standby Current (TTL)	ISTB1	-	1mA	CE# = VIH
Standby Current (CMOS)	ISTB2	-	15uA	CE# > VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.0V ~ 3.6V)

Item	Symbol	23L25611-10		23L25611-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tCE	-	100ns	-	120ns
Page Mode Access Time	tPA	-	30ns	-	30ns
Output Enable Time	tOE	-	30ns	0	30ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

AC Test Conditions

Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure



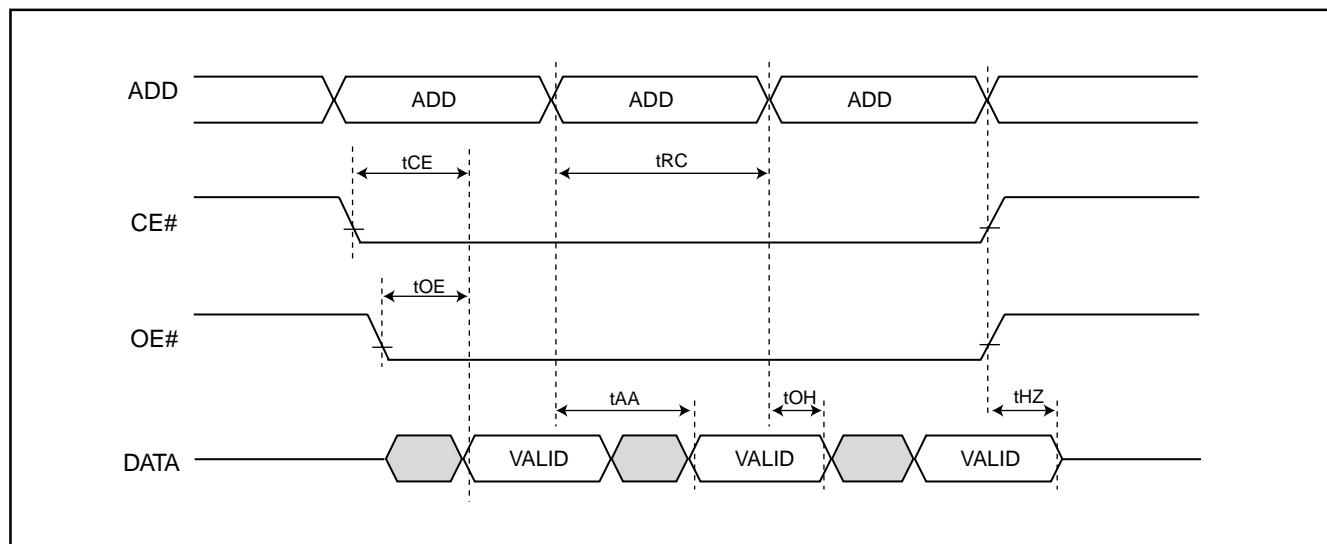
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.



TIMING DIAGRAM

RANDOM READ

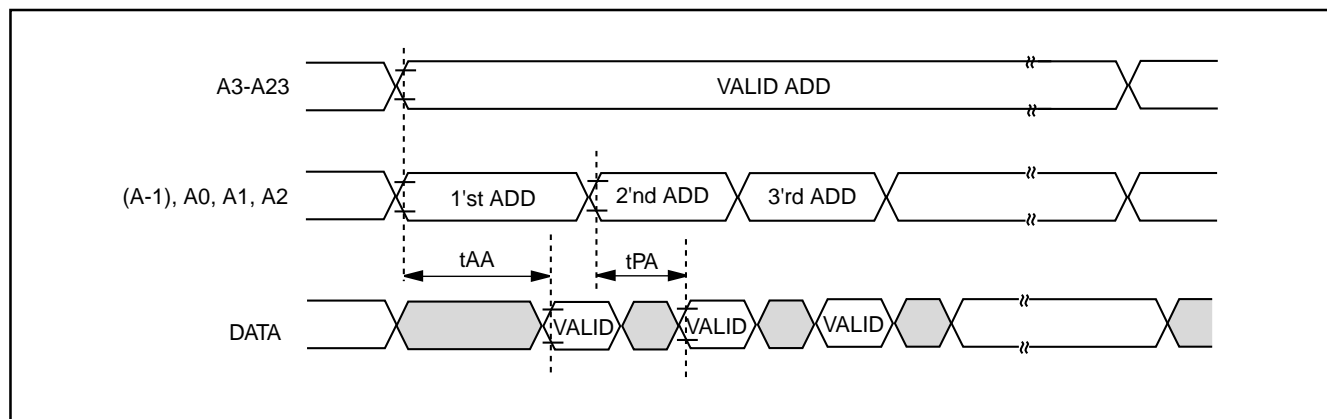


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PAGE READ

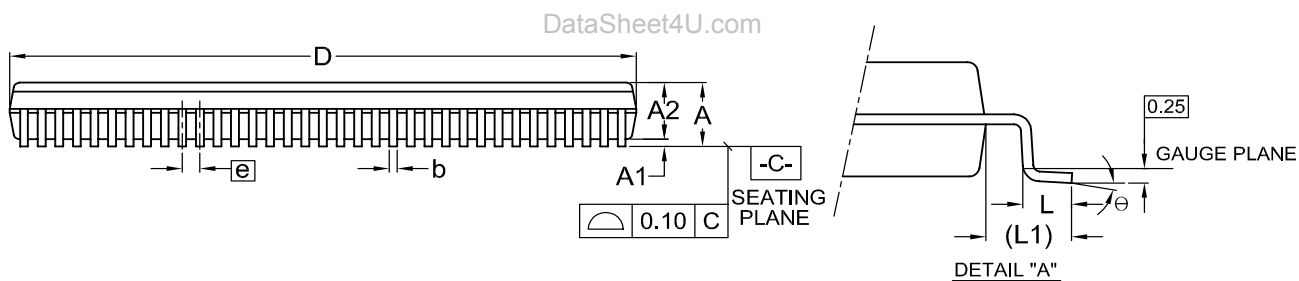
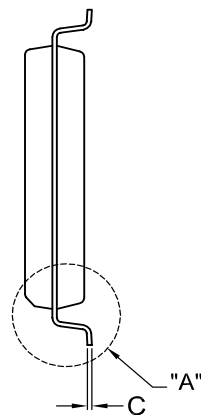
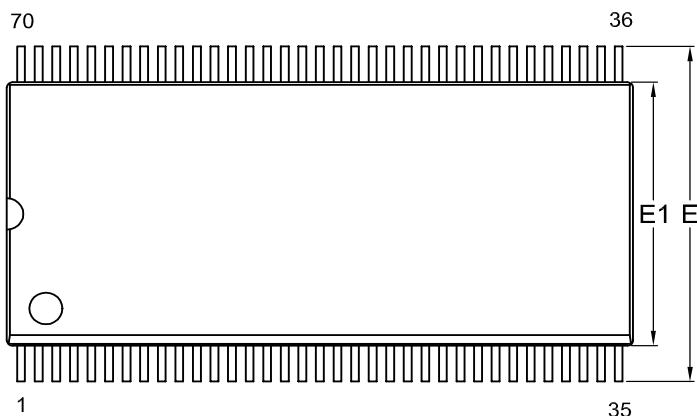
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PACKAGE INFORMATION

Title: Package Outline for SSOP 70L (500MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
UNIT													
mm	Min.	---	0.10	2.56	0.30	0.17	28.37	15.73	12.47		0.61	1.51	0
	Nom.	---	0.15	2.69	0.35	0.20	28.50	16.03	12.60	0.80	0.81	1.71	5
	Max.	3.05	0.23	2.82	0.40	0.25	28.63	16.33	12.73		1.01	1.91	10
Inch	Min.	---	0.004	0.101	0.012	0.007	1.117	0.619	0.491		0.024	0.060	0
	Nom.	---	0.006	0.106	0.014	0.008	1.122	0.631	0.496	0.031	0.032	0.068	5
	Max.	0.120	0.009	0.111	0.016	0.010	1.127	0.643	0.501		0.040	0.075	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1503	4				09-24-02



REVISION HISTORY

Revision #	Description	Page	Date
1.0	1. Changed heading as "RELIMINARY" 2. Modify Pin Configuration--Pin#6~15, Pin#24,25,68,69	P1 P1	SEP/06/2001
1.1	1. Modify Pin Configuration--Pin#10~14, 25,26	P1	SEP/07/2001
1.2	1. Modify Pin Configuration 2. Modify Operating Current:60mA-->30mA; Standby Current(CMOS):50uA-->15uA 3. Modify MODE SELECTION 4. Add 120ns in AC Characteristics 5. Add Order Informaion 6. Modify 70 pin SOP --> 70 pin SSOP	P1,2 P1 P3 P2 P1,2,5	FEB/01/2002
1.3	Modify Package Information	P5	NOV/21/2002



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