



MX23L12824

128M-BIT MASK ROM

FEATURES

- Bit organization
 - 16Mb x 8 (byte mode)
 - 8Mb x 16 (word mode)
- Fast access time
 - Random access: 120/25ns(max.) in 3.0~3.6V
 - 120/30ns(max.) in 2.7~3.6V
- Page size
 - 8 words per page
- Current
 - Operating: 50mA
 - Standby: 15uA(max.)
- Supply voltage
 - VCC : 2.7 ~ 3.6V
 - VCCQ : 2.7 ~ 3.6V
- Package
 - 64 ball mini BGA (10.0mm X 13.0mm, ball pitch 1.0mm)
- Temperature
 - -25~85° C

PIN DESCRIPTION

Symbol	Pin Function
A0~A23	Address Inputs, A0 not used in word mode
D0~D15	Data Outputs
CE0#,CE1#,CE2#	Chip Enable Input
OE#	Output Enable Input
BYTE#	Word/Byte mode Selection
VCC	Power Supply Pin
VCCQ	Output VCC Pin
GND	Ground Pin
NC	No Connection

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MODE SELECTION

CE#	OE#	BYTE#	D0~D15	D8~D15	Power
Disabled	X	X	High Z	HighZ	Stand-by
Enabled	H	X	High Z	HighZ	Active
Enabled	L	L	D0~D7	HighZ	Active
Enabled	L	H	D0~D7	D8~D15	Active

Chip Enable Truth Table

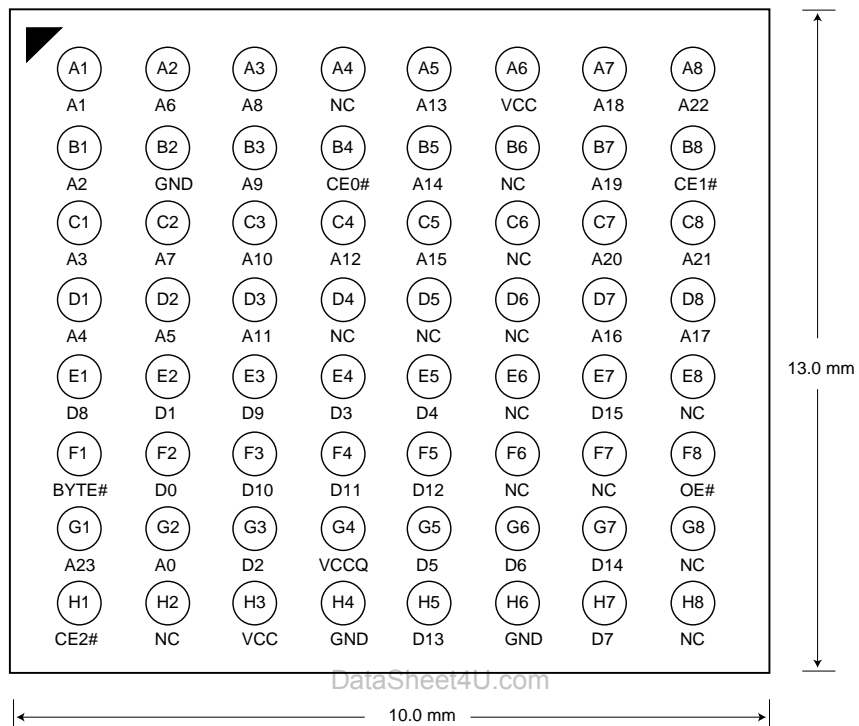
CE2#	CE1#	CE0#	DEVICE
L	L	L	Enabled
L	L	H	Disabled
L	H	L	Disabled
L	H	H	Disabled
H	L	L	Enabled
H	L	H	Enabled
H	H	L	Enabled
H	H	H	Disabled

Note: For single-chip applications, CE2#, CE1# can be strapped to GND.



PIN CONFIGURATION

64 Mini BGA (Top View, Ball Down)



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ORDER INFORMATION

Part No.	Speed	Package	Grade	Remark
MX23L12824XI-12	120ns	64 ball mini BGA	Industrial	

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	-25° C to 85° C
Storage Temperature	Tstg	-65° C to 125° C

DC CHARACTERISTICS (Ta = -25° C ~ 85° C, VCC = 2.7V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -400uA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCCQ+0.5V	
Input Low Voltage	VIL	-0.5V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC	-	50mA	f=5MHz, CE#=VIL, OE#=VIH all output open
Standby Current (CMOS)	ISTB	-	15uA	CE#>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25° C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25° C, f = 1MHZ

AC CHARACTERISTICS (Ta = -25° C ~ 85° C, VCC = 2.7V~3.6V)

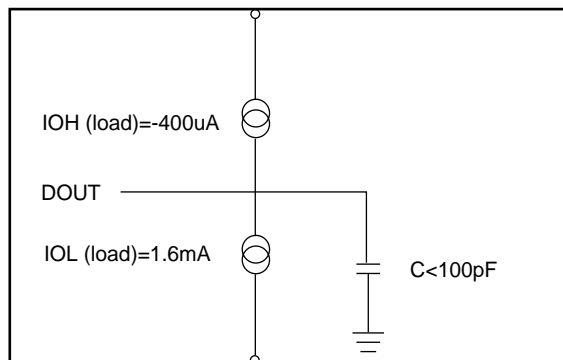
Item	Symbol	23L12824-12	
		MIN.	MAX.
Read Cycle Time	tRC	120ns	-
Address Access Time	tAA	-	120ns
Chip Enable Access Time	tACE	-	120ns
Page Access Time	tPA	-	30ns (VCC=2.7~3.6V)
		-	25ns (VCC=3.0~3.6V)
Output Enable Time	tOE	-	30ns
Output Hold After Address	tOH	0ns	-
Output High Z Delay	tHZ	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE# or CE# going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.



AC Test Conditions

Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	5ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure 100pF output load capacitance



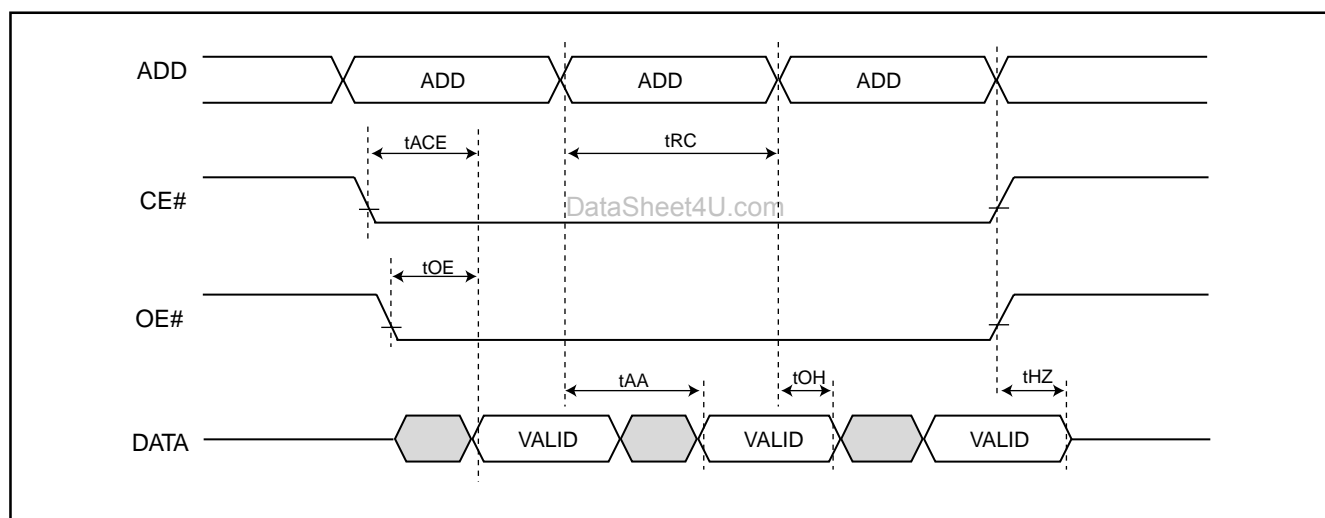
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

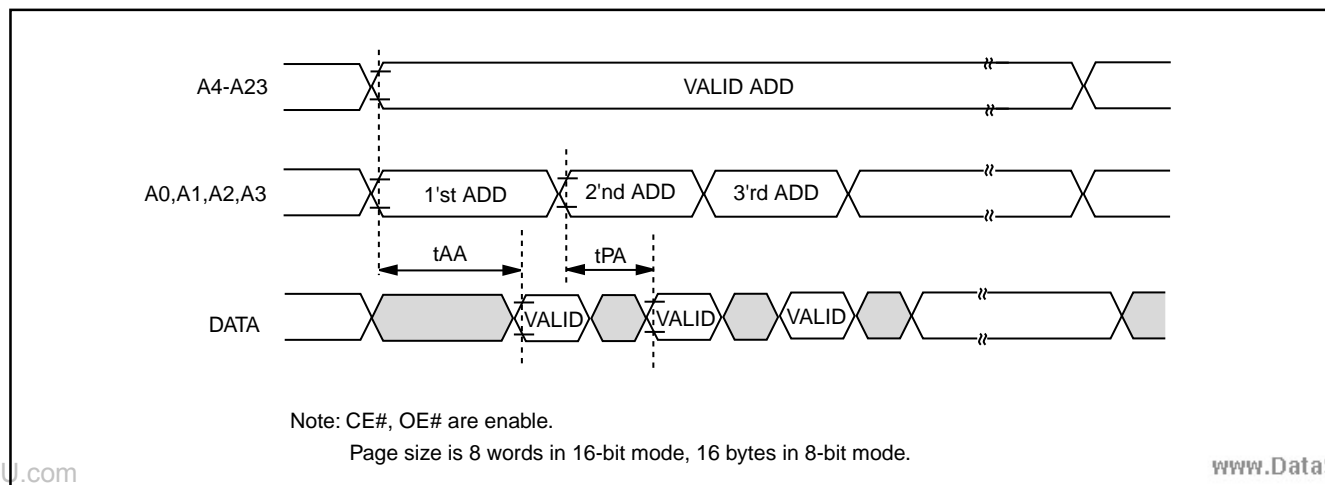
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

RANDOM READ



PAGE READ

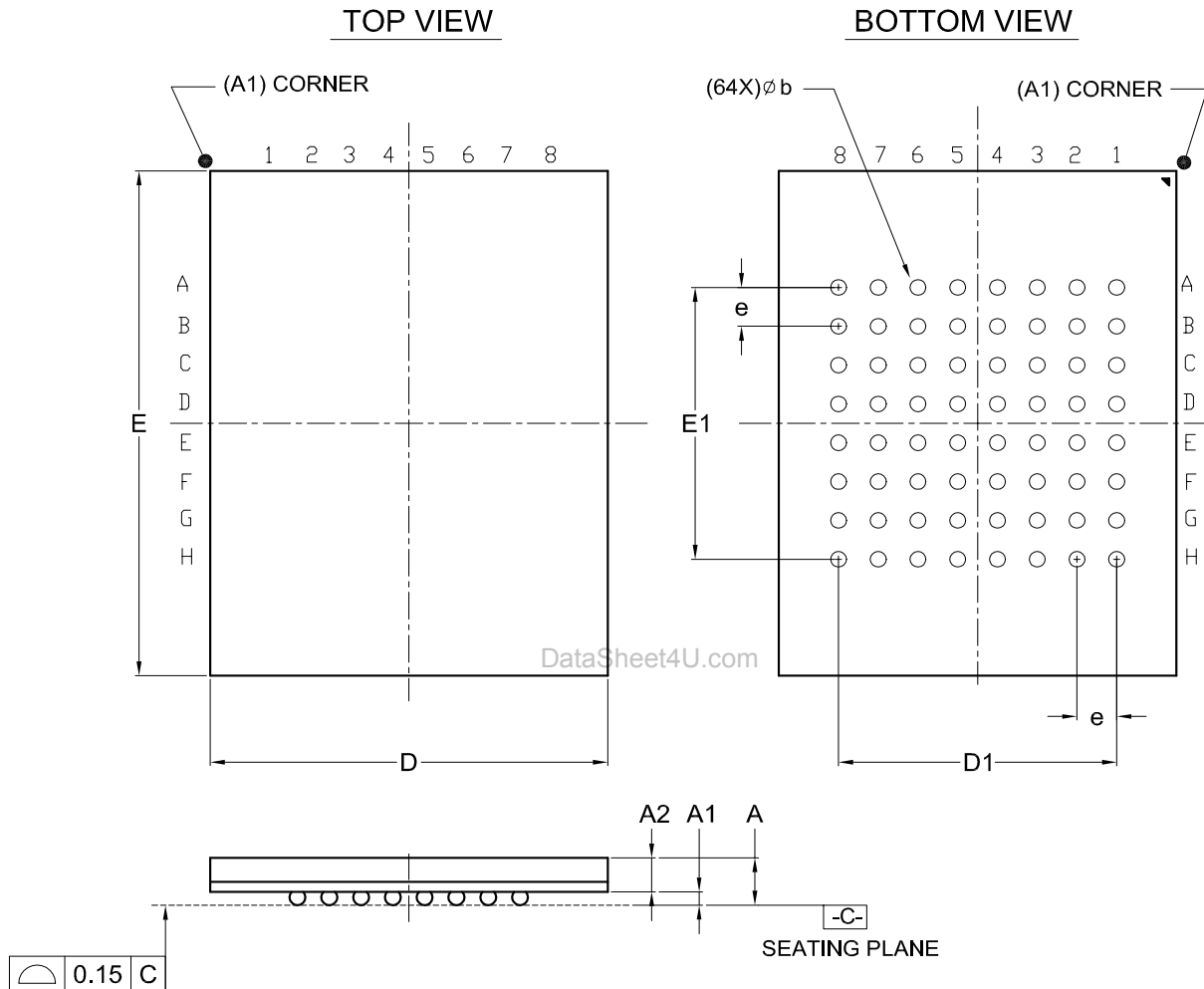




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PACKAGE INFORMATION

Title: Package Outline for CSP 64BALL(10X13X1.4MM,BALL PITCH 1.00MM,BALL DIAMETER 0.6MM)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	--	0.40	0.65	0.50	9.90		12.90		
	Nom.	--	0.50	--	0.60	10.00	7.00	13.00	7.00	1.00
	Max.	1.40	0.60	--	0.70	10.10		13.10		
Inch	Min.	--	0.016	0.026	0.020	0.390		0.508		
	Nom.	--	0.020	--	0.024	0.394	0.276	0.512	0.276	0.039
	Max.	0.055	0.024	--	0.028	0.398		0.516		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4224	3	MO-192			12-16-'03



REVISION HISTORY

Revision No.	Description	Page	Date
1.1	1. Modify page access time from 30ns to 25ns	P1,3	MAR/22/2004
1.2	1. Add tPA:25ns in 3.0~3.6V	P1,3	APR/12/2004

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