FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-20903-1E

FLASH MEMORY

CMOS

64 M (4M × 16) BIT

MirrorFlash™

MBM29PL65LM-90/10

■ DESCRIPTION

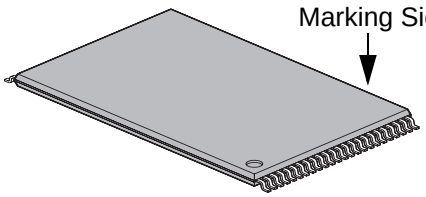
MBM29PL65LM is of 67,108,864 bit capacity +3.0 V -only Flash memory enabling word write, both across- the chip, comprehensive erase and by-the-unit, individual sector erase.
Its CMOS peripheral circuitry contributes to significant saving in power consumption even at high-speed stand-by mode operation.
MBM29PL65LM consists of 4M x 16 bit Word mode and erases 128 sectors at ever 32K word. Its package type is 48-pin TSOP.
Embedded Program Algorithm™, when executed with erase or program command sequences, automatically times the program pulse widths and verifies proper cell margin.
MBM29PL65LM, because of its capability in electrical data erase and program through write command, enables to rewrite data within the internal system. It is a truly dependable device for vast application possibilities.

■ PRODUCT LINE UP

Part No.	MBM29PL65LM-90	MBM29PL65LM-10
V_{CC}	3.0 V to 3.6 V	3.0 V to 3.6 V
V_{CCQ}	V_{CC}	V_{CC}
Max Address Access Time	90 ns	100 ns
Max $\overline{CE}$ Access Time	90 ns	100 ns
Max Page Read Access Time	25 ns	30 ns

■ PACKAGE

48-pin plastic TSOP (1)



(FPT-48P-M19)

Notes: Programming in byte mode (× 8) is prohibited.
Programming to the address that already contains data is prohibited. (It is mandatory to erase data prior to overprogram on the same address.

■ FEATURES

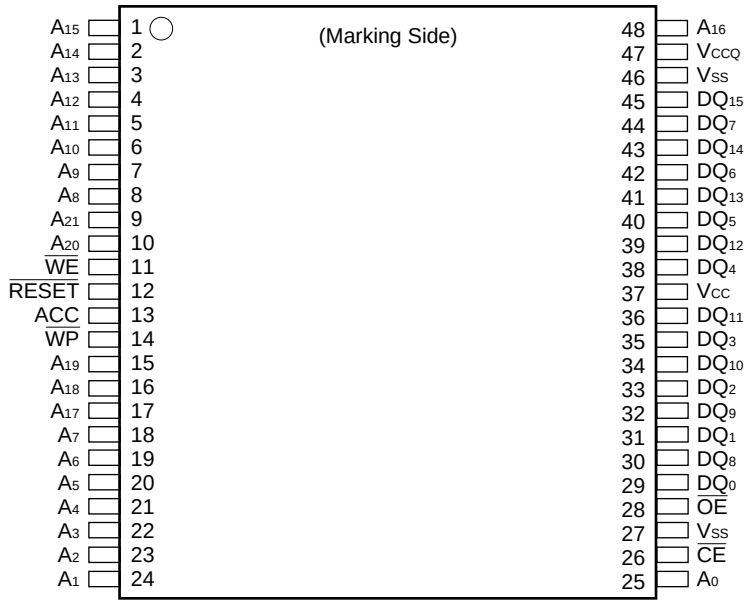
- MirrorFlash Memory™*1
- **0.23 µm Process Technology**
- 4 M × 16 bit configuration
- **Single 3.0 V read, program and erase**
- Standard 48-pin TSOP (1) (Package suffix : TN)
- **Minimum 100,000 program/erase cycles**
- **High performance Page mode** (4 words)
- **Sector erase architecture (Sectors can be grouped in any given combination.)**
  32K word sectors
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- HiddenROM Region
- Write Protect by $\overline{\text{WP}}$ pin
- **Embedded Erase™*2 Algorithms**
- **Embedded Program™*2 Algorithms**
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Automatic sleep mode**
- **Erase Suspend/Resume**
- **Low V_{CC} write inhibit**
- **Sector Group Protection**
- Extended Sector Group Protection
- Fast Program
- **Temporary sector group unprotection**
- **In accordance with CFI (Common Flash Memory Interface)**

*1 : MirrorFlash™ is a trademark of Fujitsu Limited.

*2 : Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENT

TSOP(1)

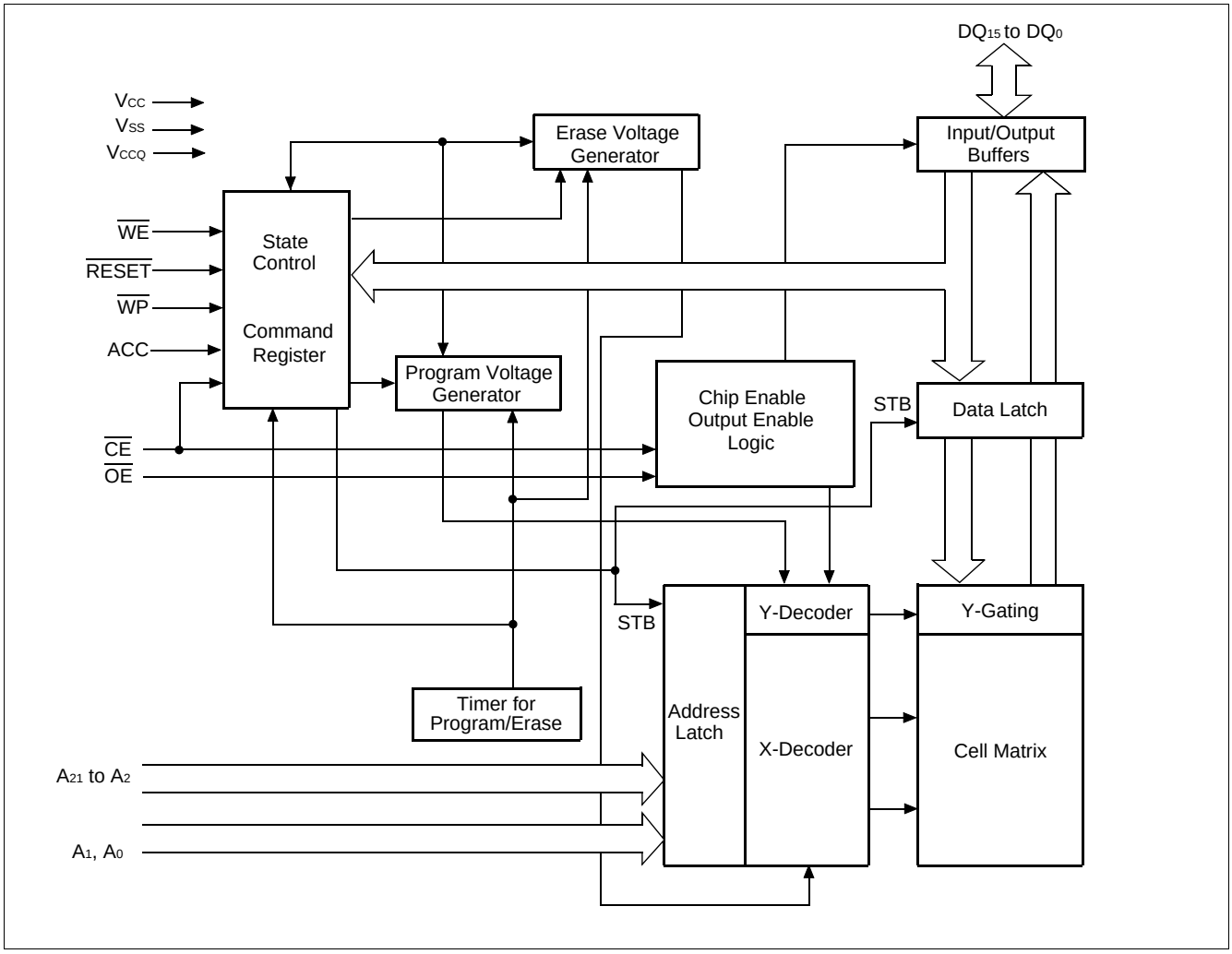


(FPT-48P-M19)

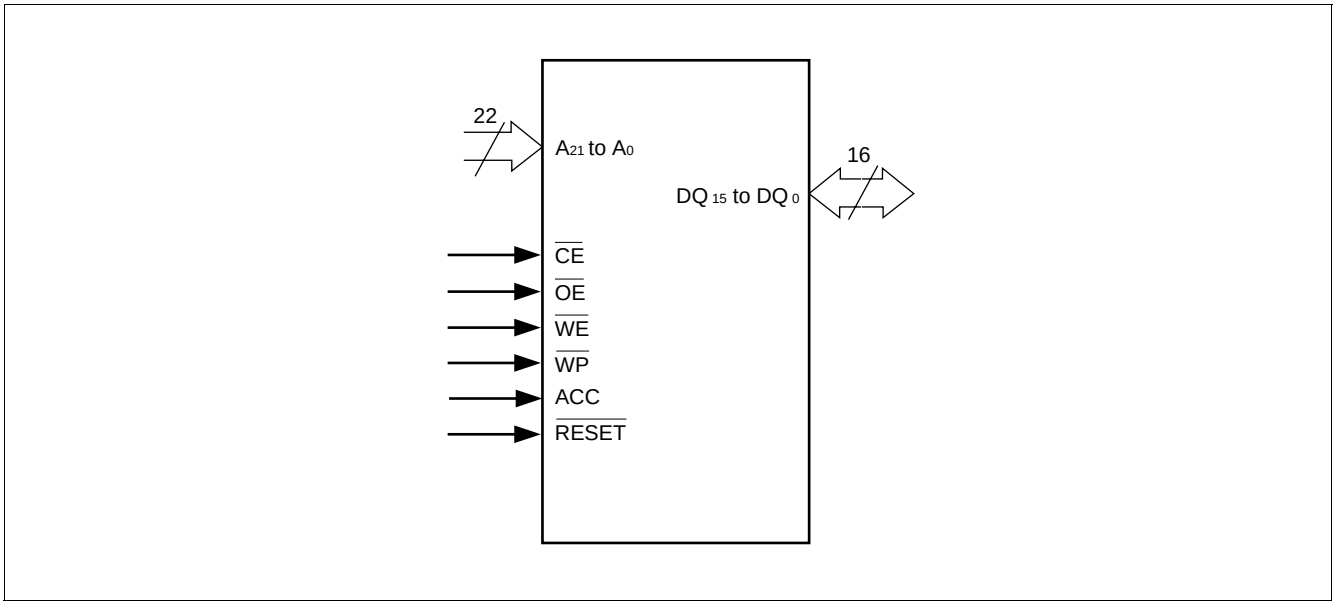
■ PIN DESCRIPTIONS

Pin Name	Function
A_{21} to A_0	Address Inputs
DQ_{15} to DQ_0	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Hardware Write Protection
ACC	Hardware Program Acceleration
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Group Unprotection
V_{CC}	Device Power Supply
V_{CCQ}	Output Power Supply
V_{SS}	Device Ground

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

MBM29PL65LM User Bus Operations Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_2	A_3	A_6	A_9	DQ_{15} to DQ_0	$\overline{RESET}$	$\overline{WP}$
Standby	H	X	X	X	X	X	X	X	X	Hi-Z	H	X
Autoselect Manufacture Code*1	L	L	H	L	L	L	L	L	V_{ID}	Code	H	X
Autoselect Device Code*1	L	L	H	H	L	L	L	L	V_{ID}	Code	H	X
Read	L	L	H	A_0	A_1	A_2	A_3	A_6	A_9	D_{OUT}	H	X
Output Disable	L	H	H	X	X	X	X	X	X	Hi-Z	H	X
Write (Program/Erase)	L	H	L	A_0	A_1	A_2	A_3	A_6	A_9	*4	H	*5
Enable Sector Group Protection*2	L	H	L	L	H	L	L	L	X	*4	V_{ID}	H
Temporary Sector Group Unprotection	X	X	X	X	X	X	X	X	X	*4	V_{ID}	H
Reset (Hardware)	X	X	X	X	X	X	X	X	X	Hi-Z	L	X
Sector Write Protection*3	X	X	X	X	X	X	X	X	X	X	H	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.
Hi-Z = High-Z, V_{ID} = 11.5 V to 12.5 V

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. See “MBM29PL65LM Standard Command Definitions”.

*2 : Refer to Sector Group Protection.

*3 : Protects the first 32K words sector (SA0).

*4 : D_{IN} or D_{OUT} as required by command sequence, data pulling, or sector protect algorithm

*5 : If $\overline{WP}$/ACC = V_{IL}, the first sector remains protected.
If $\overline{WP}$/ACC = V_{IH}, the first sector will be protected or unprotected as determined by the method specified in “Sector Group Protection” in “■ FUNCTIONAL DESCRIPTION”.

MBM29PL65LM Standard Command Definitions Table*1

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset*2	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Reset*2	3	555h	AAh	2AAh	55h	555h	F0h	RA*13	RD*13	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	555h	90h	00h*13	04h*13	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Program/Erase Suspend*3	1	XXXh	B0h	—	—	—	—	—	—	—	—	—	—
Program/Erase Resume*3	1	XXXh	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode*4	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Fast Program*4	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode*5	2	XXXh	90h	XXXh	00h*12	—	—	—	—	—	—	—	—
Write to Buffer	20	555h	AAh	2AAh	55h	SA	25h	SA	0Fh	PA	PD	WBL	PD
Program Buffer to Flash (Confirm)	1	SA	29h	—	—	—	—	—	—	—	—	—	—
Write to Buffer Abort Reset*6	3	555h	AAh	2AAh	55h	555h	F0h	—	—	—	—	—	—
Extended Sector Group Protection*7,*8	4	XXXh	60h	SGA	60h	SGA	40h	SGA*13	SD*13	—	—	—	—
Query*9	1	55h	98h	—	—	—	—	—	—	—	—	—	—
HiddenROM Entry*10	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
HiddenROM Program *10,*11	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
HiddenROM Exit*11	4	555h	AAh	2AAh	55h	555h	90h	XXXh	00h	—	—	—	—

RA = Address of the memory location to be read.
PA = Address of the memory location to be programmed Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be erased. The combination of A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16} and A_{15} will uniquely select any sector. See “Sector Address Table”
SGA = Sector Group Address to be protected. See “Sector Group Address Table”. Specify SGA which constitutes from A_{21} to A_{17} and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0).
RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
WBL = Write Buffer Location
HRA = Address of the HiddenROM area ; 000000h to 00007Fh

*1 : The command combinations not described in “MBM29PL65LM Standard Command Definitions” are illegal.

*2 : Both of these reset commands are equivalent except for "Write to Buffer Abort" reset.

*3 : The Erase Suspend and Erase Resume command are valid only during a sector erase operation.

*4 : The Set to Fast Mode command is required prior to the Fast Program command.

*5 : The Reset from Fast Mode command is required to return to the read mode when the device is in fast mode.

*6 : Reset to the read mode. The Write to Buffer Abort Reset command is required after the Write to Buffer operation was aborted.

*7 : This command is valid while $\overline{RESET} = V_{ID}$.

*8 : Sector Group Address (SGA) with $A_6 = 0$, $A_3 = 0$, $A_2 = 0$, $A_1 = 1$, and $A_0 = 0$

*9 : The valid address are A_6 to A_0.

*10 : The HiddenROM Entry command is required prior to the HiddenROM programming.

*11 : This command is valid during HiddenROM mode.

*12 : The data “F0h” is also acceptable.

*13 : Indicates read cycle.

Notes : • X = “H” or “L”
• Bus operations are defined in “User Bus Operations Table”.

Autoselect Codes Table

Type	A_{21} to A_{17}	A_6	A_3	A_2	A_1	A_0	Code (HEX)
Manufacturer’s Code	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh
Extended Device Code*1	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	2213h
	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	2201h
Sector Group Protection*3	Sector Group Address	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	*2

*1 : At Word mode, a read cycle at address 01h outputs device code. When 227Eh is output, it indicates that reading two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of 0Eh, as well as at 0Fh.

*2 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*3 : Given $\overline{CE}$ = Fix, wait for one cycle after the rising edge of WE (the last write command), then indicate SGA as (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0).

Sector Address Table

Sector	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector Size (Kwords)	Address Range
SA0	0	0	0	0	0	0	0	32	000000h to 007FFFh
SA1	0	0	0	0	0	0	1	32	008000h to 00FFFFh
SA2	0	0	0	0	0	1	0	32	010000h to 017FFFh
SA3	0	0	0	0	0	1	1	32	018000h to 01FFFFh
SA4	0	0	0	0	1	0	0	32	020000h to 027FFFh
SA5	0	0	0	0	1	0	1	32	028000h to 02FFFFh
SA6	0	0	0	0	1	1	0	32	030000h to 037FFFh
SA7	0	0	0	0	1	1	1	32	038000h to 03FFFFh
SA8	0	0	0	1	0	0	0	32	040000h to 047FFFh
SA9	0	0	0	1	0	0	1	32	048000h to 04FFFFh
SA10	0	0	0	1	0	1	0	32	050000h to 057FFFh
SA11	0	0	0	1	0	1	1	32	058000h to 05FFFFh
SA12	0	0	0	1	1	0	0	32	060000h to 067FFFh
SA13	0	0	0	1	1	0	1	32	068000h to 06FFFFh
SA14	0	0	0	1	1	1	0	32	070000h to 077FFFh
SA15	0	0	0	1	1	1	1	32	078000h to 07FFFFh
SA16	0	0	1	0	0	0	0	32	080000h to 087FFFh
SA17	0	0	1	0	0	0	1	32	088000h to 08FFFFh
SA18	0	0	1	0	0	1	0	32	090000h to 097FFFh
SA19	0	0	1	0	0	1	1	32	098000h to 09FFFFh
SA20	0	0	1	0	1	0	0	32	0A0000h to 0A7FFFh
SA21	0	0	1	0	1	0	1	32	0A8000h to 0AFFFFh
SA22	0	0	1	0	1	1	0	32	0B0000h to 0B7FFFh
SA23	0	0	1	0	1	1	1	32	0B8000h to 0BFFFFh
SA24	0	0	1	1	0	0	0	32	0C0000h to 0C7FFFh
SA25	0	0	1	1	0	0	1	32	0C8000h to 0CFFFFh
SA26	0	0	1	1	0	1	0	32	0D0000h to 0D7FFFh
SA27	0	0	1	1	0	1	1	32	0D8000h to 0DFFFFh
SA28	0	0	1	1	1	0	0	32	0E0000h to 0E7FFFh
SA29	0	0	1	1	1	0	1	32	0E8000h to 0EFFFFh
SA30	0	0	1	1	1	1	0	32	0F0000h to 0F7FFFh

(Continued)

Sector	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector Size (Kwords)	Address Range
SA31	0	0	1	1	1	1	1	32	0F8000h to 0FFFFFh
SA32	0	1	0	0	0	0	0	32	100000h to 107FFFh
SA33	0	1	0	0	0	0	1	32	108000h to 10FFFFh
SA34	0	1	0	0	0	1	0	32	110000h to 117FFFh
SA35	0	1	0	0	0	1	1	32	118000h to 11FFFFh
SA36	0	1	0	0	1	0	0	32	120000h to 127FFFh
SA37	0	1	0	0	1	0	1	32	128000h to 12FFFFh
SA38	0	1	0	0	1	1	0	32	130000h to 137FFFh
SA39	0	1	0	0	1	1	1	32	138000h to 13FFFFh
SA40	0	1	0	1	0	0	0	32	140000h to 147FFFh
SA41	0	1	0	1	0	0	1	32	148000h to 14FFFFh
SA42	0	1	0	1	0	1	0	32	150000h to 157FFFh
SA43	0	1	0	1	0	1	1	32	158000h to 15FFFFh
SA44	0	1	0	1	1	0	0	32	160000h to 167FFFh
SA45	0	1	0	1	1	0	1	32	168000h to 16FFFFh
SA46	0	1	0	1	1	1	0	32	170000h to 177FFFh
SA47	0	1	0	1	1	1	1	32	178000h to 17FFFFh
SA48	0	1	1	0	0	0	0	32	180000h to 187FFFh
SA49	0	1	1	0	0	0	1	32	188000h to 18FFFFh
SA50	0	1	1	0	0	1	0	32	190000h to 197FFFh
SA51	0	1	1	0	0	1	1	32	198000h to 19FFFFh
SA52	0	1	1	0	1	0	0	32	1A0000h to 1A7FFFh
SA53	0	1	1	0	1	0	1	32	1A8000h to 1AFFFFh
SA54	0	1	1	0	1	1	0	32	1B0000h to 1B7FFFh
SA55	0	1	1	0	1	1	1	32	1B8000h to 1BFFFFh
SA56	0	1	1	1	0	0	0	32	1C0000h to 1C7FFFh
SA57	0	1	1	1	0	0	1	32	1C8000h to 1CFFFFh
SA58	0	1	1	1	0	1	0	32	1D0000h to 1D7FFFh
SA59	0	1	1	1	0	1	1	32	1D8000h to 1DFFFFh
SA60	0	1	1	1	1	0	0	32	1E0000h to 1E7FFFh
SA61	0	1	1	1	1	0	1	32	1E8000h to 1EFFFFh
SA62	0	1	1	1	1	1	0	32	1F0000h to 1F7FFFh

(Continued)

Sector	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector Size (Kwords)	Address Range
SA63	0	1	1	1	1	1	1	32	1F8000h to 1FFFFFh
SA64	1	0	0	0	0	0	0	32	200000h to 207FFFh
SA65	1	0	0	0	0	0	1	32	208000h to 20FFFFh
SA66	1	0	0	0	0	1	0	32	210000h to 217FFFh
SA67	1	0	0	0	0	1	1	32	218000h to 21FFFFh
SA68	1	0	0	0	1	0	0	32	220000h to 227FFFh
SA69	1	0	0	0	1	0	1	32	228000h to 22FFFFh
SA70	1	0	0	0	1	1	0	32	230000h to 237FFFh
SA71	1	0	0	0	1	1	1	32	238000h to 23FFFFh
SA72	1	0	0	1	0	0	0	32	240000h to 247FFFh
SA73	1	0	0	1	0	0	1	32	248000h to 24FFFFh
SA74	1	0	0	1	0	1	0	32	250000h to 257FFFh
SA75	1	0	0	1	0	1	1	32	258000h to 25FFFFh
SA76	1	0	0	1	1	0	0	32	260000h to 267FFFh
SA77	1	0	0	1	1	0	1	32	268000h to 26FFFFh
SA78	1	0	0	1	1	1	0	32	270000h to 277FFFh
SA79	1	0	0	1	1	1	1	32	278000h to 27FFFFh
SA80	1	0	1	0	0	0	0	32	280000h to 287FFFh
SA81	1	0	1	0	0	0	1	32	288000h to 28FFFFh
SA82	1	0	1	0	0	1	0	32	290000h to 297FFFh
SA83	1	0	1	0	0	1	1	32	298000h to 29FFFFh
SA84	1	0	1	0	1	0	0	32	2A0000h to 2A7FFFh
SA85	1	0	1	0	1	0	1	32	2A8000h to 2AFFFFh
SA86	1	0	1	0	1	1	0	32	2B0000h to 2B7FFFh
SA87	1	0	1	0	1	1	1	32	2B8000h to 2BFFFFh
SA88	1	0	1	1	0	0	0	32	2C0000h to 2C7FFFh
SA89	1	0	1	1	0	0	1	32	2C8000h to 2CFFFFh
SA90	1	0	1	1	0	1	0	32	2D0000h to 2D7FFFh
SA91	1	0	1	1	0	1	1	32	2D8000h to 2DFFFFh
SA92	1	0	1	1	1	0	0	32	2E0000h to 2EE7FFh
SA93	1	0	1	1	1	0	1	32	2E8000h to 2EFFFFh
SA94	1	0	1	1	1	1	0	32	2F0000h to 2F7FFFh

(Continued)

(Continued)

Sector	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	Sector Size (Kwords)	Address Range
SA95	1	0	1	1	1	1	1	32	2F8000h to 2FFFFFh
SA96	1	1	0	0	0	0	0	32	300000h to 307FFFh
SA97	1	1	0	0	0	0	1	32	308000h to 30FFFFh
SA98	1	1	0	0	0	1	0	32	310000h to 317FFFh
SA99	1	1	0	0	0	1	1	32	318000h to 31FFFFh
SA100	1	1	0	0	1	0	0	32	320000h to 327FFFh
SA101	1	1	0	0	1	0	1	32	328000h to 32FFFFh
SA102	1	1	0	0	1	1	0	32	330000h to 337FFFh
SA103	1	1	0	0	1	1	1	32	338000h to 33FFFFh
SA104	1	1	0	1	0	0	0	32	340000h to 347FFFh
SA105	1	1	0	1	0	0	1	32	348000h to 34FFFFh
SA106	1	1	0	1	0	1	0	32	350000h to 357FFFh
SA107	1	1	0	1	0	1	1	32	358000h to 35FFFFh
SA108	1	1	0	1	1	0	0	32	360000h to 367FFFh
SA109	1	1	0	1	1	0	1	32	368000h to 36FFFFh
SA110	1	1	0	1	1	1	0	32	370000h to 377FFFh
SA111	1	1	0	1	1	1	1	32	378000h to 37FFFFh
SA112	1	1	1	0	0	0	0	32	380000h to 387FFFh
SA113	1	1	1	0	0	0	1	32	388000h to 38FFFFh
SA114	1	1	1	0	0	1	0	32	390000h to 397FFFh
SA115	1	1	1	0	0	1	1	32	398000h to 39FFFFh
SA116	1	1	1	0	1	0	0	32	3A0000h to 3A7FFFh
SA117	1	1	1	0	1	0	1	32	3A8000h to 3AFFFFh
SA118	1	1	1	0	1	1	0	32	3B0000h to 3B7FFFh
SA119	1	1	1	0	1	1	1	32	3B8000h to 3BFFFFh
SA120	1	1	1	1	0	0	0	32	3C0000h to 3C7FFFh
SA121	1	1	1	1	0	0	1	32	3C8000h to 3CFFFFh
SA122	1	1	1	1	0	1	0	32	3D0000h to 3D7FFFh
SA123	1	1	1	1	0	1	1	32	3D8000h to 3DFFFFh
SA124	1	1	1	1	1	0	0	32	3E0000h to 3E7FFFh
SA125	1	1	1	1	1	0	1	32	3E8000h to 3EFFFFh
SA126	1	1	1	1	1	1	0	32	3F0000h to 3F7FFFh
SA127	1	1	1	1	1	1	1	32	3F8000h to 3FFFFFh

Sector Group Address Table

Sector Group Address	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	Sector Group Size (Kwords)	Sectors
SGA0	0	0	0	0	0	128	SA0 to SA3
SGA1	0	0	0	0	1	128	SA4 to SA7
SGA2	0	0	0	1	0	128	SA8 to SA11
SGA3	0	0	0	1	1	128	SA12 to SA15
SGA4	0	0	1	0	0	128	SA16 to SA19
SGA5	0	0	1	0	1	128	SA20 to SA23
SGA6	0	0	1	1	0	128	SA24 to SA27
SGA7	0	0	1	1	1	128	SA28 to SA31
SGA8	0	1	0	0	0	128	SA32 to SA35
SGA9	0	1	0	0	1	128	SA36 to SA39
SGA10	0	1	0	1	0	128	SA40 to SA43
SGA11	0	1	0	1	1	128	SA44 to SA47
SGA12	0	1	1	0	0	128	SA48 to SA51
SGA13	0	1	1	0	1	128	SA52 to SA55
SGA14	0	1	1	1	0	128	SA56 to SA59
SGA15	0	1	1	1	1	128	SA60 to SA63
SGA16	1	0	0	0	0	128	SA64 to SA67
SGA17	1	0	0	0	1	128	SA68 to SA71
SGA18	1	0	0	1	0	128	SA72 to SA75
SGA19	1	0	0	1	1	128	SA76 to SA79
SGA20	1	0	1	0	0	128	SA80 to SA83
SGA21	1	0	1	0	1	128	SA84 to SA87
SGA22	1	0	1	1	0	128	SA88 to SA91
SGA23	1	0	1	1	1	128	SA92 to SA95
SGA24	1	1	0	0	0	128	SA96 to SA99
SGA25	1	1	0	0	1	128	SA100 to SA103
SGA26	1	1	0	1	0	128	SA104 to SA107
SGA27	1	1	0	1	1	128	SA108 to SA111
SGA28	1	1	1	0	0	128	SA112 to SA115
SGA29	1	1	1	0	1	128	SA116 to SA119
SGA30	1	1	1	1	0	128	SA120 to SA123
SGA31	1	1	1	1	1	128	SA124 to SA127

Common Flash Memory Interface Code Table

A_6 to A_0	DQ_{15} to DQ_0	Description
10h 11h 12h	0051h 0052h 0059h	Query-unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set 02h : AMD/FJ standard
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = not applicable)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table
1Bh	0027h	V_{CC} Min (write/erase) DQ_7 to DQ_4: 1V/bit, DQ_3 to DQ_0: 100 mV/bit
1Ch	0036h	V_{CC} Max (write/erase) DQ_7 to DQ_4: 1V/bit, DQ_3 to DQ_0: 100 mV/bit
1Dh	0000h	V_{PP} Min voltage (00h = no V_{pp} pin)
1Eh	0000h	V_{PP} Max voltage (00h =no V_{pp} pin)
1Fh	0007h	Typical timeout per single write 2^N µs
20h	0007h	Typical timeout for Min size buffer write 2^N µs
21h	000Ah	Typical timeout per individual sector erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms
23h	0001h	Max timeout for write 2^N times typical
24h	0005h	Max timeout for buffer write 2^N times typical
25h	0004h	Max timeout per individual sector erase 2^N times typical
26h	0000h	Max timeout for full chip erase 2^N times typical
27h	0017h	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description 01h : × 16
2Ah 2Bh	0005h 0000h	Max number of byte in multi-byte write = 2^N
2Ch	0001h	Number of Erase Block Regions within device (02h = Boot)
2Dh 2Eh 2Fh 30h	007Fh 0000h 0000h 0001h	Erase Block Region 1 Information bit 15 to bit 0 : y = number of sectors bit 31 to bit 16 : z = size (z × 256 Byte)
31h 32h 33h 34h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information bit 15 to bit 0 : y = number of sectors bit 31 to bit 16 : z = size (z × 256 Byte)

(Continued)

(Continued)

A_6 to A_0	DQ_{15} to DQ_0	Description
35h 36h 37h 38h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information bit 15 to bit 0 : y = number of sectors bit 31 to bit 16 : z = size (z × 256 Byte)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information bit 15 to bit 0 : y = number of sectors bit 31 to bit 16 : z = size (z × 256 Byte)
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0033h	Minor version number, ASCII
45h	0008h	Address Sensitive Unlock 08h : Supported 09h : Not Supported
46h	0002h	Erase Suspend (02h = To Read & Write)
47h	0004h	Sector Group Protection 00h : Not Supported X : Number of sectors in per group
48h	0001h	Sector Temporary Unprotection 00h : Not Supported 01h : Supported
49h	0004h	Sector Group Protection Algorithm
4Ah	0000h	Dual Operation (00h = Not Supported)
4Bh	0000h	Burst Mode Type (00h = Not Supported)
4Ch	0001h	Page Mode Type (01h = 4-Word Page Supported)
4Dh	00B5h	V_{ACC} (Acceleration) Supply Minimum 00h = Not Supported DQ_7 to DQ_4: 1V/bit, DQ_3 to DQ_0: 100mV/bit
4Eh	00C5h	V_{ACC} (Acceleration) Supply Maximum 00h = Not Supported DQ_7 to DQ_4: 1V/bit, DQ_3 to DQ_0: 100mV/bit
4Fh	0004h	Write Protect 04h = Uniform Sectors Bottom Write Protect
50h	01h	Program Suspend 00h = Not Supported 01h = Supported

■ FUNCTIONAL DESCRIPTION

Standby Mode

There are two ways to implement the standby mode on the device, one using both the $\overline{CE}$ and $\overline{RESET}$ pins, and the other via the $\overline{RESET}$ pin only.

When using both pins, CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ input held at $V_{CC} \pm 0.3$ V. Under this condition the current consumed is less than 5 μA Max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even when $\overline{CE}$ = "H". The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, CMOS standby mode is achieved with $\overline{RESET}$ input held at $V_{SS} \pm 0.3$ V ($\overline{CE}$ = "H" or "L") .
Under this condition the current consumed is less than 5 μA Max. Once the $\overline{RESET}$ pin is set high, the device requires t_{RH} as a wake-up time for output to be valid for read access.

During standby mode, the output is in the high impedance state regardless of $\overline{OE}$ input.

Automatic Sleep Mode

Automatic sleep mode works to resin power consumption during read-out of the device data. This is useful in the application such as a handy terminal which requires low power consumption.

To activate this mode, the device automatically switches itself to low power mode when address remain stable during
access time of t_{ACC} + 30 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ on this mode. The current consumed is typically 1 μA (CMOS Level) .

During simultaneous operation, V_{CC} active current (I_{CC2}) is required.

Since, the data are latched during this mode, the data are continuously read out. When the addresses are changed, the mode is automatically canceled and the device reads the data for changed address.

Autoselect

Autoselect mode allows reading out of a binary code and identifies its manufacturer and type. It is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9. Three identifier bytes may then be sequenced from the device outputs by toggling addresses. All addresses are DON'T CARES except A_6 to A_0.

The manufacturer and device codes may also be read via the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in "Common Definitions Table" of "■ DEVICE BUS OPERATIONS".

A read cycle from address 00h returns the manufacturer's code (Fujitsu = 04h) . A read cycle from address 01h outputs device code. At word mode, 227Eh is output, it indicates that two additional codes, called Extended Device Codes is required. Therefore the system may continue reading out these Extended Device Codes at addresses of 0Eh and 0Fh. Refer to "Autoselect Codes Table" in "■ DEVICE BUS OPERATIONS".

Read Mode

The device has two control functions required to obtain data at the outputs. $\overline{CE}$ is the power control and used for a device selection. $\overline{OE}$ is the output control and used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. Assuming the addresses have been stable for at least t_{ACC} - t_{OE} time. When reading out a data without changing addresses after power-up, input hardware reset or to change $\overline{CE}$ pin from "H" or "L".

Page Mode Read

The device is capable of fast Page mode read and are compatible with Page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Page size is 4 words, within the appropriate Page being selected by the higher address bits A_{21} to A_2 and the address bits A_1 to A_0 in Word mode (A_1 to A_{-1} in Byte mode). The initial page access is equal to the random access (t_{ACC}) and subsequent Page read access (as long as the locations specified by the microprocessor fall within that Page) is equivalent to the page access time (t_{PACC}).

Output Disable

With the $\overline{OE}$ input is at logic high level (V_{IH}), output from the device is disabled. This causes the output pins to be in a high impedance state.

Write

Device erase and programming are accomplished via the command register. The contents of the register serve as input to the internal state machine. The state machine output dictates the device function.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever starts later, while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever starts first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Group Protection

The device features hardware sector group protection. This feature will disable both program and erase operations in any combination of 32 sector groups of memory. See “Sector Group Address Table (MBM29PL65LM)” in “■ DEVICE BUS OPERATION”. The user’s side can use the sector group protection using programming equipment. The device is shipped with all sector groups that are unprotected.

To activate it, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, $\overline{CE}$ = V_{IL} and $A_6 = A_3 = A_2 = A_0 = V_{IL}$, $A_1 = V_{IH}$. The sector group addresses (A_{21}, A_{20}, A_{19}, A_{18}, and A_{17}) should be set to the sector to be protected. “Sector Address Table (MBM29PL65LM)” in “■ DEVICE BUS OPERATION” defines the sector address for each of the seventy-one (71) individual sectors, and “Sector Group Address Table (MBM29PL65LM)” in “■ DEVICE BUS OPERATION” defines the sector group address for each of the twenty-four (24) individual group sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector group addresses must be held constant during the $\overline{WE}$ pulse. See “Sector Group Protection Timing Diagram” in “■ TIMING DIAGRAM” and “Sector Group Protection Algorithm” in “■ FLOW CHART” for sector group protection timing diagram and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector group addresses (A_{21}, A_{20}, A_{19}, A_{18} and A_{17}) while (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) will produce a logical “1” code at device output DQ_0 for a protected sector. Otherwise the device will produce “0” for unprotected sectors. In this mode, the lower order addresses, except for A_0, A_1, A_2, A_3 and A_6 can be either High or Low.

Where the high order addresses (A_{21}, A_{20}, A_{19}, A_{18} and A_{17}) are the desired sector group address will produce a logical “1” at DQ_0 for a protected sector group. See “Sector Group Protection Verify Autoselect Codes” in “■ DEVICE BUS OPERATION” for Autoselect codes.

Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the devices in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (V_{ID}). During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the V_{ID} is taken away from the $\overline{RESET}$ pin, all the previously protected sector groups will be

protected again. Refer to “Temporary Sector Group Unprotection Timing Diagram” in ■ SWITCHING WAVEFORMS and “Temporary Sector Group Unprotection Algorithm” in ■ FLOW CHART.

Hardware Reset

The device may be reset by driving the $\overline{\text{RESET}}$ pin to V_{IL}. The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least “t_{RP}” in order to properly reset the internal state machine. Any operation in the process of being executed is terminated and the internal state machine is reset to the read mode “t_{READY}” after the $\overline{\text{RESET}}$ pin is driven low.

Furthermore once the $\overline{\text{RESET}}$ pin goes high the device requires an additional “t_{RH}” before it allows read access.

When the $\overline{\text{RESET}}$ pin is low, the device is in the standby mode for the duration of the pulse and all the data output pins are tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location are corrupted.

Write Protect ($\overline{\text{WP}}$)

Aside from Sector Group Protection, MBM29PL65LM provides another function that protects the first sector (SA0) during programming and erase. When $\overline{\text{WP}} = V_{IL}$, this first sector (SA0) becomes protected while Sector Group Protection for all the other sectors are temporarily lifted.

Accelerated Program Operation

The device offers accelerated program operation which enables the programming in high speed. If the system asserts V_{ACC} to the $\overline{\text{ACC}}$ pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 85%. This function is primarily intended to allow high speed program, so caution is needed as the sector group becomes temporarily unprotected.

The system uses fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device automatically set to fast mode. Therefore the present sequence is used for programming and detection of completion during acceleration mode.

Removing V_{ACC} from the $\overline{\text{ACC}}$ pin and applying V_{IL} or V_{IH} returns the device to normal operation. Do not remove V_{ACC} from $\overline{\text{ACC}}$ pin while programming. See “Accelerated Program Timing Diagram”.

V_{CCQ}

The output voltage generated on the device is determined based on the V_{CCQ} level. This feature allows the device to operate in mixed-voltage environments, driving and receiving signals to and from other devices on the same bus.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register.

"MBM29PL65LM Command Definitions Table" in ■ DEVICE BUS OPERATION shows the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Also the Program Suspend (B0h) and Program Resume (30h) commands are valid only while the Program operation is in progress. Moreover, Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored.

Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to Reset mode, verify mode of secter protect commands, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device automatically powers-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. Therefore manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a higher voltage. However multiplexing high voltage onto the address lines is not generally desired system design practice.

he device contains Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

This is followed by a third write cycle that contains the address and the Autoselect command. Then the manufacture and device codes can be read from the address, and an actual data of memory cell can be read from the another address.

Following the command write, a read cycle from address 00h returns the manufacturer's code (Fujitsu=04h). And, at double word mode, a read cycle at address 01h outputs device code. At word mode, 227Eh is output, this indicates that two additional codes, called Extended Device Codes will be required. Therefore the system may continue reading out these Extended Device Codes at the address of 0Eh, as well as at (BA) 0Fh (at word mode, 1Eh). Refer to "MBM29PL65LX Autoselect Codes Table" in ■ DEVICE BUS OPERATION.

To terminate the operation, it is necessary to write the Reset command sequence into the register. To execute the Autoselect command during the operation, Reset command sequence must be written before the Autoselect command.

Program Command

The device is programmed on word-by-word basis (or double word-by-double word). Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later, and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) starts programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device automatically provides adequate internally generated program pulses and verify programmed cell margin.

The system can determine the status of the program operation by using DQ_7 ($\overline{Data}$ Polling), DQ_6 (Toggle Bit) or RY/$\overline{BY}$. The $\overline{Data}$ Polling and Toggle Bit are automatically performed at the memory location being programmed.

The programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which the devices return to the read mode and plogram addresses are no longer latched. Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance. Hence $\overline{\text{Data}}$ Polling requires the same address which is being programmed.

If hardware reset occurs during the programming operation, the data being written is not guaranteed.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Reset mode will show that the data is still “0”. Only erase operations can convert from “0”s to “1”s.Refer to "Embedded Program™ Algorithm" using typical command strings and bus operations.

Program Suspend/Resume Command

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any address. Writing the Program Suspend command (B0h) during the Embedded Program operation immediately suspends the programming. The bank addresses of sector being programmed should be set when writing the Program Suspend command.

When the Program Suspend command is written during a programming process, the device halts the program operation within 1 μs and updates the status bits.

After the program operation has been suspended, the system can read data from any address. The data at program-suspended address is not valid. Normal read timing and command definitions apply.

After the Program Resume command (30h) is written, the device reverts to programming. The bank addresses of sectors being suspended should be set when writing the Program Resume command. The system can determine the program operation status using the DQ_7 or DQ_6 status bits, just as in the standard program operation. See “Write Operation Status” for more information. When issuing program suspend command in 4 μs after issuing program command, determine the status of program operation by reading status bit at more 4 μs after issuing program resume command.

The system may also write the Autoselect command sequence in the Program Suspend mode.

The device allows reading Autoselect codes at the addresses within programming sectors, since the codes are not stored in the memory. When the device exits from the Autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See “Autoselect Command Sequence” for more information.

The system must write the Program Resume command to exit from the Program Suspend mode and continue programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming.

Do not read CFI code after HiddenROM Entry and Exit in program suspend mode.

Write Buffer Programming Operations

Write Buffer Programming allows the system write to series of 16 words in one programming operation. This results in faster effective word programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle selecting the Sector Address in which programming will occur. In forth cycle contains both Sector Address and unique code for data bus width will be loaded into the page buffer at the Sector Address in which programming will occur.

The system then writes the starting address/data combination. This “starting address” must be the same Sector Address used in third and fourth cycles and its lower addresses of A_3 to A_0 should be 0h. All subsequent address must be incremented by 1. Addresses are latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens later and the data is latched on the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever happens first. The rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ (whichever happens first) starts programming. Upon executing the Write Buffer Programming Operations com-

mand sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

DQ_7($\overline{Data}$ Polling), DQ_6(Toggle Bit), DQ_5(Exceeded Timing Limits), DQ_1(Write-to-Buffer Abort) should be monitored to determine the device status during Write Buffer Programming. In addition to these functions, it is also possible to indicate to the host system that Write Buffer Programming Operations are either in progress or have been completed by RY/$\overline{BY}$. See “Hardware Sequence Flags”.The $\overline{Data}$ polling techniques described in “$\overline{Data}$ Polling Algorithm” in ■ FLOW CHART should be used while monitoring the last address location loaded into the write buffer. In addition, it is not neccessary to specify an address in Toggle Bit techniques described in “Toggle Bit Algorithm” in ■ FLOW CHART. The automatic programing operation is completed when the data on DQ7 is equivalent to the data written to this bit at which time the device returns to the read mode and addresses are no longer latched (See "Hardware Sequence Flags").

The write-buffer programming operation can be suspended using the standard program suspend/resume commands.

Once the write buffer programming is set, the system must then write the “Program Buffer to Flash” command at the Sector Address. Any other address/data combination will abort the Write Buffer Programming operation and the device will continue busy state.

The Write Buffer Programming Sequence can be ABORTED by doing the following :

- Different Sector Address is asserted.
- Write data other than the “Program Buffer to Flash" command after the specified number of “data load” cycles.

A “Write-to-Buffer-Abort Reset” command sequence must be written to the device to return to read mode. (See “MBM29PL65LM Standard Command Definitions” in ■ DEVICE BUS OPERATION for details on this command sequence.)

Chip Erase Command

Chip erase is a six-bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. (Preprogram Function) The system is not required to provide any controls or timings during these operations.

The system can determine the erase operation status by using DQ_7 ($\overline{Data}$ Polling), or DQ_6 (Toggle Bit). The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on DQ_7 is “1” at which the device returns to read the mode.

Chip Erase Time: Sector Erase Time × All sectors + Chip Program Time (Preprogramming)

Refer to "Embedded Erase™ Algorithm" for typical command strings and bus operations.

Sector Erase Command

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever starts later, while the command (Data = 30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever states first. After time-out of “t_{TOW}” from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors are erased concurrently by writing the six bus cycle operations on "MBM29XL12DF Command Definitions Table" in ■ DEVICE BUS OPERATION. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “t_{TOW}” otherwise that command is not accepted and erasure does not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of “t_{TOW}” from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever starts first initiates the execution of the Sector Erase command(s). If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever

starts first occurs within the "t_{TOW}" time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, "Sector Erase Timer".) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun may corrupt the data in the sector. In that case restart the erase on those sectors and allow them to complete. Refer to "Write Operation Status" section for Sector Erase Timer operation. Loading the sector erase buffer may be done in any sequence and with any number of sectors.

Sector erase does not require the user to program prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data}}$ Polling), or DQ_6 (Toggle Bit).

The sector erase begins after the "t_{TOW}" time out from the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever starts first for the last sector erase command pulse and terminates when the data on DQ_7 is "1" at which time the device returns to the read mode. See "Write Operation Status" section. $\overline{\text{Data}}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] $\times$ Number of Sector Erase.

Erase Suspend/Resume Command

The Erase Suspend command allows the user to interrupt Sector Erase operation and then perform read to a sector not being erased. This command is applicable ONLY during the Sector Erase operation within the time-out period for Sectore erase.

Writting the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation.

When the "Erase Suspend" command is written during the Sector Erase operation, the device takes a maximum of "t_{SPD}" to suspend the erase operation. When the devices have entered the erase-suspended mode, the RY/BY output pin will be at High-Z and the DQ_7 bit will be at logic "1" and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation is suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode causes DQ_2 to toggle. See the section on DQ_2.

To resume the operation of Sector Erase, the Resume command (30h) should be written. Any further writes of the Resume command at this point is ignored. Another Erase Suspend command is written after the chip resumes erasing.

Do not issuing program command after entering erase-suspend-read mode.

Fast Mode Set/Reset Command

Fast Mode function dispenses with the initial two unlock cycles required in the standard program command sequence writing Fast Mode command into the command register. In this mode the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. The read operation is also executed after exiting this mode. During the Fast mode, do not write any commands other than the Fast program/Fast mode reset command. To exit this mode, write Fast Mode Reset command into the command register. Refer to "Embedded Program Algorithm for Fast Mode". The V_{CC} active current is required even $\overline{CE} = V_{IH}$ during Fast Mode.

Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). Refer to "Embedded Program Algorithm for Fast Mode".

Extended Sector Group Protection

In addition to normal sector group protection, the device has Extended Sector Group Protection as extended function. This function enables protection of the sector group by forcing V_{ID} on $\overline{RESET}$ pin and writes a command sequence. Unlike conventional procedures, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector group protection in this mode. The extended sector group protection requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then the sector group addresses pins (A_{21}, A_{20}, A_{19}, A_{18}, and A_{17}) and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) should be set to the sector group to be protected (set V_{IL} for the other addresses pins is recommended), and write extended sector group protection command (60h). A sector group is typically protected in 250 µs.

To verify programming of the protection circuitry, the sector group addresses pins (A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) should be set and write a command (40h). Following the command write, a logical “1” at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical “0”, write the extended sector group protection command (60h) again. To terminate the operation, set $\overline{RESET}$ pin to V_{IH}. (Refer to the “Extended Sector Group Protection Timing Diagram” in ■ SWITCHING WAVEFORMS and “Extended Sector Group Protection Algorithm” in ■ FLOW CHART.)

Query Command (CFI : Common Flash Memory Interface)

To verify programming of the protection circuitry, the sector group addresses pins (A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0) should be set and write a command (40h). Following the command write, a logical “1” at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical “0”, write the extended sector group protection command (60h) again. To terminate the operation, set $\overline{RESET}$ pin to V_{IH}. (Refer to the “Extended Sector Group Protection Timing Diagram” in ■ SWITCHING WAVEFORMS and “Extended Sector Group Protection Algorithm” in ■ FLOW CHART.)

The operation is initiated by writing the query command (98h) into the command register. Following the command write, a read cycle from specific address retrives device information. Refer to "Common Flash Memory Interface Code" in ■ DEVICE BUS OPERATION in detail. Please note that output data of upper byte (DQ_{15} to DQ_8) is “0” in word mode (16 bit) read. To terminate operation, write the Read/Reset command sequence into the register.

HiddenROM Mode
HiddenROM Region

The HiddenROM (HiddenROM) feature provides a Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the HiddenROM region is protected, any further modification of that region is impossible. This ensures the security of the ESN once the product is shipped to the field. This device occupies the address of the 000000h to 00007Fh.

After the system writes the HiddenROM Entry command sequence, it may read the HiddenROM region by using device addresses A_6 to A_0 (A_{20} to A_7 are all “0”). That is, the device sends only program command that would normally be sent to the address to the HiddenROM region. This mode of operation continues until the system issues the Exit HiddenROM command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the address.

If you request Fujitsu to program the ESN in the device, please contact a Fujitsu representative for more information.

HiddenROM Entry Command

The device has a HiddenROM area with One Time Protect function. This area is to enter the security code and to unable the change of the code once set. Program/erase is possible in this area until it is protected. However once it is protected, it is impossible to unprotect. Therefore extreme caution is required.

HiddenROM area is 128 words. This area is normally the “outermost” 8K words boot block area. Therefore, write the HiddenROM entry command sequence to enter the HiddenROM area. It is called HiddenROM mode when the HiddenROM area appears.

Sectors other than the block area SA0 can be read during HiddenROM mode. Read/program of the HiddenROM area is possible during HiddenROM mode. Write the HiddenROM reset command sequence to exit the HiddenROM mode. Note that any other commands should not be issued than the HiddenROM program/protection/reset commands during the HiddenROM mode. When you issue the other commands including the suspend resume capability, send the HiddenROM reset command first to exit the HiddenROM mode and then issue each command.

HiddenROM Program Command

To program the data to the HiddenROM area, write the HiddenROM program command sequence during HiddenROM mode. This command is the same as the program command in usual except to write the command during HiddenROM mode. Therefore the detection of completion method is the same as using the DQ_7 data polling, and DQ_6 toggle bit. Need to pay attention to the address to be programmed. If the address other than the HiddenROM area is selected to program, data of the address are changed.During the write into the HiddenROM region, the program suspend command issuance is prohibited.

HiddenROM Protect Command

The method to protect the HiddenROM is to apply high voltage (V_{ID}) to A_9 and $\overline{OE}$, set the sector address in the HiddenROM area and $(A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0)$, and apply the write pulse during the HiddenROM mode. The same command sequence may be used because it is the same as the extension sector group protect in the past, except that it is in the HiddenROM mode and does not apply high voltage to the $\overline{RESET}$ pin. Please refer to above mentioned “Extended Sector Group Protection” for details of sector group protect setting.

The same command sequence may be used because it is the same as the extension sector group protect in the past, except that it is in the HiddenROM mode and does not apply high voltage to the $\overline{RESET}$ pin. Please refer to above mentioned “Extended Sector Group Protection” for details of sector group protect setting.

Other sector will be effected if the address other than those for HiddenROM area is selected for the sector address, so please be carefull. Once it is protected, protection can not be cancelled, so please pay the closest attention.

Write Operation Status

Hardware Sequence Flags

Detailed in “Hardware Sequence Flags” are all the status flags which can determine the status of the bank for the current mode operation. During sector erase, the part provides the status flags automatically to the I/O ports.

The information on DQ_2 is address-sensitive. This means that if an address from an erasing sector is consecutively read, the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consecutively read. This allows users to determine which sectors are in erase and which are not.

Hardware Sequence Flags Table

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2	DQ_1 *3
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle *1	N/A
	Program Suspend Mode	Program-Suspend-Read (Program Suspend Sector)	Data	Data	Data	Data	Data	Data
		Program-Supend -Read (Non-Program Suspended Sector)	Data	Data	Data	Data	Data	Data
	Erase Suspend Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle *1	N/A
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1 *2	N/A
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1	N/A
	Embedded Erase Algorithm		0	Toggle	1	1	N/A	N/A
	Erase Suspend Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A	N/A
Write to Buffer *4	BUSY State		$\overline{DQ_7}$	Toggle	0	N/A	N/A	0
	Exceeded Timing Limits		$\overline{DQ_7}$	Toggle	1	N/A	N/A	0
	ABORT State		N/A	Toggle	0	N/A	N/A	1

*1 : Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle.

*2 : Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

*3 : DQ_1 indicates the Write-to-Buffer ABORT status during Write-Buffer-Programming operations.

*4 : The $\overline{Data}$ Polling algorithm detailed in “$\overline{Data}$ Polling Algorithm” in “ ■ FLOW CHART” should be used for Write-Buffer-Programming operations. Note that $\overline{DQ_7}$ during Write-Buffer-Programming indicates the data-bar for DQ_7 data for the LAST LOADED WRITE-BUFFER ADDRESS location.

DQ_7

$\overline{Data}$ Polling

The device features $\overline{Data}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, an attempt to read the device will produce a complement of data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a “0” at the DQ_7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read device will produce a “1” on DQ_7. The flowchart for $\overline{Data}$ Polling (DQ_7) is shown in “Data Polling Algorithm”. For programming, the $\overline{Data}$ Polling is valid after the rising edge of the fourth write pulse in the four write pulse sequences.

For programming, the $\overline{Data}$ Polling is valid after the rising edge of the fourth write pulse in the four write pulse sequences.

For chip erase and sector erase, the $\overline{Data}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequences. $\overline{Data}$ Polling must be performed at sector addresses of sectors being erased, not protected sectors. Otherwise the status may become invalid.

If a program address falls within a protected sector, $\overline{Data}$ Polling on DQ_7 is active for approximately 1 μs, then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{Data}$ Polling on DQ_7 is active for approximately 400 μs, then the bank returns to read mode.

Once the Embedded Algorithm operation is close to being completed, the device data pins (DQ_7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that device is driving status information on DQ_7 at one instant, and then that byte's valid data at the next instant. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if device has completed the Embedded Algorithm operation and DQ_7 has a valid data, data outputs on DQ_0 to DQ_6 may still be invalid. The valid data on DQ_0 to DQ_7 will be read on successive read attempts.

The $\overline{Data}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. See "Toggle Bit Status" and "$\overline{Data}$ Polling during Embedded Algorithm Operation Timing Diagram".

DQ_6
Toggle Bit I

The device also features the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the busy bank will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequences. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequences. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written is protected, the toggle bit will toggle for about 1 µs and then stop toggling with data unchanged. In erase, the device will erase all selected sectors except for protected ones. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 µs and then drop back into read mode, having data kept remained.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ_6 to toggle.

The system can use DQ_6 to determine whether a sector is actively erased or is erase-suspended. When a bank is actively erased (that is, the Embedded Erase Algorithm is in progress) , DQ_6 toggles. When a bank enters the Erase Suspend mode, DQ_6 stops toggling. Successive read cycles during erase-suspend-program cause DQ_6 to toggle. See "AC Wavefrom for Toggle Bit I during Embedded Algorithm Operations".

DQ_5
Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count) . Under these conditions DQ_5 will produce "1". This is a failure condition indicating that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling is only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down device under these conditions (to approximately 2 mA) . The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in "MBM29PL65LM User Bus Operations Table (DW/$\overline{W}$ = V_{IL})" and "MBM29XL12DF User Bus Operations Table (DW/$\overline{W}$ = V_{IH})" in ■ DEVICE BUS OPERATION.

The DQ_5 failure condition may also appear if a user tries to program a non-blank location without pre-erase. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads valid data on DQ_7 bit and DQ_6 never stop toggling. Once the device has exceeded timing limits, the DQ_5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used. If this occurs, reset device with the command sequence.

DQ_3
Sector Erase Timer

After completion of the initial sector erase command sequence, sector erase time-out begins. DQ_3 will remain low until the time-out is completed. $\overline{Data}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates that a valid erase command has been written, DQ_3 may be used to determine whether the sector erase timer window is still open. If DQ_3 is high (“1”) the internally controlled erase cycle has begun. If DQ_3 is low (“0”) , the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See “Hardware Sequence Flags”.

DQ_2

Toggle Bit II

This toggle bit II, along with DQ_6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the non-erase suspended sector will indicate a logic “1” at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows :

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also “Toggle Bit Status” and "DQ_2 vs DQ_6".

Furthermore DQ_2 can also be used to determine which sector is being erased. At the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

Reading Toggle Bits DQ_6/DQ_2

Whenever the system initially begins reading toggle bit status, it must read DQ_7 to DQ_0 at least twice in a row to determine whether a toggle bit is toggling. Typically a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ_7 to DQ_0 on the following read cycle.

However, if, after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ_5 is high (see the section on DQ_5) . If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ_5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ_5 has not gone high. The system may continue to monitor the toggle bit and DQ_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. Refer to “Toggle Bit Algorithm”.

Toggle Bit Status Table

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle *1
Erase-Suspend-Read (Erase-Suspended Sector)	1	1	Toggle *1
Erase-Suspend-Program	$\overline{DQ_7}$	Toggle	1 *2

*1 : Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle.

*2 : Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

DQ_1

Write-to-Buffer Abort

DQ_1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ_1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See "Write Buffer Programming Operations" section for more details.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up device automatically resets internal state machine to Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequence.

Device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than V_{LKO}. If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition, the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the user’s responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above V_{LKO}.

If Embedded Erase Algorithm is interrupted, the intervened erasing sector(s) is(are) not valid.

Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to read mode on power-up.

Sector Protection

Device user is able to protect each sector group individually to store and protect data. Protection circuit voids both write and erase commands that are addressed to protected sectors. Any commands to write or erase addressed to protected sector are ignored.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–20	+85	°C
Voltage with Respect to Ground All Pins Except A_9, $\overline{OE}$, and $\overline{RESET}$ *1,*2	V_{IN}, V_{OUT}	–0.5	V_{CC} +0.5	V
Power Supply Voltage *1	V_{CC},V_{CCQ}	–0.5	+4.0	V
A_9, $\overline{OE}$, and $\overline{RESET}$ *1,*3	V_{IN}	–0.5	+12.5	V
$\overline{WP}$/ACC *1,*3	V_{ACC}	–0.5	+12.5	V

*1 : Voltage is defined on the basis of VSS = GND = 0 V.

*2 : Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –0.2 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods of up to 20 ns

*3 : Minimum DC input voltage is –0.5V. During voltage transitions, these pins may undershoot V_{SS} to –0.2 V for periods of up to 20 ns.Voltage difference between input and supply voltage (V_{IN}–V_{CC}) dose not exceed to +9.0 V.Maximum DC input voltage is +12.5 V which may overshoot to +14.0 V for periods of up to 20 ns .

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING RANGES*1

Parameter		Symbol	Value		Unit
			Min	Max	
Ambient Temperature	90	T_A	–20	+70	°C
	10		–20	+85	
V_{CC} Supply Voltage *2, *3		V_{CC}	+3.0	+3.6	V
V_{CCQ} Supply Voltage *2, *3		V_{CCQ}	V_{CC}		V

*1 : Operating ranges define those limits between which the functionality of the device is guaranteed.

*2 : Voltage is defined on the basis of V_{SS} = GND = 0 V.

*3 : V_{CC} and V_{CCQ} supply voltage must be on the same level.

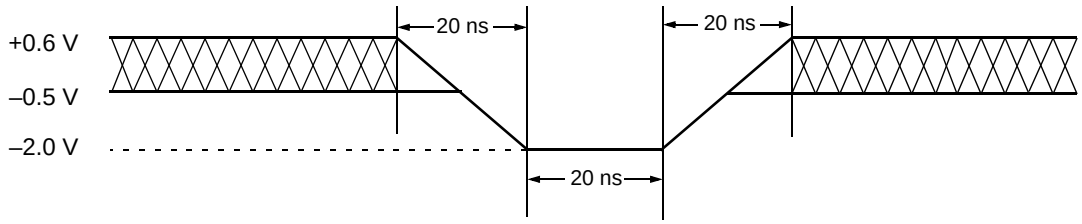
WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

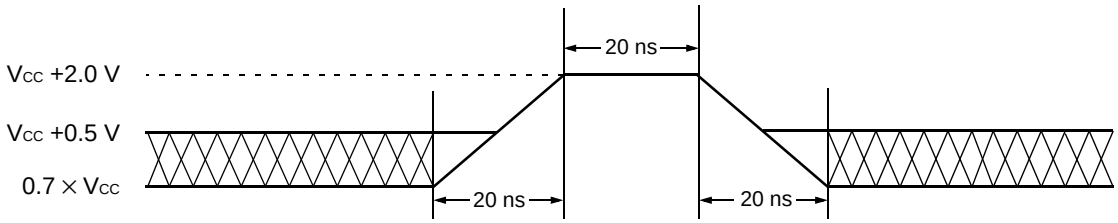
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT

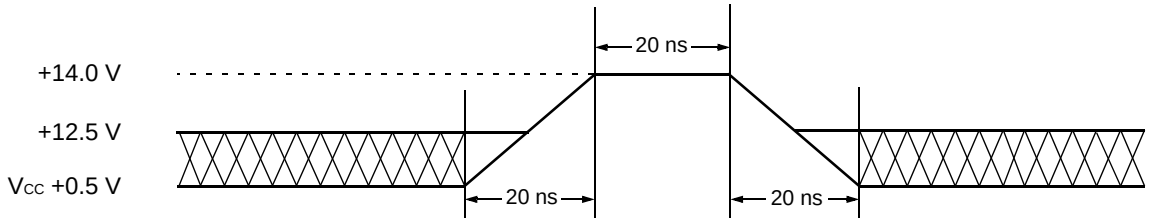
1. Maximum Undershoot Waveform



2. Maximum Overshoot Waveform 1



3. Maximum Overshoot Waveform 2



Note : This waveform is applied for A_9, $\overline{OE}$ and $\overline{RESET}$.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max	$\overline{WP}$ Pin	–2.0	—	+2.0	µA
			Others	–1.0	—	+1.0	
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max		–1.0	—	+1.0	µA
A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	V_{CC} = V_{CC} Max, A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V		—	—	35	µA
V_{CC} Active Current (Read) *1,*2	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5 MHz		—	15	25	mA
		$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 10 MHz		—	35	50	mA
V_{CC} Active Current (Intra-Page Read) *2	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, t_{PRC} = 25 ns, 4-Word		—	10	20	mA
V_{CC} Active Current (Program / Erase) *2,*3	I_{CC3}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	50	60	mA
V_{CC} Standby Current *2	I_{CC4}	$\overline{CE}$ = V_{CC} ± 0.3 V, $\overline{RESET}$ = V_{CC} ± 0.3 V, $\overline{OE}$ = V_{IH}, $\overline{WP}$ = V_{CC} ± 0.3 V		—	1	5	µA
V_{CC} Reset Current *2	I_{CC5}	$\overline{RESET}$ = V_{CC} ± 0.3 V, $\overline{WP}$ = V_{CC} ± 0.3 V		—	1	5	µA
V_{CC} Automatic Sleep Current *4	I_{CC6}	$\overline{CE}$ = V_{SS} ± 0.3 V, $\overline{RESET}$ = V_{CC} ± 0.3 V, V_{IN} = V_{CC} ± 0.3 V or V_{ss} ± 0.3 V, $\overline{WP}$ = V_{CC} ± 0.3 V		—	1	5	µA
V_{CC} Active Current (Erase-Suspend-Program) *2	I_{CC7}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	50	60	mA
ACC Accelerated Program Current	I_{ACC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Vcc = Vcc Max, ACC =V_{ACC} Max	ACC Pin	—	—	45	mA
			Vcc Pin	—	—	60	
Input Low Level	V_{IL}	—		–0.5	—	0.6	V
Input High Level	V_{IH}	—		0.7 × V_{CC}	—	V_{CC} + 0.3	V
Voltage for ACC Sector Protection/Unprotection and Program Acceleration	V_{ACC}	V_{CC} = 3.0 V to 3.6 V		11.5	12.0	12.5	V
Voltage for Autoselect, and Temporary Sector Unprotected	V_{ID}	V_{CC} = 3.0 V to 3.6 V		11.5	12.0	12.5	V
Output Low Voltage Level	V_{OL}	I_{OL} = 4.0 mA, V_{CC} = V_{CC} Min, V_{CCQ} = V_{CCQ} Min		—	—	0.45	V
Output High Voltage Level	V_{OH}	I_{OH} = –2.0 mA, V_{CC} = V_{CC} Min, V_{CCQ} = V_{CCQ} Min		0.85 × V_{CCQ}	—	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—		2.3	—	2.5	V

*1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2 : Maximum I_{CC} values are tested with V_{CC} = V_{CC} Max and V_{CCQ} = V_{CCQ} Max.

*3 : I_{CC} active while Embedded Erase or Embedded Program or Write Buffer Programming is in progress.

*4 : Automatic sleep mode enables the low power mode when address remain stable for t_{ACC} + 30 ns.

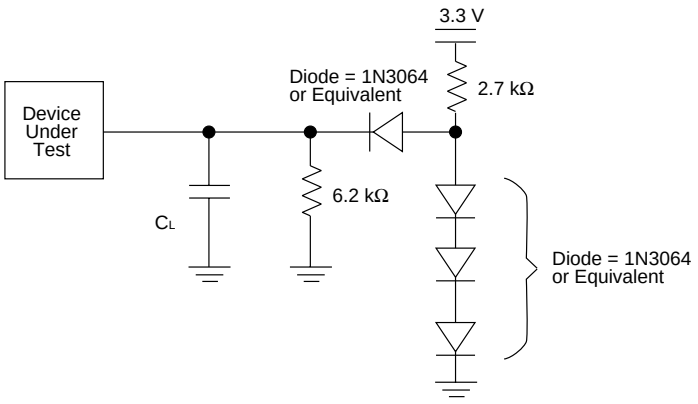
2. AC Characteristics

• Read Only Operations Characteristics

Parameter		Symbol		Condition	MBM29PL65LM-90*			MBM29PL65LM-10*			Unit
		JEDEC	Standard		Min	Typ	Max	Min	Typ	Max	
Read Cycle Time		t_{RC}	t_{RC}	—	90	—	—	100	—	—	ns
Address to Output Delay		t_{ACC}	t_{ACC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}	—	—	90	—	—	100	ns
Chip Enable to Output Delay		t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}	—	—	90	—	—	100	ns
Page Read Cycle Time		t_{PRC}	t_{PRC}	—	25	—	—	30	—	—	ns
Page Address to Output Delay		t_{PACC}	t_{PACC}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}	—	—	25	—	—	30	ns
Output Enable to Output Delay		t_{OE}	t_{OE}	—	—	—	25	—	—	30	ns
Chip Enable to Output High-Z		t_{DF}	t_{DF}	—	—	—	25	—	—	30	ns
Output Enable Hold Time	Read	t_{OEH}	t_{OEH}	—	0	—	—	0	—	—	ns
	Toggle and $\overline{Data}$ Polling			—	10	—	—	10	—	—	ns
Output Enable to Output High-Z		t_{DF}	t_{DF}	—	—	—	25	—	—	30	ns
Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		t_{OH}	t_{OH}	—	0	—	—	0	—	—	ns
$\overline{RESET}$ Pin Low to Read Mode		t_{READY}	t_{READY}	—	—	—	20	—	—	20	µs

* : Test Conditions;
- Input pulse levels : 0.0 V / V_{CC}
- Input rise times : 5 ns
- Input fall times : 5 ns
- Timing measurement reference level
  - Input : 0.5 × V_{CC}
  - Output : 0.5 × V_{CC}
- Output Load : 1 TTL + 30 pF

•Test Conditions



- **Write (Erase/Program) Operations**

Parameter		Symbol		MBM29PL65LM-90			MBM29PL65LM-10			Unit
		JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Write Cycle Time		t_{WC}	t_{WC}	90	—	—	100	—	—	ns
Address Setup Time		t_{AS}	t_{AS}	0	—	—	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling		t_{ASO}	t_{ASO}	15	—	—	15	—	—	ns
Address Hold Time		t_{AH}	t_{AH}	45	—	—	45	—	—	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling		t_{AHT}	t_{AHT}	0	—	—	0	—	—	ns
Data Setup Time		t_{DS}	t_{DS}	35	—	—	35	—	—	ns
Data Hold Time		t_{DH}	t_{DH}	0	—	—	0	—	—	ns
Output Enable Setup Time		t_{OES}	t_{OES}	0	—	—	0	—	—	ns
$\overline{CE}$ High During Toggle Bit Polling		t_{CEPH}	t_{CEPH}	20	—	—	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling		t_{OEPH}	t_{OEPH}	20	—	—	20	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		t_{GHWL}	t_{GHWL}	0	—	—	0	—	—	ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{CE}$ Low)		t_{GHEL}	t_{GHEL}	0	—	—	0	—	—	ns
$\overline{CE}$ Setup Time		t_{CS}	t_{CS}	0	—	—	0	—	—	ns
$\overline{WE}$ Setup Time		t_{WS}	t_{WS}	0	—	—	0	—	—	ns
$\overline{CE}$ Hold Time		t_{CH}	t_{CH}	0	—	—	0	—	—	ns
$\overline{WE}$ Hold Time		t_{WH}	t_{WH}	0	—	—	0	—	—	ns
$\overline{CE}$ Pulse Width		t_{CP}	t_{CP}	35	—	—	35	—	—	ns
Write Pulse Width		t_{WP}	t_{WP}	35	—	—	35	—	—	ns
$\overline{CE}$ Pulse Width High		t_{CPH}	t_{CPH}	25	—	—	25	—	—	ns
Write Pulse Width High		t_{WPH}	t_{WPH}	30	—	—	30	—	—	ns
Effective Page Programming Time (Write Buffer Programming)	Per Word	t_{WHWH1}	t_{WHWH1}	—	23.5	—	—	23.5	—	µs
Programming Time	Word			—	100	—	—	100	—	µs
Sector Erase Operation *1		t_{WHWH2}	t_{WHWH2}	—	1.0	—	—	1.0	—	s
V_{CC} Setup Time		t_{VCS}	t_{VCS}	50	—	—	50	—	—	µs

(Continued)

(Continued)

Parameter	Symbol		MBM29PL65LM-90			MBM29PL65LM-10			Unit
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
Rise Time to V_{ID} *2	t_{VIDR}	t_{VIDR}	500	—	—	500	—	—	ns
Rise Time to V_{ACC} *3	t_{VACCR}	t_{VACCR}	500	—	—	500	—	—	ns
Voltage Transition Time *2	t_{VLHT}	t_{VLHT}	4	—	—	4	—	—	µs
Write Pulse Width *2	t_{WPP}	t_{WPP}	100	—	—	100	—	—	µs
$\overline{OE}$ Setup Time to $\overline{WE}$ Active *2	t_{OESP}	t_{OESP}	4	—	—	4	—	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$ Active *2	t_{CSP}	t_{CSP}	4	—	—	4	—	—	µs
$\overline{RESET}$ Pulse Width	t_{RP}	t_{RP}	500	—	—	500	—	—	ns
$\overline{RESET}$ High Time Before Read	t_{RH}	t_{RH}	100	—	—	100	—	—	ns
Delay Time from Embedded Output Enable	t_{EOE}	t_{EOE}	—	—	90	—	—	100	ns
Erase Time-out Time	t_{TOW}	t_{TOW}	50	—	—	50	—	—	µs
Erase Suspend Transition Time	t_{SPD}	t_{SPD}	—	—	20	—	—	20	µs

*1 : This does not include the preprogramming time.

*2 : This timing is for Sector Group Protection operation.

*3 : This timing is for Accelerated Program operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Remarks
	Min	Typ	Max		
Sector Erase Time	—	1	15	s	Excludes programming time prior to erasure
Programming Time	—	100	3000	µs	Excludes system-level overhead
Effective Page Programming Time (Write Buffer Programming)	—	23.5	—	µs	
Chip Programming Time	—	—	600	s	
Absolute Maximum Programming Time (16 words)	—	—	6	ms	Non programming within the same page
Erase/Program Cycle	100,000	—	—	cycle	—

■ TSOP (1) PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = 0	—	8	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	—	8.5	12	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	—	8	10	pF
$\overline{RESET}$ pin and ACC Pin Capacitance	C_{IN3}	V_{IN} = 0	—	20	25	pF

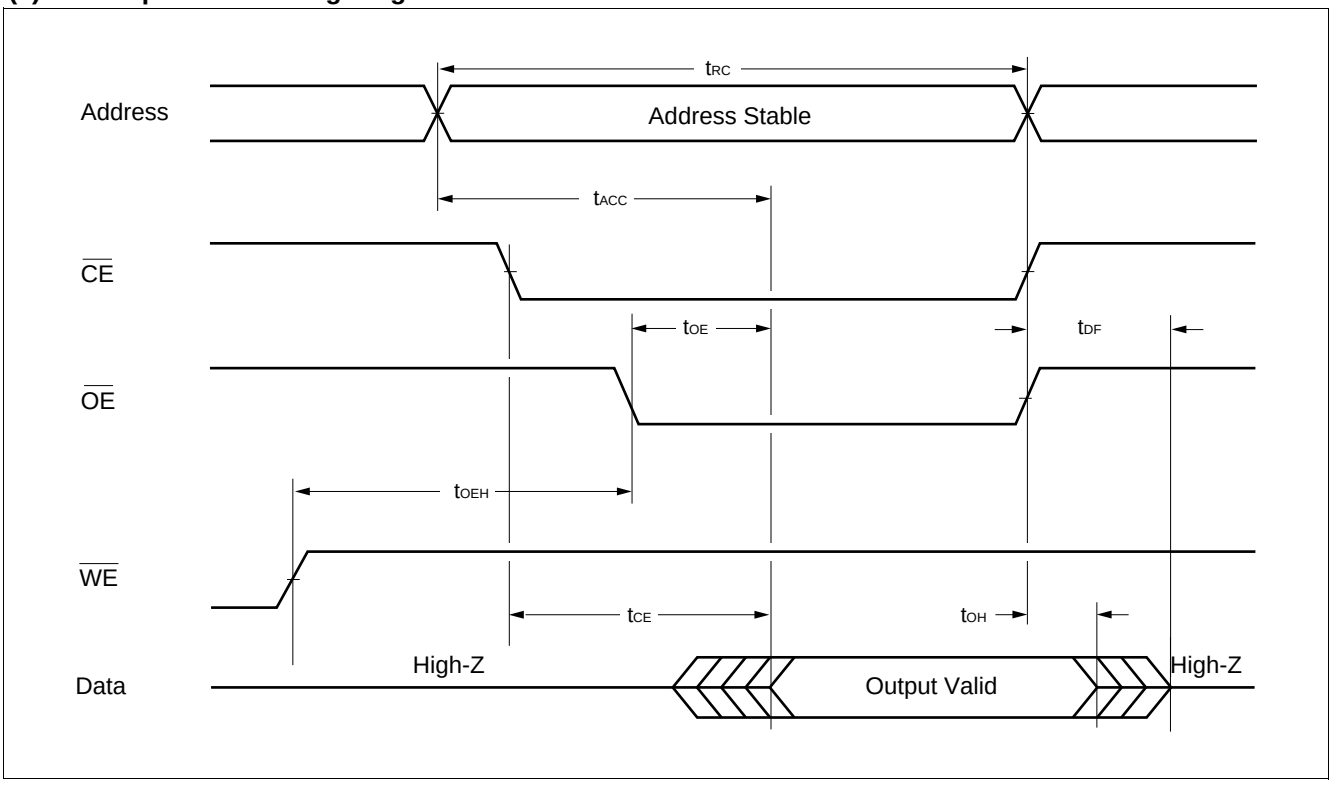
Note : Test conditions T_A = +25°C, f = 1.0 MHz
DQ_{15} pin capacitance is stipulated by output capacitance.

■ TIMING DIAGRAM

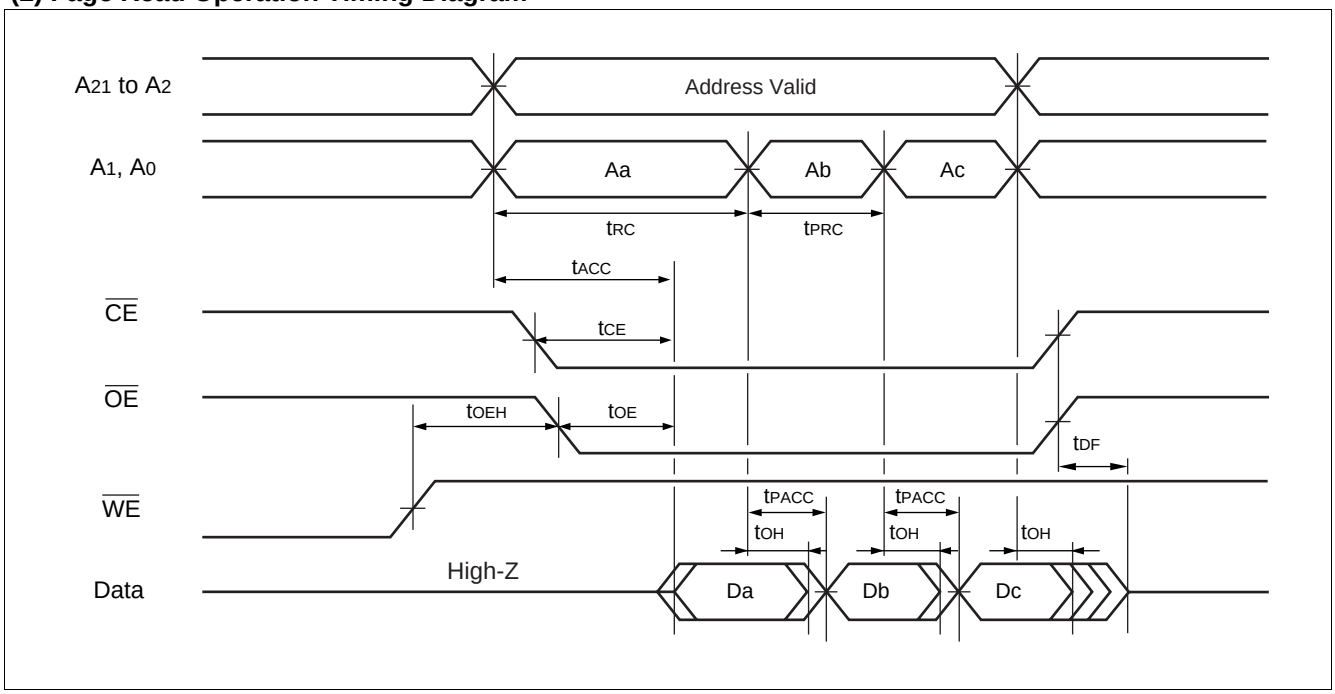
- Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	"H" or "L" Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

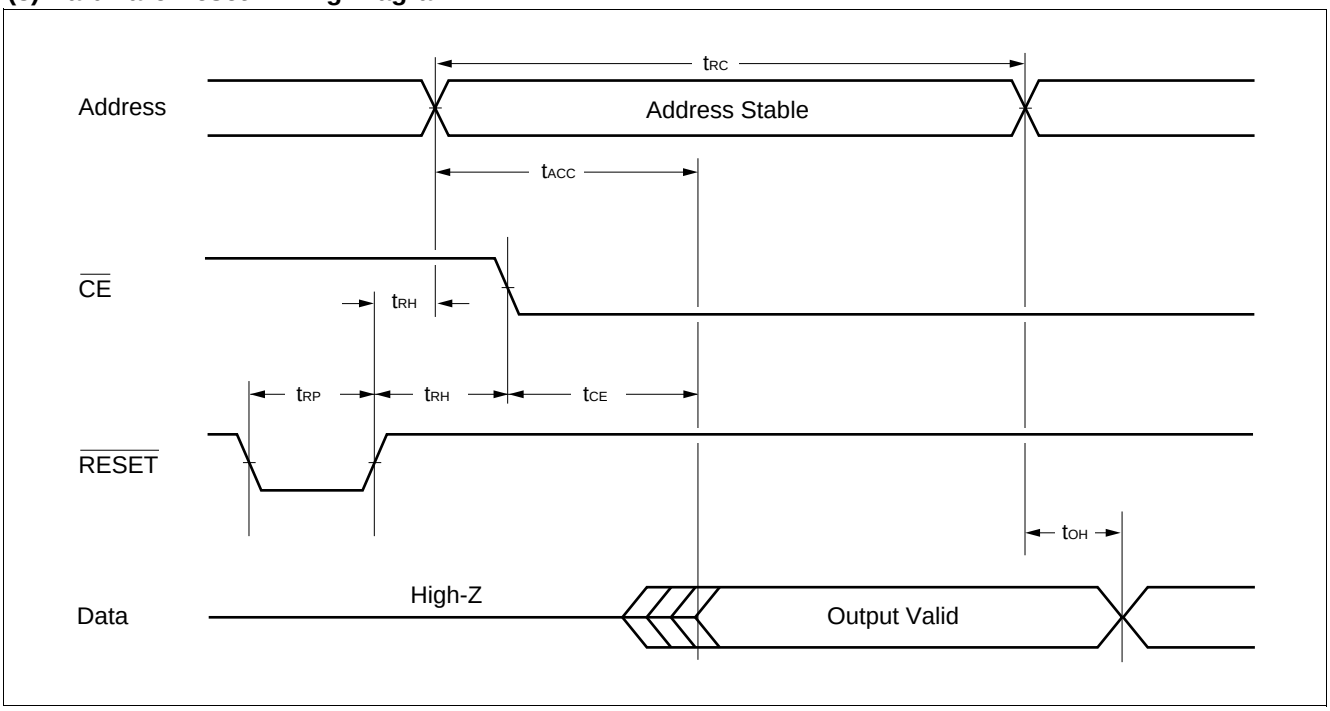
(1) Read Operation Timing Diagram



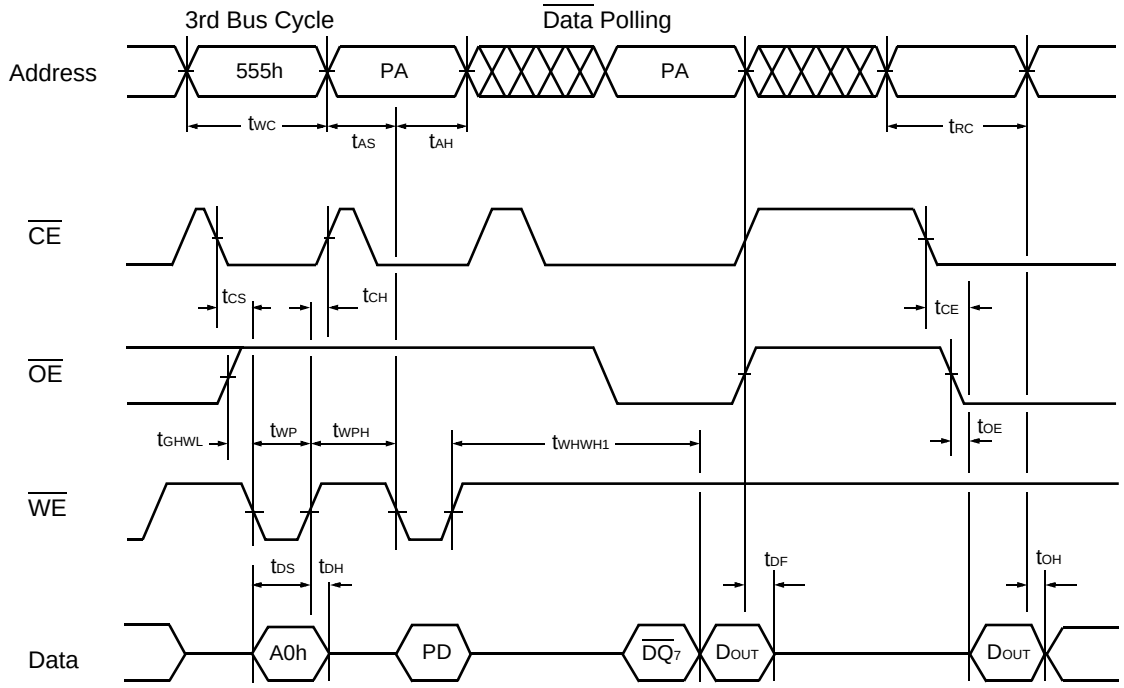
(2) Page Read Operation Timing Diagram



(3) Hardware Reset Timing Diagram



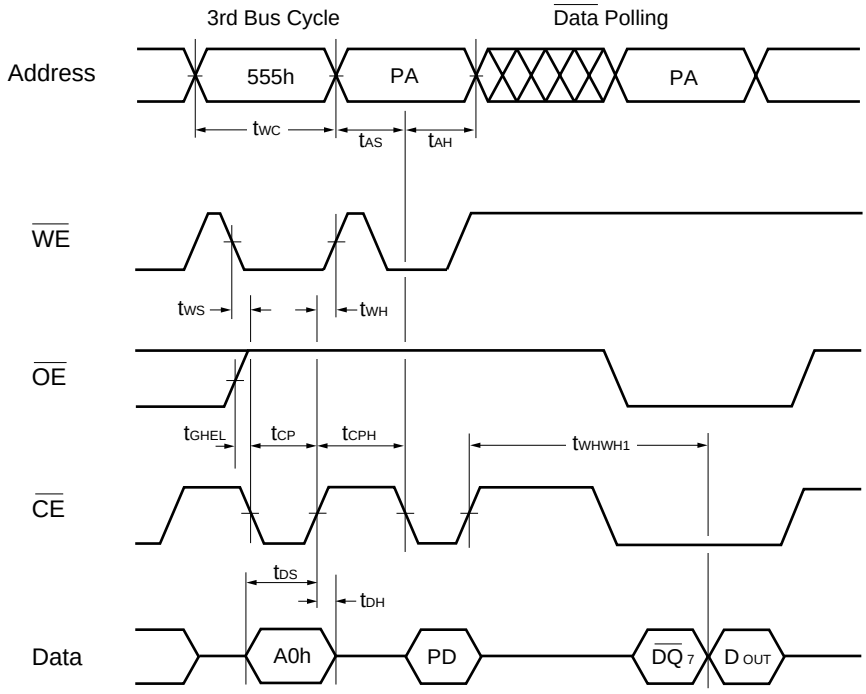
(4) Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram



PA : Address of the memory location to be programmed.
PD : Data to be programmed at word address.
$\overline{DQ_7}$: The output of the complement of the data written to the device.
D_{OUT} : The output of the data written to the device

Note : Figure indicates the last two bus cycles out of four bus cycle sequence.

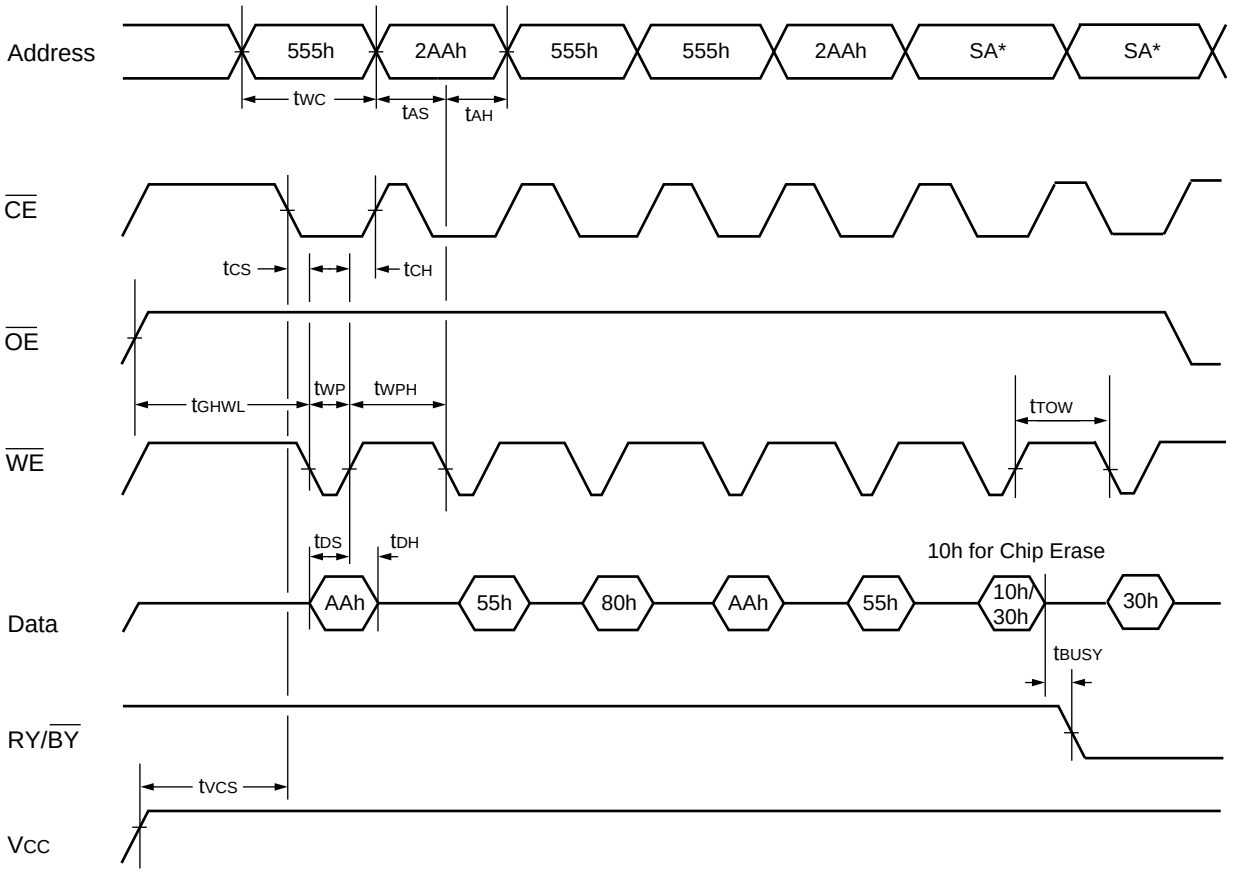
(5) Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram



PA : Address of the memory location to be programmed.
PD : Data to be programmed at word address.
$\overline{DQ}_7$: The output of the complement of the data written to the device.
D_{OUT} : The output of the data written to the device.

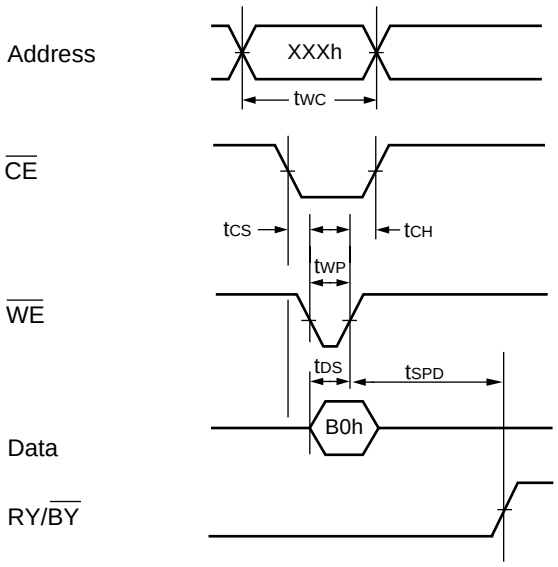
Note : Figure indicates the last two bus cycles out of four bus cycle sequence.

(6) Chip/Sector Erase Operation Timing Diagram

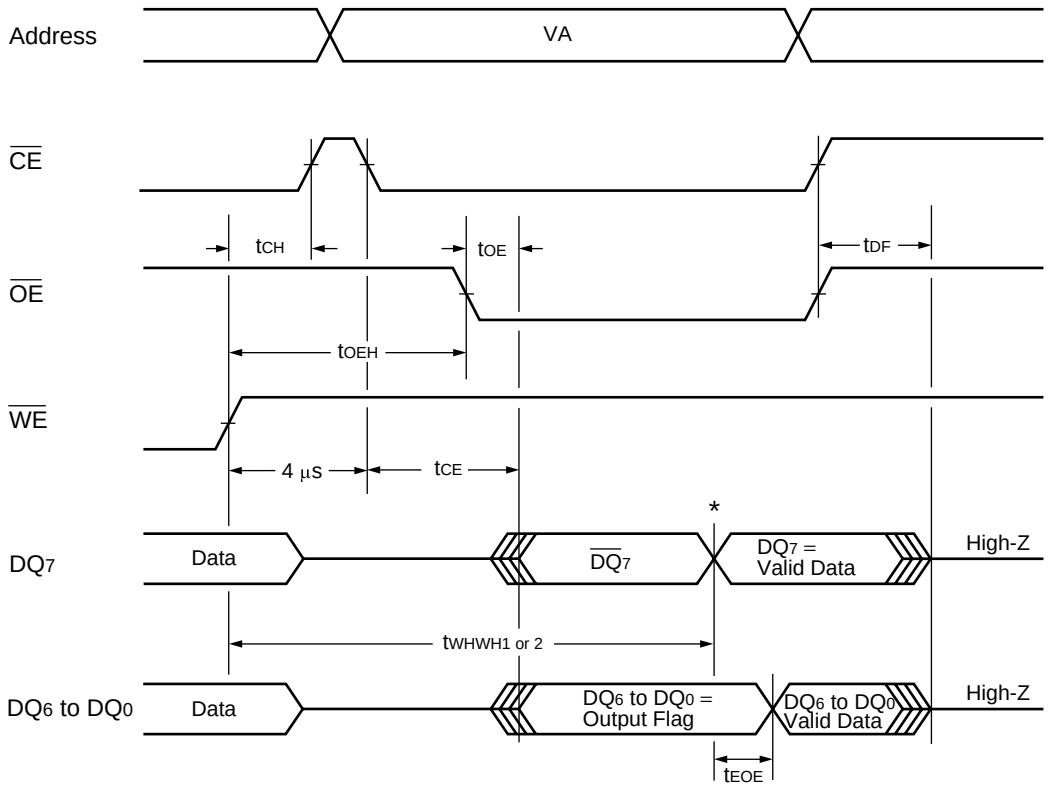


* : SA is the sector address for Sector Erase. Address = 555h (Word), AAAh (Byte) for Chip Erase.

(7) Erase Suspend Operation Timing Diagram



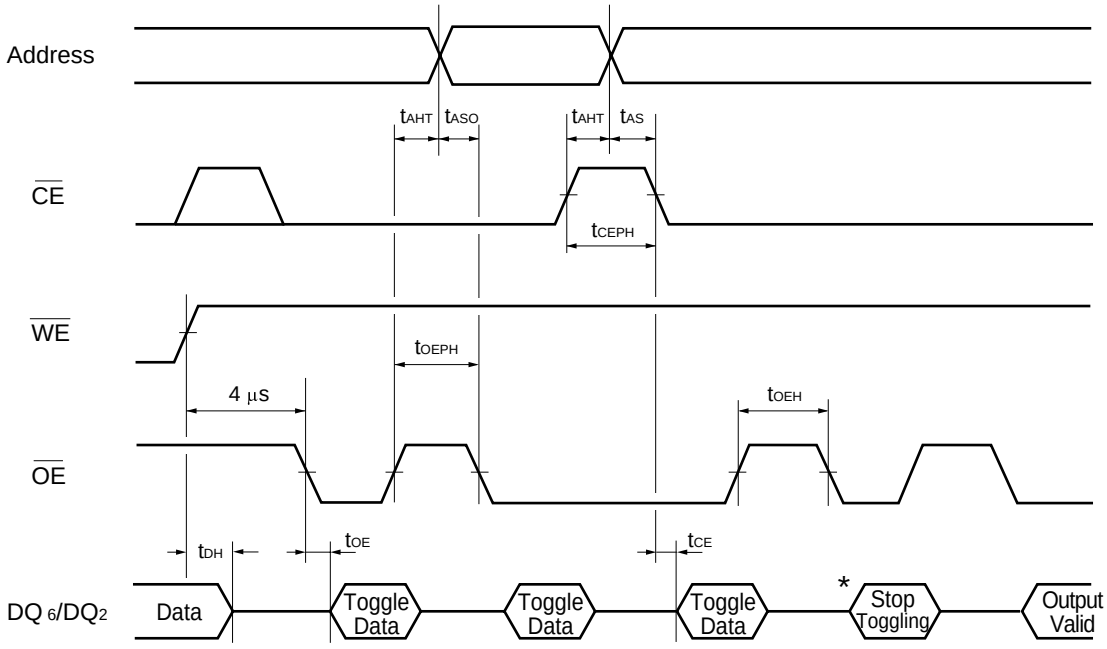
(8) $\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram



* : DQ_7 = Valid Data (The device has completed the Embedded operation.)

Note : When checking Hardware Sequence Flags during program operations, it should be checked 4 μs after issuing program command.

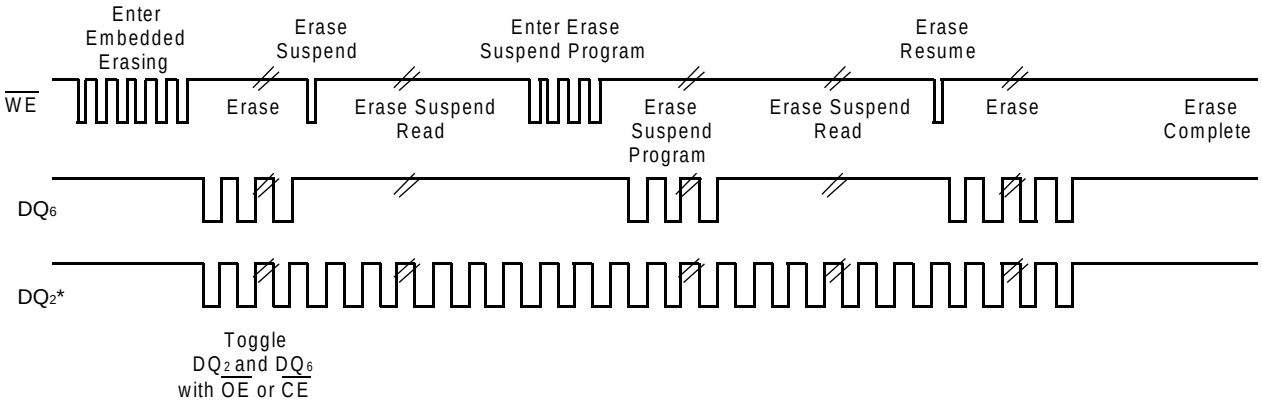
(9) Toggle Bit I Timing Diagram during Embedded Algorithm Operations



* : DQ_6 stops toggling (The device has completed the Embedded operation).

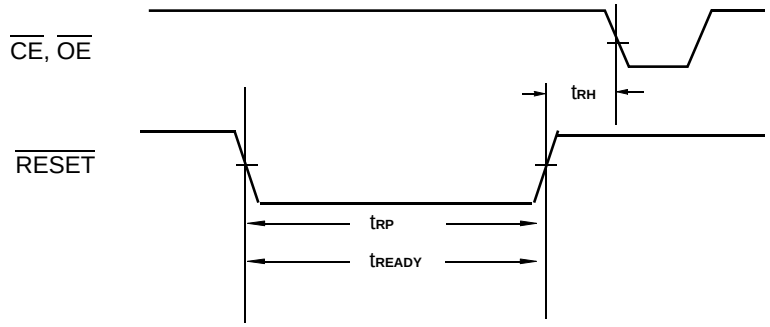
Note : When checking Hardware Sequence Flags during program operations, it should be checked 4 μs after issuing program command.

(10) DQ_2 vs. DQ_6

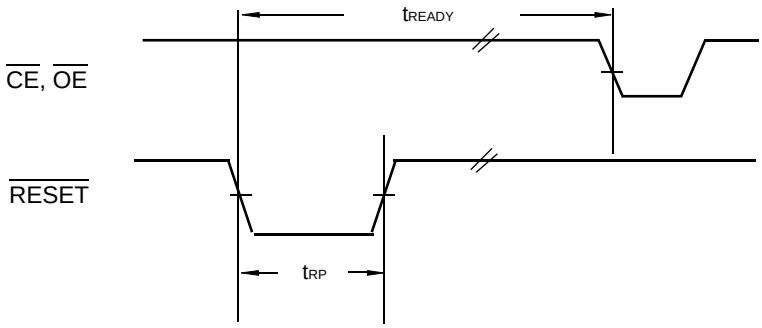


* : DQ_2 is read from the erase-suspended sector.

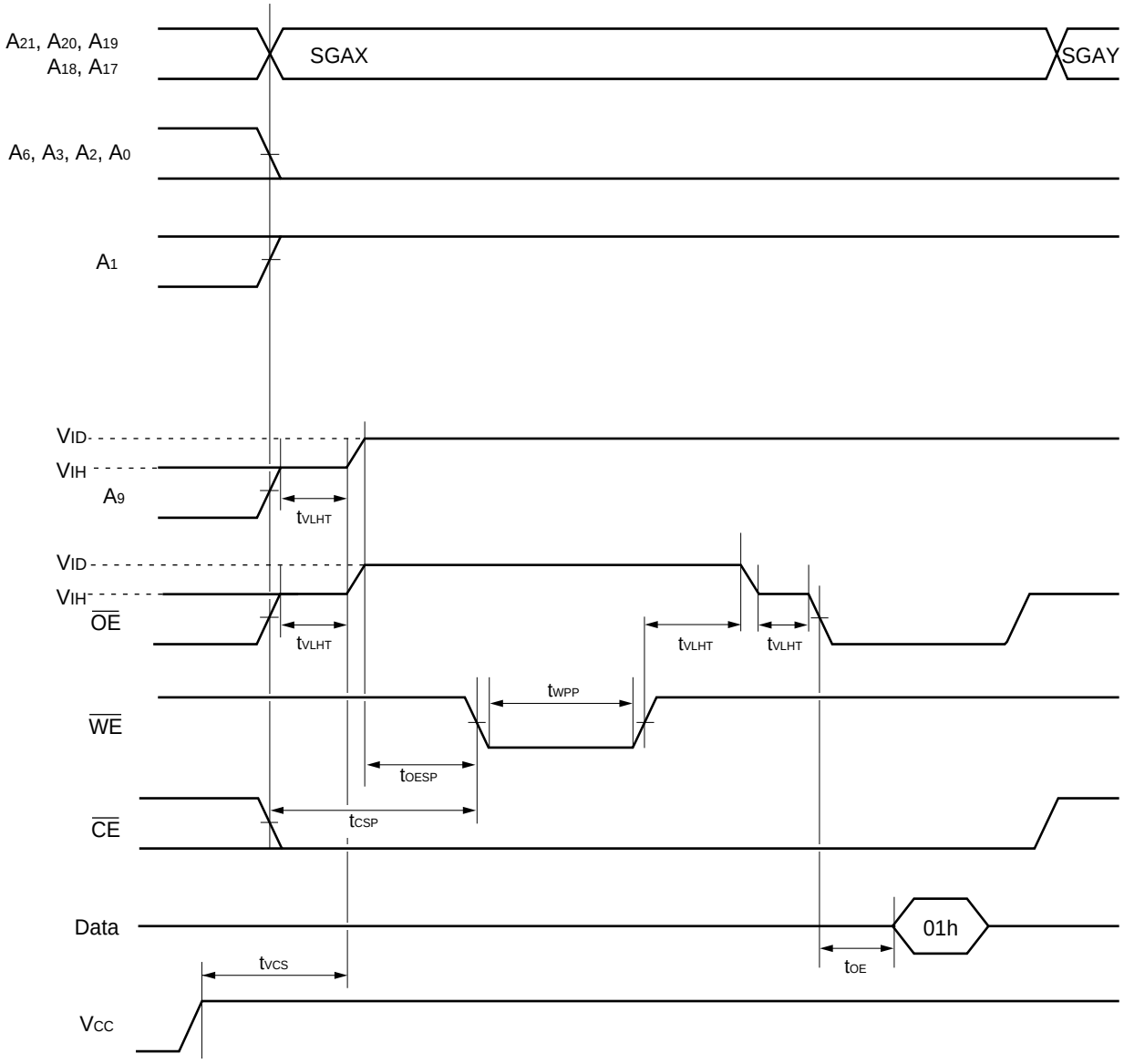
(11) $\overline{\text{RESET}}$ Timing Diagram (Not during Embedded Algorithms)



(12) $\overline{\text{RESET}}$ Timing Diagram (During Embedded Algorithms)

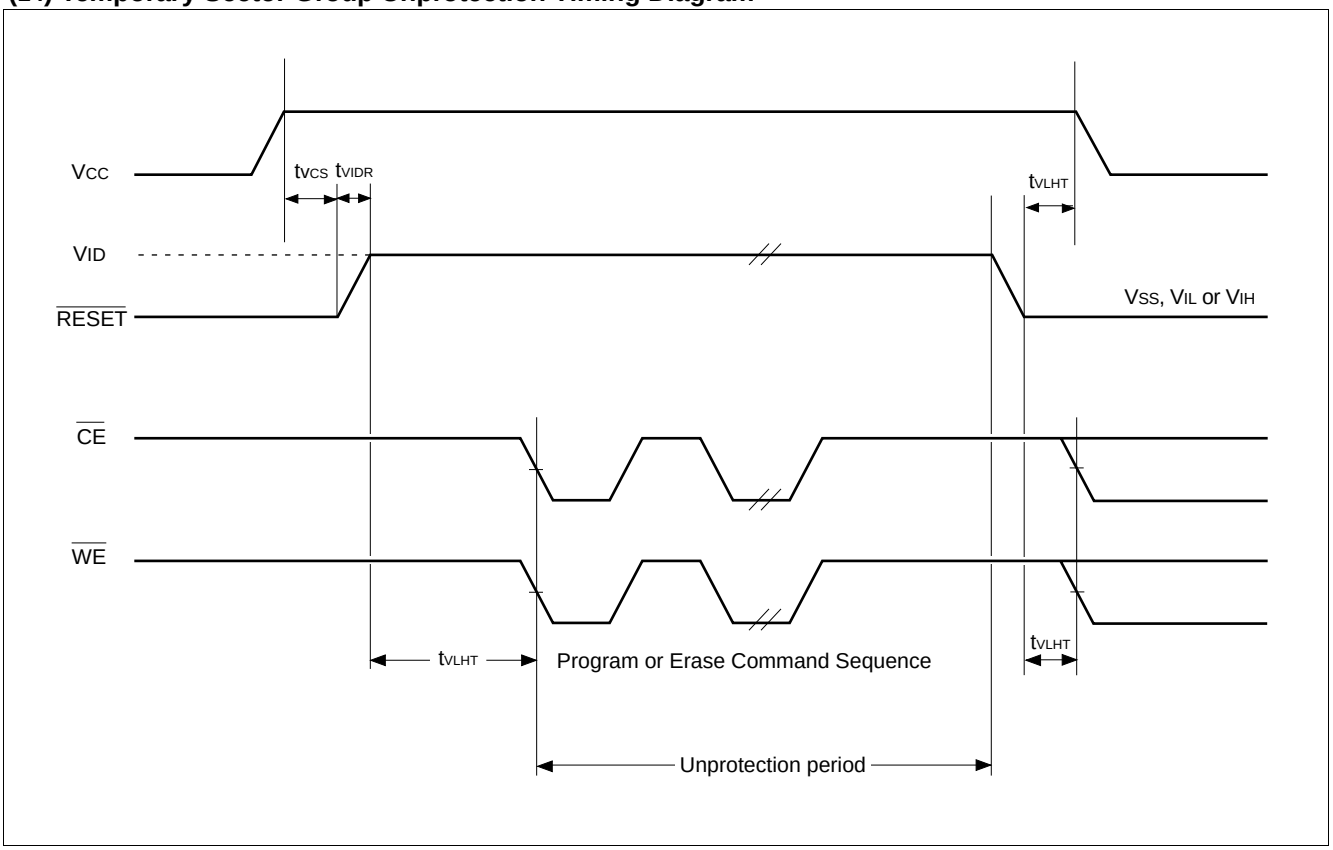


(13) Sector Group Protection Timing Diagram

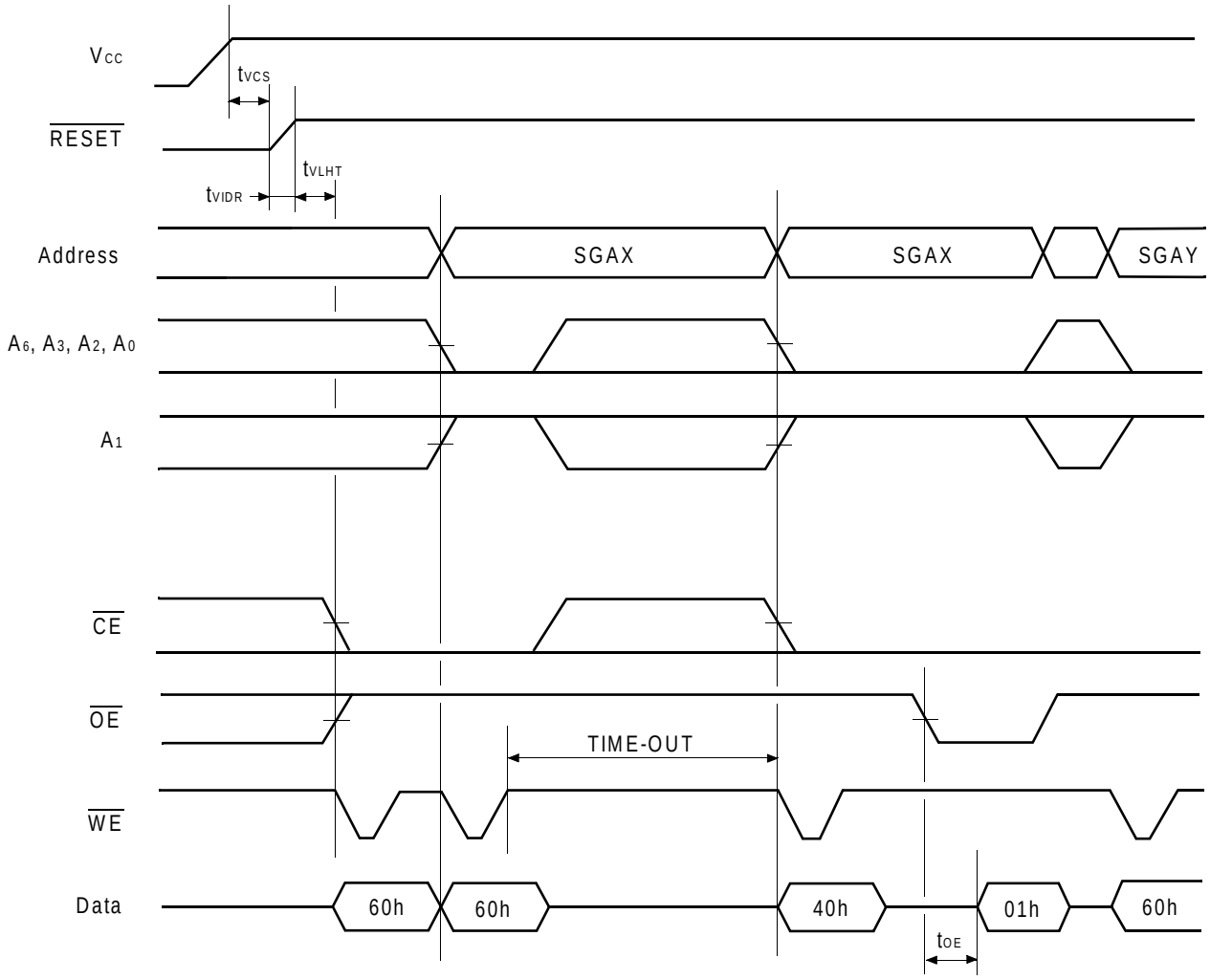


SGAX : Sector Group Address to be protected
SGAY : Next Sector Group Address to be protected

(14) Temporary Sector Group Unprotection Timing Diagram

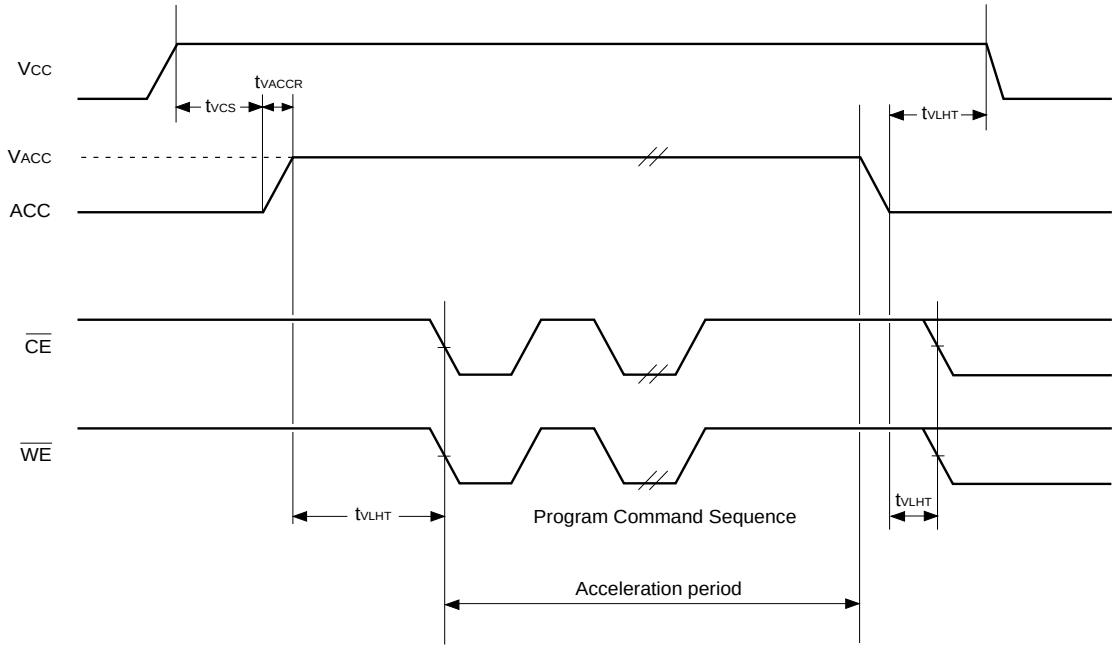


(15) Extended Sector Group Protection Timing Diagram



SGAX : Sector Group Address to be protected
SGAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 250 ms (Min)

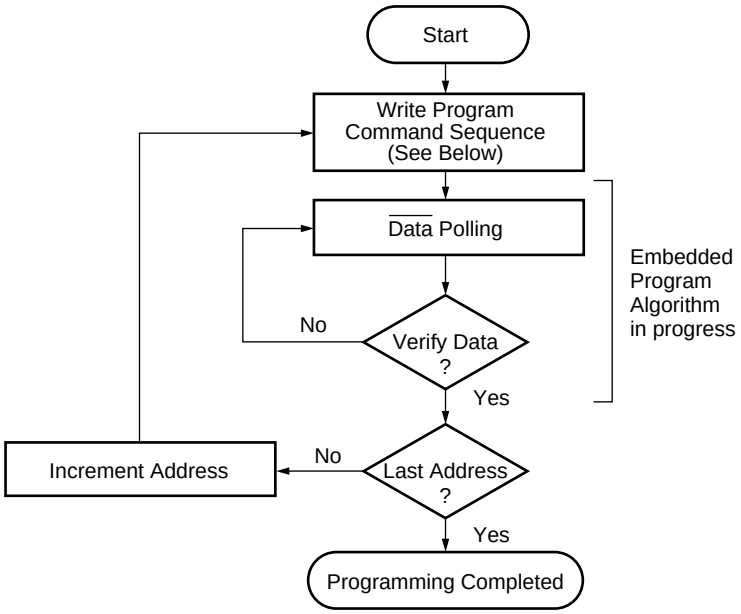
(16) Accelerated Program Timing Diagram



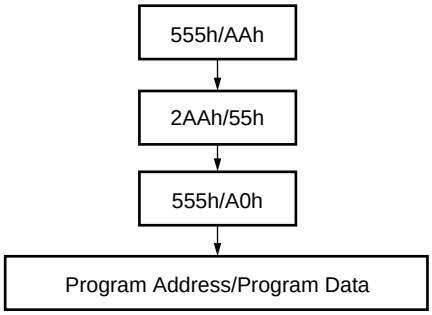
■ FLOW CHART

(1) Embedded Program™ Algorithm

EMBEDDED ALGORITHMS

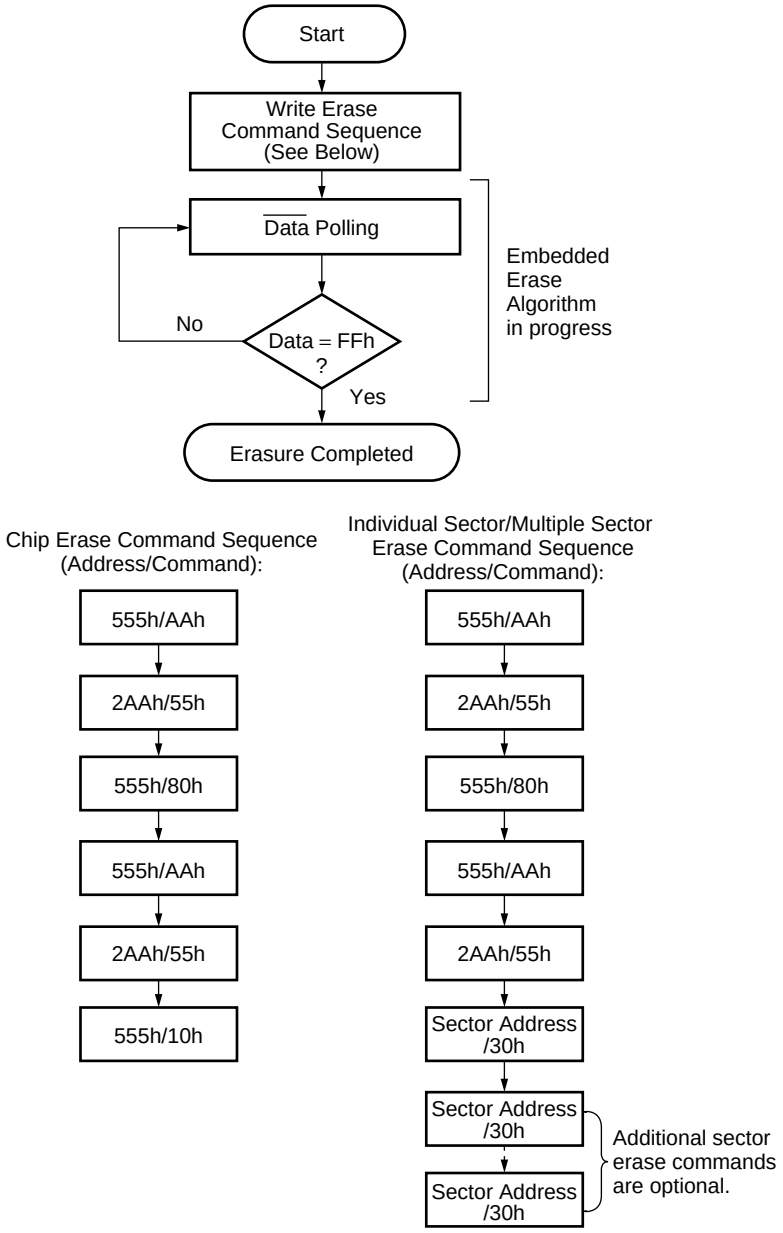


Program Command Sequence (Address/Command):

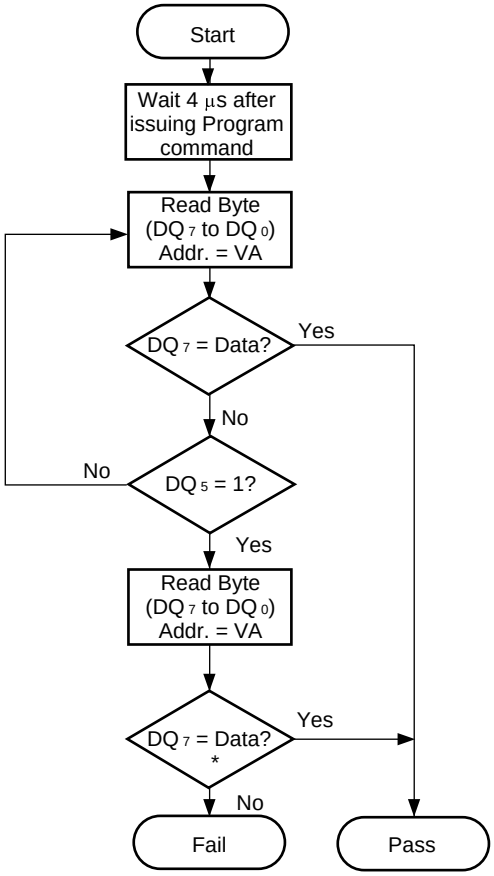


(2) Embedded Erase™ Algorithm

EMBEDDED ALGORITHMS



(3) $\overline{\text{Data}}$ Polling Algorithm

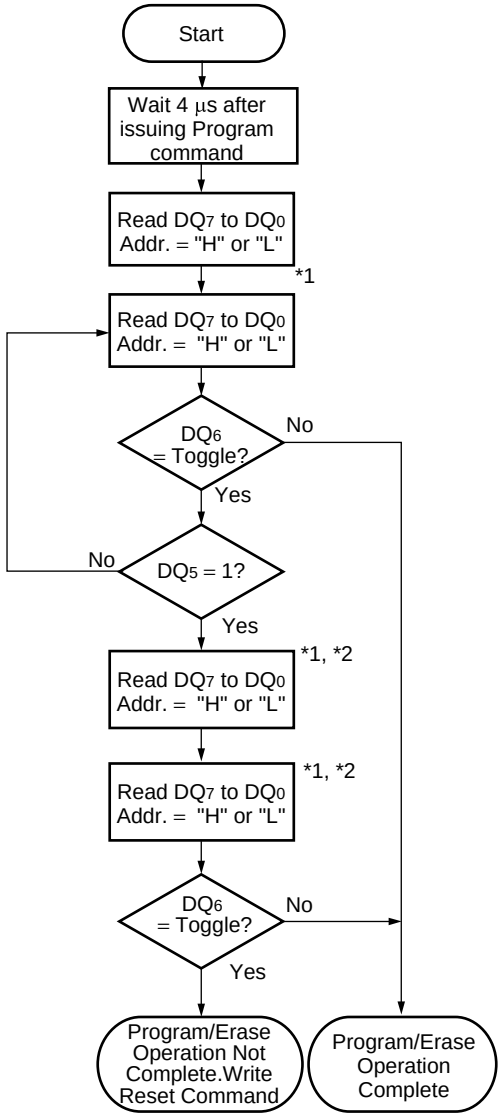


VA = Valid address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple sector erases operation
= Any of the sector addresses within the sector not being protected during chip erase operation

(There may not be accurate indications to determine that the data polling has been completed.)

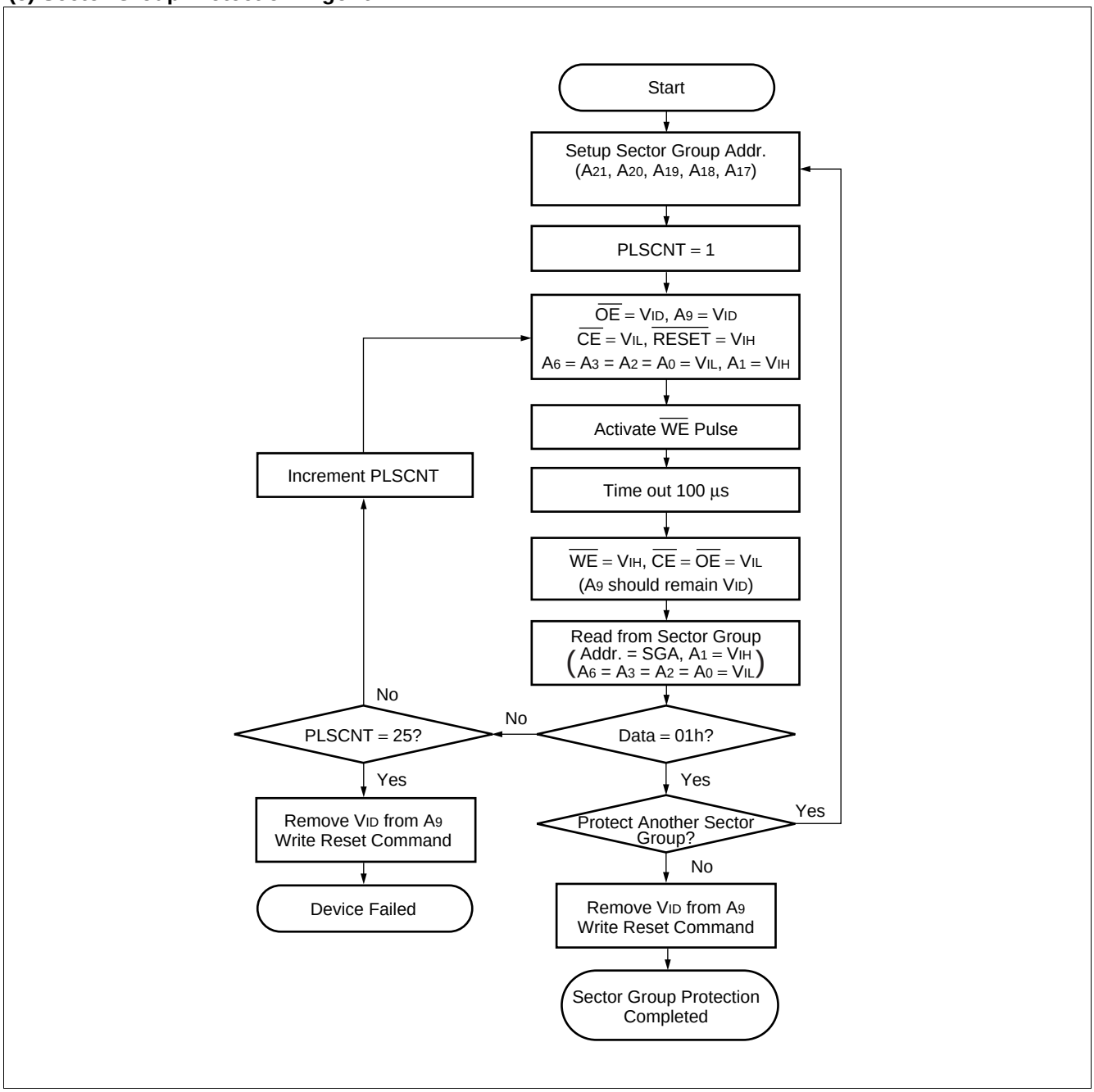
* : DQ_7 is rechecked even if DQ_5 = “1” because DQ_7 may change simultaneously with DQ_5.

(4) Toggle Bit Algorithm

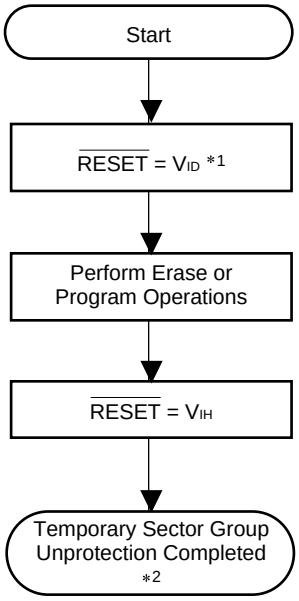


*1 : Read Toggle bit twice to determine whether it is toggling.
*2 : Recheck Toggle bit because it may stop toggling as DQ_5 changes to “1”.

(5) Sector Group Protection Algorithm

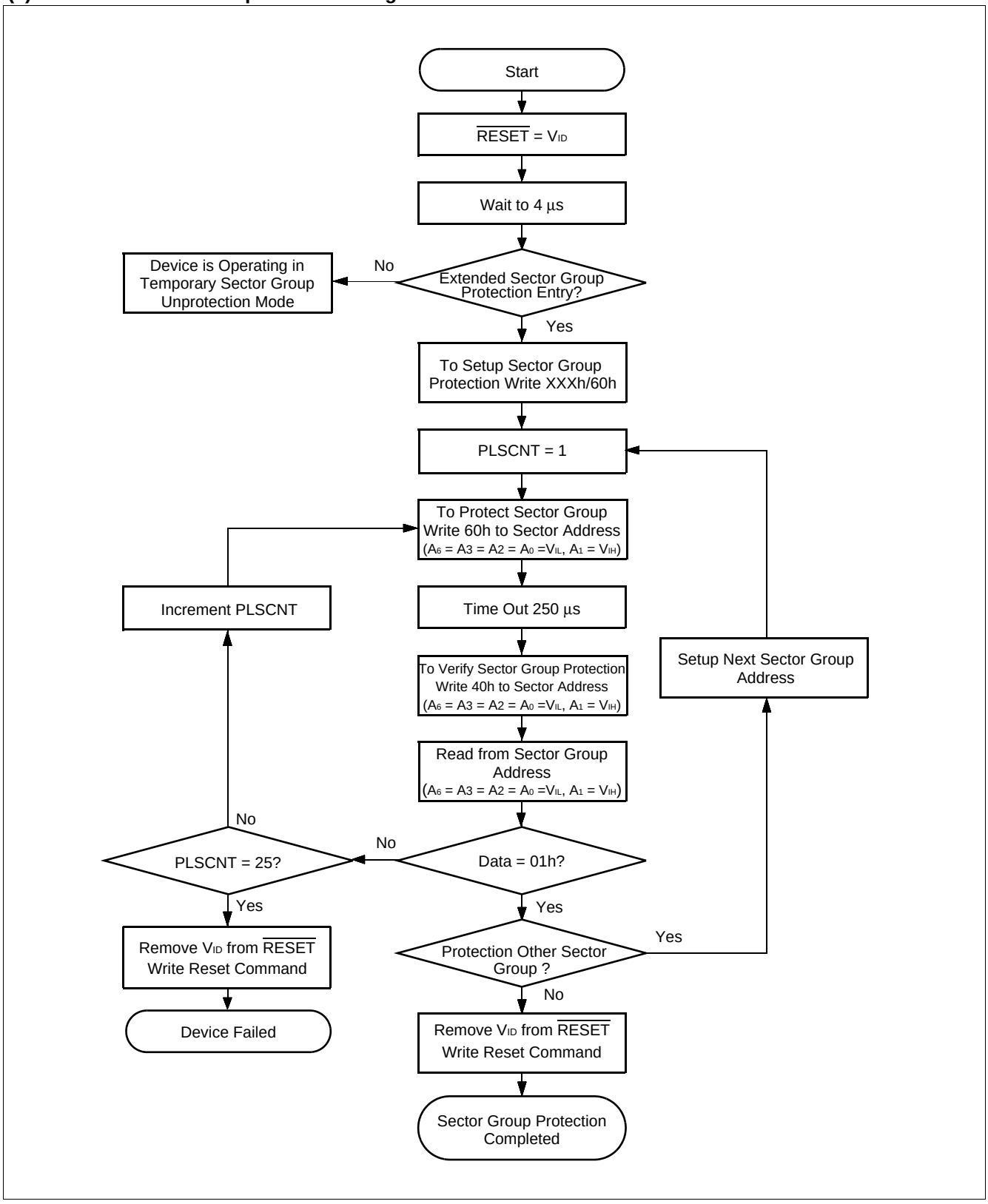


(6) Temporary Sector Group Unprotection Algorithm



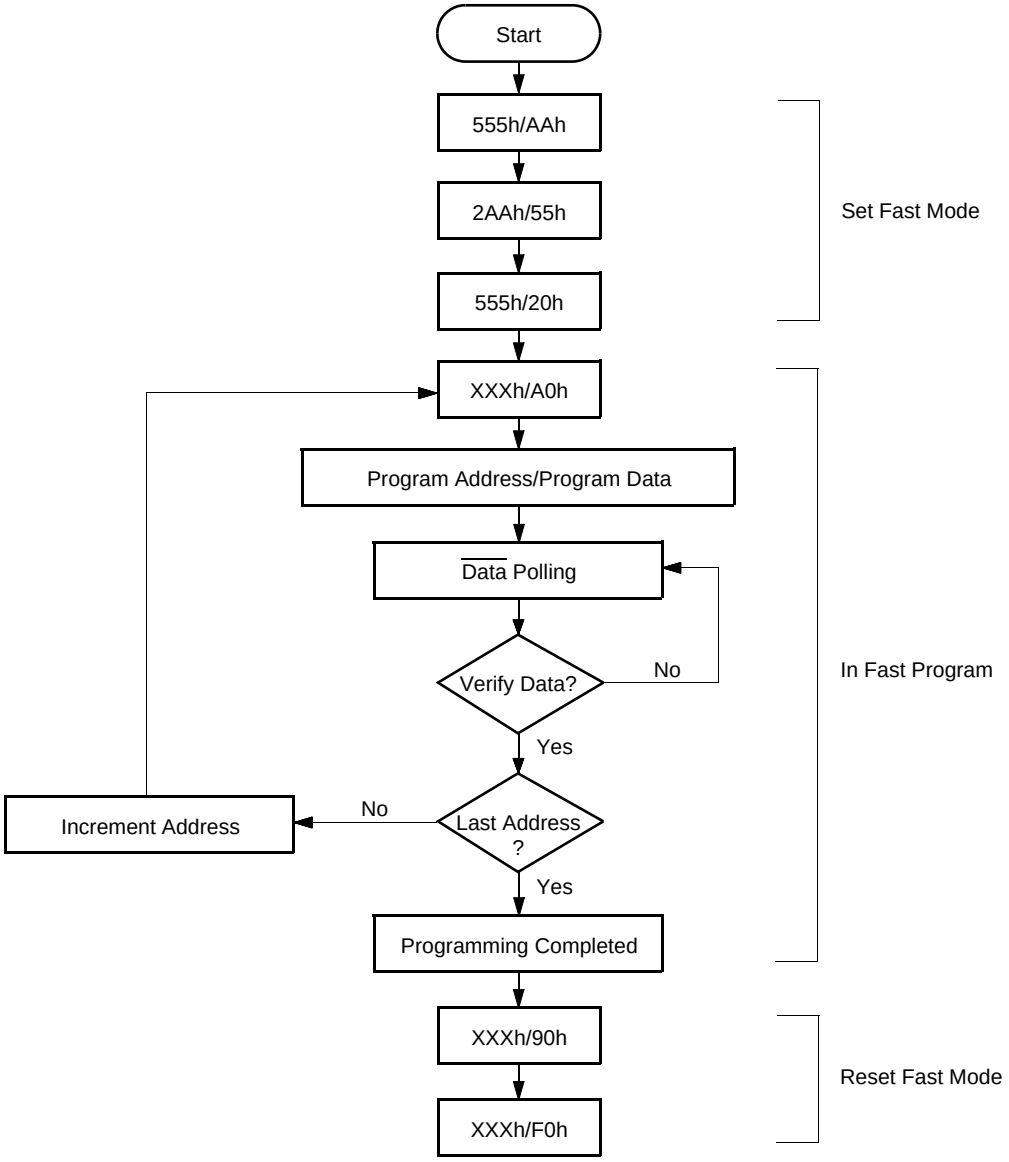
*1 : All protected sector groups are unprotected.
*2 : All previously protected sector groups are protected.

(7) Extended Sector Group Protection Algorithm



(8) Embedded Program™ Algorithm for Fast Mode

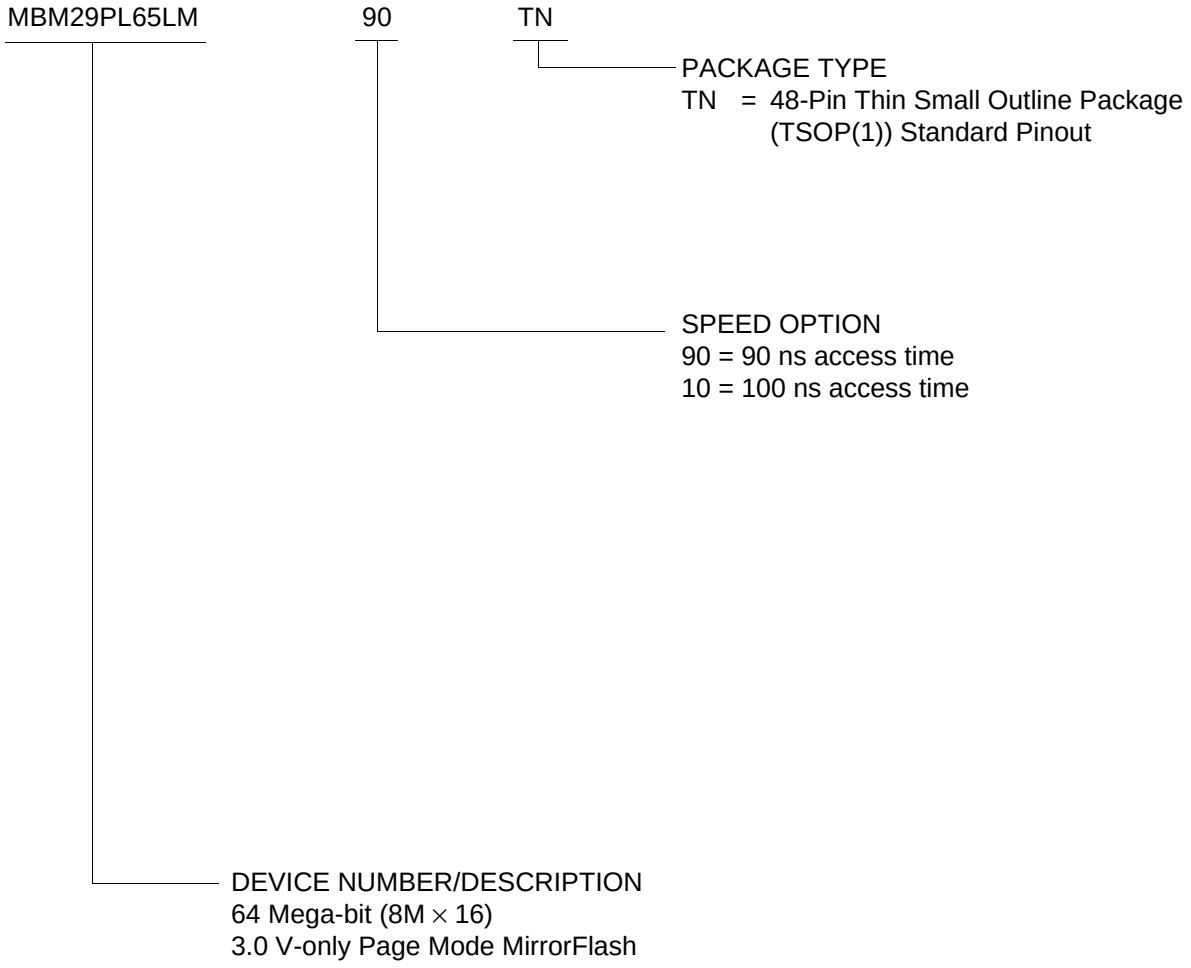
FAST MODE ALGORITHM



Note : The sequence is applied for Word (×16) mode.

■ ORDERING INFORMATION

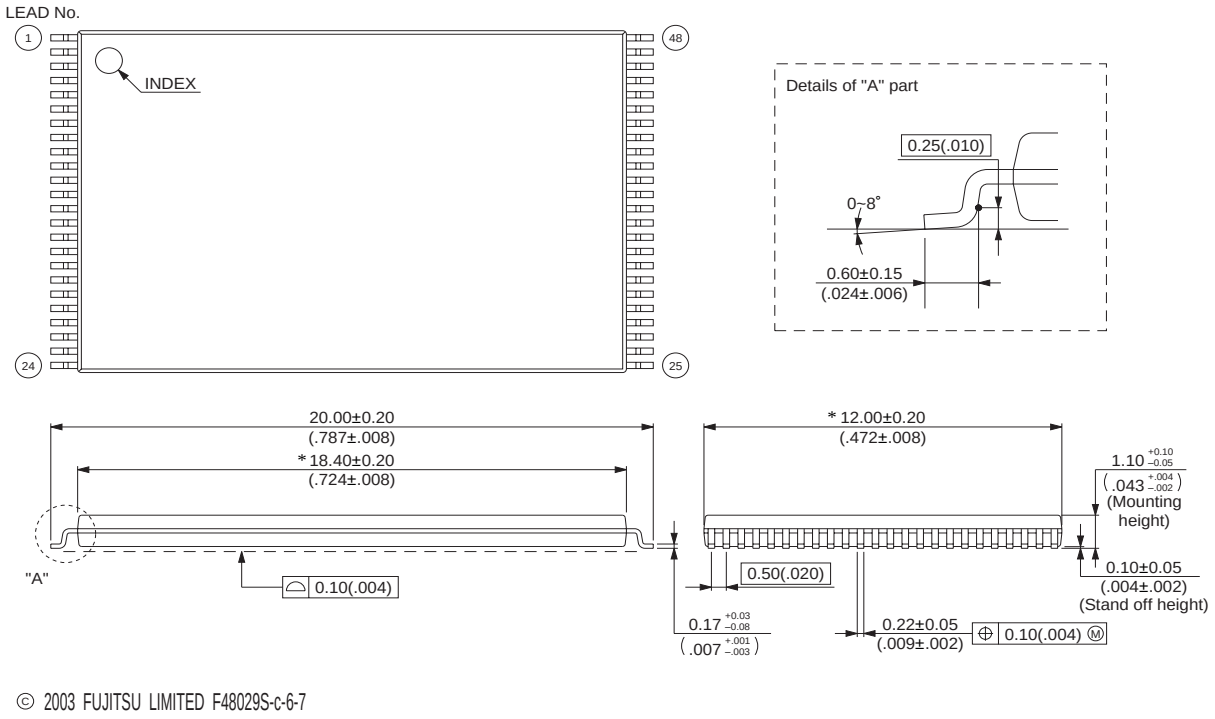
Part No.	Package	Access Time (ns)	Remarks
MBM29PL65LM90TN	48-pin, plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	90 ns	
MBM29PL65LM10TN		100 ns	



■ PACKAGE DIMENSION

48-pin plastic TSOP(1)
(FPT-48P-M19)

Note 1) * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15(.006)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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F0312