DS05-20891-4E

FLASH MEMORY

CMOS

16 M (2 M × 8/1 M × 16) BIT Dual Operation

MBM29DS163TE/BE10

■ DESCRIPTION

The MBM29DS163TE/BE is 16 M-bit, 1.8 V-only Flash memory organized as 2 M bytes of 8 bits each or 1 M words of 16 bits each. The device is offered in 48-pin TSOP (1) and 48-ball FBGA packages. This device is designed to be programmed in system with standard system 1.8 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

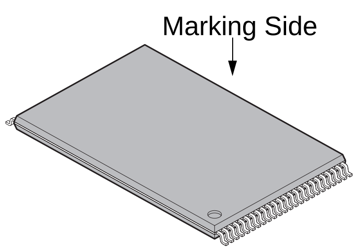
(Continued)

■ PRODUCT LINE UP

Part No.	MBM29DS163TE/BE10
Power Supply Voltage (V)	$V_{CC} = 2.0\ V^{+0.2\ V}_{-0.2\ V}$
Max Address Access Time (ns)	100
Max $\overline{CE}$ Access Time (ns)	100
Max $\overline{OE}$ Access Time (ns)	35

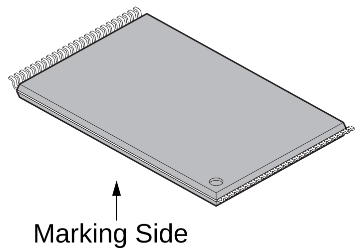
■ PACKAGES

48-pin plastic TSOP (1)



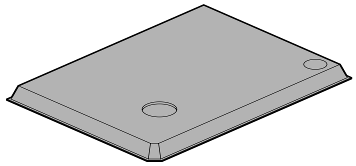
(FPT-48P-M19)

48-pin plastic TSOP (1)



(FPT-48P-M20)

48-ball plastic FBGA



(BGA-48P-M11)

FUJITSU

(Continued)

The device is organized into two banks, Bank 1 and Bank 2, which can be considered to be two separate memory arrays as far as certain operations are concerned. This device is the same as Fujitsu's standard 1.8 V only Flash memories with the additional capability of allowing a normal non-delayed read access from a non-busy bank of the array while an embedded write (either a program or an erase) operation is simultaneously taking place on the other bank.

The standard device offers access time 100 ns, allowing operation of high-speed microprocessors without wait state. To eliminate bus contention the device has separate chip enable ($\overline{CE}$) , write enable ($\overline{WE}$) , and output enable ($\overline{OE}$) controls.

The device is pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The device is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This invokes the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verify proper cell margin.

A sector is typically erased and verified in 1.0 second (if already completely preprogrammed) .

The device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The device is erased when shipped from the factory.

The device features single 1.8 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{Data}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the RY/$\overline{BY}$ output pin. Once the end of a program or erase cycle is completed, the device internally resets to the read mode.

The device also has a hardware $\overline{RESET}$ pin. When this pin is driven low, execution of any Embedded Program Algorithm or Embedded Erase Algorithm is terminated. The internal state machine is then reset to the read mode. The $\overline{RESET}$ pin may be tied to the system reset circuitry. Therefore, if a system reset occurs during the Embedded Program Algorithm or Embedded Erase Algorithm, the device is automatically reset to the read mode and will have erroneous data stored in the address locations being programmed or erased. These locations need re-writing after the Reset. Resetting the device enables the system's microprocessor to read the boot-up firmware from the Flash memory.

Fujitsu's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The device memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

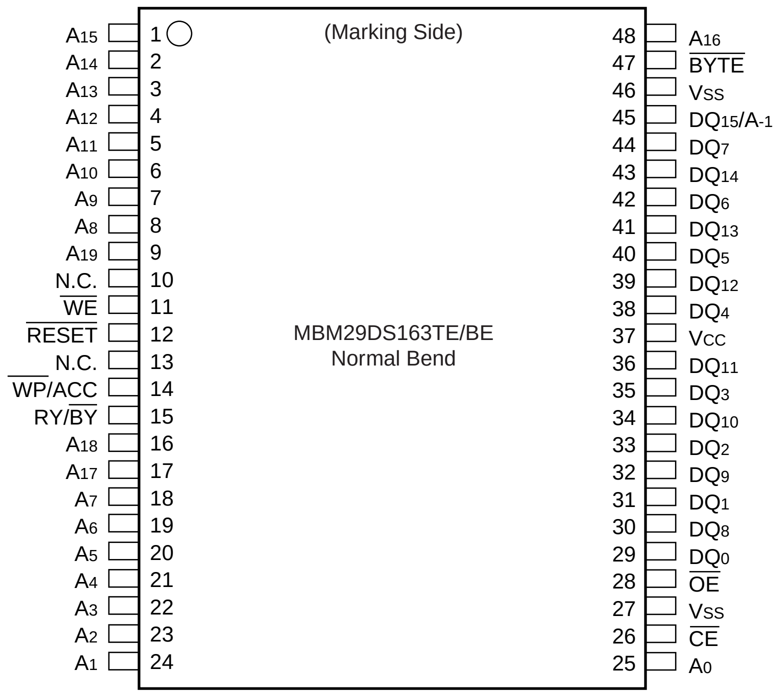
■ FEATURES

- **0.23 µm Process Technology**
- **Simultaneous Read/Write Operations (Dual Bank)**
  Host system can program or erase in one bank, and then read immediately and simultaneously from the other bank with zero latency between read and write operations
  Read-while-erase
  Read-while-program
- **Single 1.8 V Read, Program, and Erase**
  Minimized system level power requirements
- **Compatible with JEDEC-standard Commands**
  Use the same software commands as E^2PROMs
- **Compatible with JEDEC-standard Worldwide Pinouts**
  48-pin TSOP (1) (Package suffix : TN – Normal Bend Type, TR – Reversed Bend Type)
  48-ball FBGA (Package suffix : PBT)
- **Minimum 100,000 Program/Erase Cycles**
- **High Performance**
  100 ns maximum access time
- **Sector Erase Architecture**
  Eight 4 K word and thirty-one 32 K word sectors in word mode
  Eight 8 K byte and thirty-one 64 K byte sectors in byte mode
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **HiddenROM Region**
  64 K byte of HiddenROM, accessible through a new “HiddenROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC Input Pin**
  At V_{IL}, allows protection of boot sectors, regardless of sector protection/unprotection status
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, increases program performance
- **Embedded Erase™* Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™* Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Program Suspend/Resume**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Sector Group Protection**
  Hardware method disables any combination of sector groups from program or erase operations
- **Sector Group Protection Set function by Extended sector group protection command**
- **Fast Programming Function by Extended Command**
- **Temporary Sector Group Unprotection**
  Temporary sector group unprotection via the $\overline{\text{RESET}}$ pin.
- **In accordance with CFI (<u>C</u>ommon <u>F</u>lash Memory <u>I</u>nterface)**

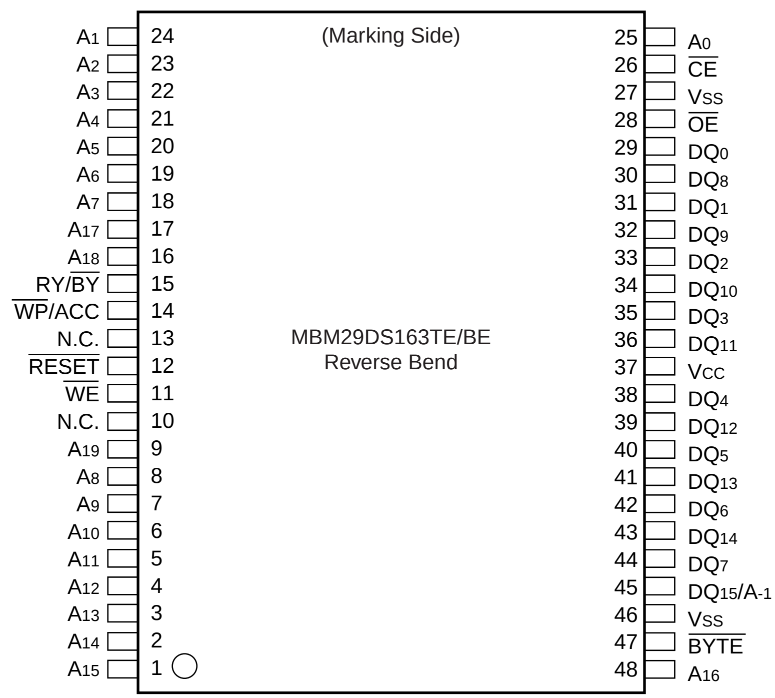
*: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

■ PIN ASSIGNMENTS

TSOP (1)



(FPT-48P-M19)



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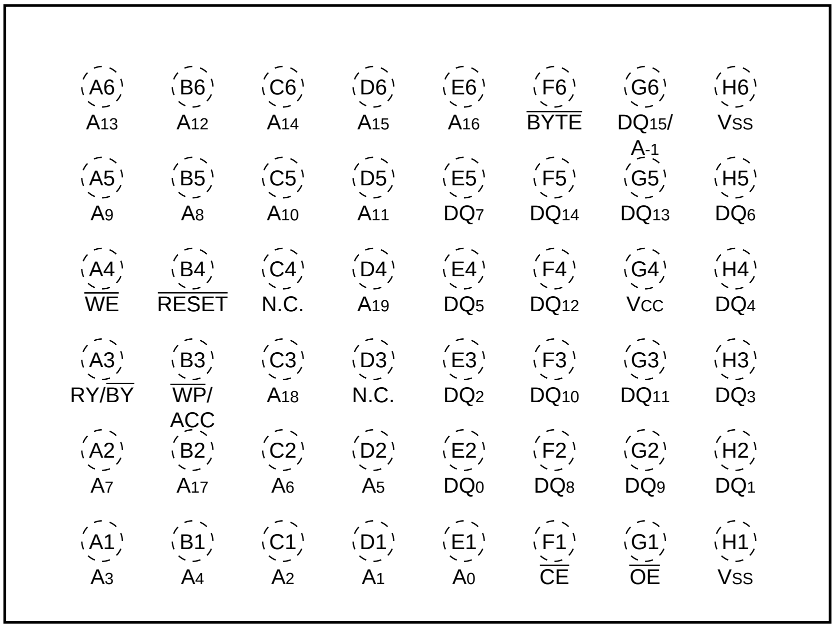
FBGA
(TOP VIEW)
Marking Side

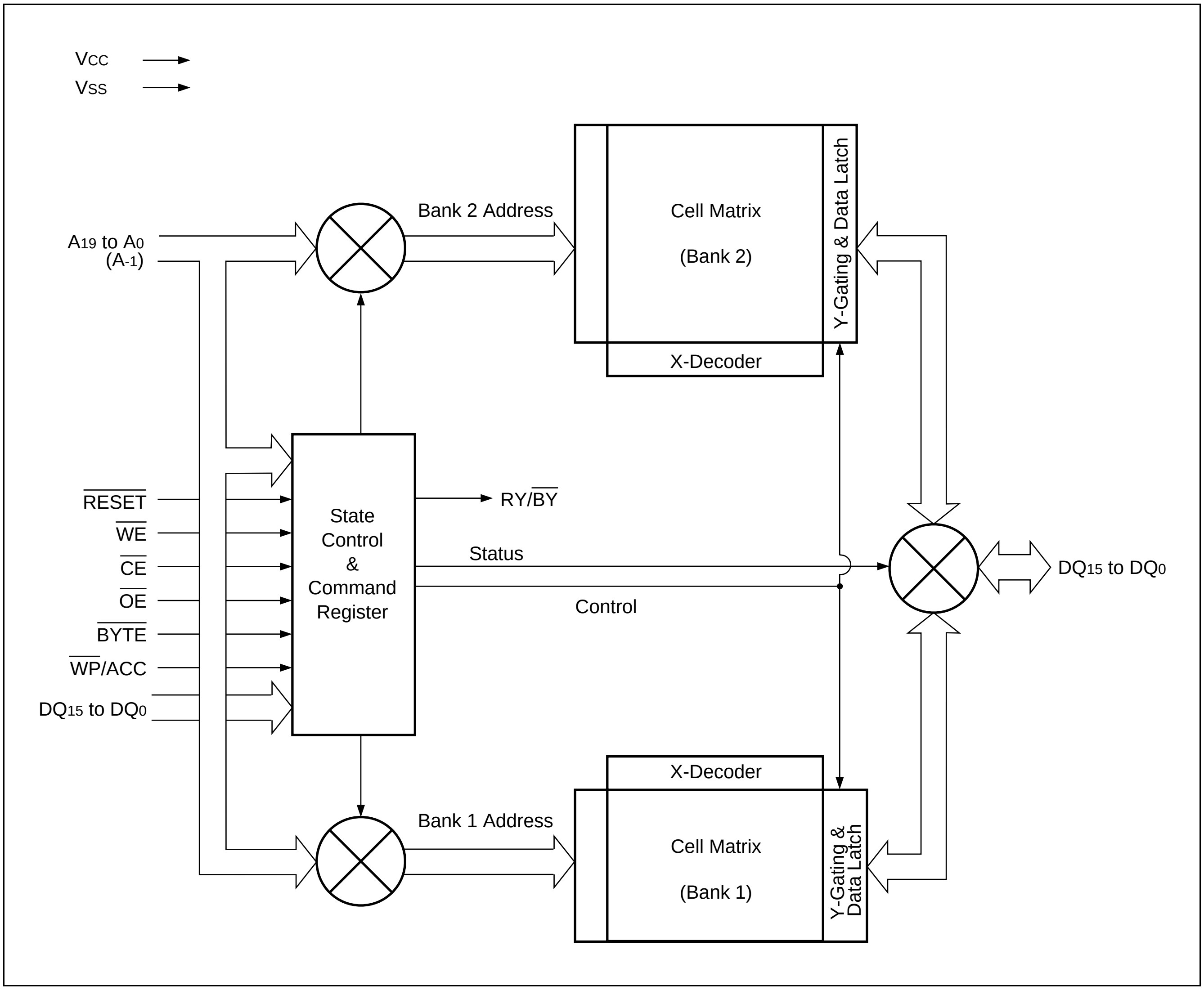


(BGA-48P-M11)

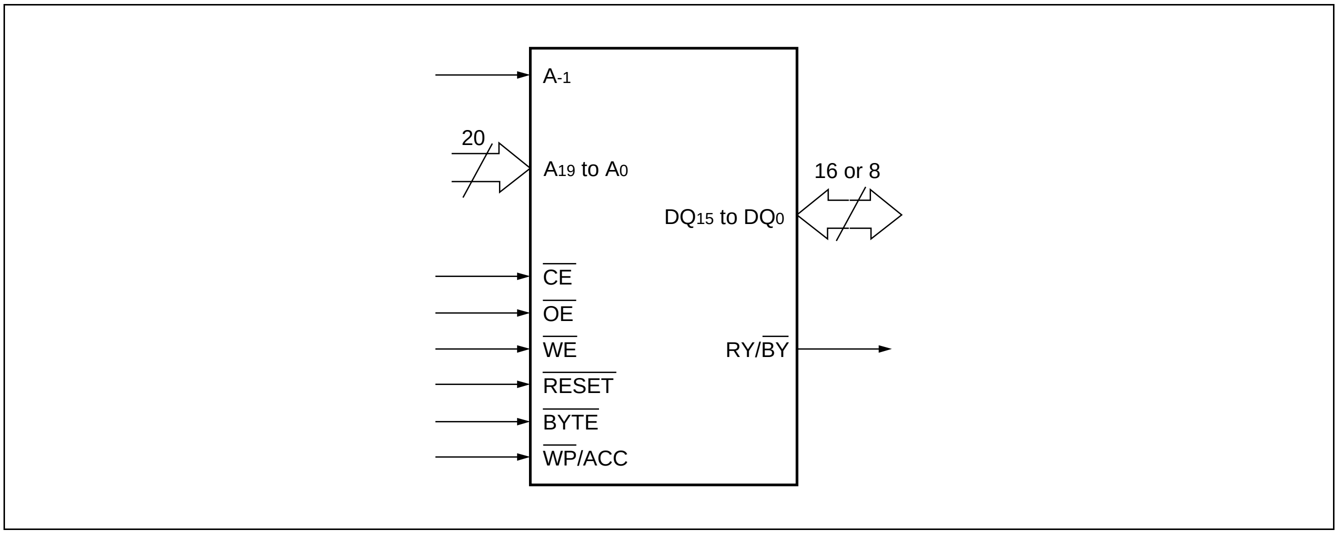
■ PIN DESCRIPTION

Pin	Function
A_{19} to A_0, A_{-1}	Address Inputs
DQ_{15} to DQ_0	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Group Unprotection
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
$\overline{WP}$/ACC	Hardware Write Protection/Program Acceleration
N.C.	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply

■ BLOCK DIAGRAM



■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

MBM29DS163TE/BE User Bus Operations ($\overline{BYTE} = V_{IH}$) Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_{15} to DQ_0	$\overline{RESET}$	$\overline{WP}$/ACC
Auto-Select Manufacturer Code*1	L	L	H	L	L	L	V_{ID}	Code	H	X
Auto-Select Device Code*1	L	L	H	H	L	L	V_{ID}	Code	H	X
Read*3	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H	X
Standby	H	X	X	X	X	X	X	High-Z	H	X
Output Disable	L	H	H	X	X	X	X	High-Z	H	X
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H	X
Enable Sector Group Protection*2, *4	L	V_{ID}	¯|_|¯	L	H	L	V_{ID}	X	H	X
Verify Sector Group Protection*2, *4	L	L	H	L	H	L	V_{ID}	Code	H	X
Temporary Sector Group Unprotection*5	X	X	X	X	X	X	X	X	V_{ID}	X
Reset (Hardware) /Standby	X	X	X	X	X	X	X	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	L

MBM29DS163TE/BE User Bus Operations ($\overline{BYTE} = V_{IL}$) Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{15}/A_{-1}	A_0	A_1	A_6	A_9	DQ_7 to DQ_0	$\overline{RESET}$	$\overline{WP}$/ACC
Auto-Select Manufacturer Code*1	L	L	H	L	L	L	L	V_{ID}	Code	H	X
Auto-Select Device Code*1	L	L	H	L	H	L	L	V_{ID}	Code	H	X
Read*3	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}	H	X
Standby	H	X	X	X	X	X	X	X	High-Z	H	X
Output Disable	L	H	H	X	X	X	X	X	High-Z	H	X
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	D_{IN}	H	X
Enable Sector Group Protection *2, *4	L	V_{ID}	¯|_|¯	L	L	H	L	V_{ID}	X	H	X
Verify Sector Group Protection*2, *4	L	L	H	L	L	H	L	V_{ID}	Code	H	X
Temporary Sector Group Unprotection*5	X	X	X	X	X	X	X	X	X	V_{ID}	X
Reset (Hardware) /Standby	X	X	X	X	X	X	X	X	High-Z	L	X
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	L

Legend : L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ¯|_|¯ = Pulse input. See DC Characteristics for voltage levels.

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. See "MBM29DS163TE/BE Command Definitions" Table.

*2 : Refer to the section on Sector Group Protection.

*3 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4 : V_{CC} must be between the minimum and maximum of the operation range.

*5 : Also used for the extended sector group protection.

MBM29DS163TE/BE Command Definitions Table

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset*1	Word	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/Reset*1	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA*7	RD*7	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect	Word	3	555h	AAh	2AAh	55h	(BA) 555h	90h	IA*7	ID*7	—	—	—	—
	Byte		AAAh		555h		(BA) AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Program Suspend		1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Program Resume		1	BA	30h	—	—	—	—	—	—	—	—	—	—
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Erase Suspend		1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	BA	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Fast Program*2	Word	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXXh											
Reset from Fast Mode*2	Word	2	BA	90h	XXXh	*6 F0h	—	—	—	—	—	—	—	—
	Byte		BA		XXXh									
Extended Sector Group Protection*3	Word	3	XXXh	60h	SPA	60h	SPA	40h	SPA*7	SD*7	—	—	—	—
	Byte													
Query*4	Word	1	55h	98h	—	—	—	—	—	—	—	—	—	—
	Byte		AAh											
HiddenROM Entry	Word	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
HiddenROM Program*5	Word	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							

(Continued)

(Continued)

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
HiddenROM Erase*5	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	HRA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
HiddenROM Exit*5	Word	4	555h	AAh	2AAh	55h	(HRBA) 555h	90h	XXXh	00h	—	—	—	—
	Byte		AAAh		555h		(HRBA) AAAh							

*1 : Both of these reset commands one equivalent.

*2 : This command is valid while Fast Mode.

*3 : This command is valid while $\overline{\text{RESET}}$ = V_{ID}.

*4 : The valid addresses are A_6 to A_0.

*5 : This command is valid while HiddenROM mode.

*6 : The data "00h" is also acceptable.

*7 : The fourth bus cycle is only for read.

Notes :
- Address bits A_{19} to A_{11} = X = "H" or "L" for all address commands except or Program Address (PA) , Sector Address (SA) , and Bank Address (BA) .
- Bus operations are defined in "MBM29DS163TE/BE User Bus Operation ($\overline{\text{BYTE}}$ = V_{IH})" Table and "MBM29DS163TE/BE User Bus Operation ($\overline{\text{BYTE}}$ = V_{IL})" Table.
- RA = Address of the memory location to be read
  IA = Autoselect read address sets both the bank address specified at (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}) and all the other A_6, A_1, A_0, (A_{-1}) .
  PA = Address of the memory location to be programmed
  Addresses are latched on the falling edge of the write pulse.
  SA = Address of the sector to be erased. The combination of A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
  BA = Bank Address (A_{19} to A_{15})
- RD = Data read from location RA during read operation.
  ID = Device code/manufacture code for the address located by IA.
  PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- SPA = Sector group address to be protected. Set sector group address (SGA) and (A_6, A_1, A_0) = (0, 1, 0) .
  SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.
- HRA = Address of the HiddenROM area
  29DS163TE (Top Boot Type) Word Mode : 0F8000h to 0FFFFFh
  Byte Mode : 1F0000h to 1FFFFFh
  29DS163BE (Bottom Boot Type) Word Mode : 000000h to 007FFFh
  Byte Mode : 000000h to 00FFFFh
- HRBA = Bank Address of the HiddenROM area
  29DS163TE (Top Boot Type) : $A_{19} = A_{18} = A_{17} = A_{16} = A_{15} = V_{IH}$
  29DS163BE (Bottom Boot Type) : $A_{19} = A_{18} = A_{17} = A_{16} = A_{15} = V_{IL}$
- The system should generate the following address patterns :
  Word Mode : 555h or 2AAh to addresses A_{10} to A_0
  Byte Mode : AAAh or 555h to addresses A_{10} to A_0, and A_{-1}

- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
- Command combinations not described in “MBM29DS163TE/BE Command Definitions” Table are illegal.

MBM29DS163TE/BE Sector Group Protection Verify Autoselect Codes Table

Type			A_{19} to A_{12}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture's Code			BA*3	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MBM29DS163TE	Byte	BA*3	V_{IL}	V_{IL}	V_{IH}	V_{IL}	95h
		Word					X	2295h
	MBM29DS163BE	Byte	BA*3	V_{IL}	V_{IL}	V_{IH}	V_{IL}	96h
		Word					X	2296h
Extend Code	MBM29DS163TE/BE	Byte	BA*3	V_{IL}	V_{IH}	V_{IH}	V_{IL}	05h
		Word					X	2205h
Sector Group Protection			Sector Group Addresses	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h*2

*1 : A_{-1} is for Byte mode.

*2 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*3 : BA is Bank Address which is needed only in Command Autoselect mode.

Expanded Autoselect Code Table

Type			Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code			04h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29DS 163TE	(B)	95h	A_{-1}	HZ	HZ	HZ	HZ	HZ	HZ	HZ	1	0	0	1	0	1	0	1
		(W)	2295h	0	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1
	MBM29DS 163BE	(B)	96h	A_{-1}	HZ	HZ	HZ	HZ	HZ	HZ	HZ	1	0	0	1	0	1	1	0
		(W)	2296h	0	0	1	0	0	0	1	0	1	0	0	1	0	1	1	0
Extend Code	MBM29DS 163TE/BE	(B)	05h	A_{-1}	HZ	HZ	HZ	HZ	HZ	HZ	HZ	0	0	0	0	0	1	0	1
		(W)	2205h	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	1
Sector Group Protection			01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B) : Byte mode
(W) : Word mode
HZ : High-Z

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

Sector Address Table (MBM29DS163TE)

Bank	Sec-tor	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address										
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
Bank 2	SA0	0	0	0	0	0	X	X	X	64/32	000000h to 00FFFFh	000000h to 007FFFh
	SA1	0	0	0	0	1	X	X	X	64/32	010000h to 01FFFFh	008000h to 00FFFFh
	SA2	0	0	0	1	0	X	X	X	64/32	020000h to 02FFFFh	010000h to 017FFFh
	SA3	0	0	0	1	1	X	X	X	64/32	030000h to 03FFFFh	018000h to 01FFFFh
	SA4	0	0	1	0	0	X	X	X	64/32	040000h to 04FFFFh	020000h to 027FFFh
	SA5	0	0	1	0	1	X	X	X	64/32	050000h to 05FFFFh	028000h to 02FFFFh
	SA6	0	0	1	1	0	X	X	X	64/32	060000h to 06FFFFh	030000h to 037FFFh
	SA7	0	0	1	1	1	X	X	X	64/32	070000h to 07FFFFh	038000h to 03FFFFh
	SA8	0	1	0	0	0	X	X	X	64/32	080000h to 08FFFFh	040000h to 048000h
	SA9	0	1	0	0	1	X	X	X	64/32	090000h to 09FFFFh	048000h to 04FFFFh
	SA10	0	1	0	1	0	X	X	X	64/32	0A0000h to 0AFFFFh	050000h to 058000h
	SA11	0	1	0	1	1	X	X	X	64/32	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA12	0	1	1	0	0	X	X	X	64/32	0C0000h to 0CFFFFh	060000h to 068000h
	SA13	0	1	1	0	1	X	X	X	64/32	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA14	0	1	1	1	0	X	X	X	64/32	0E0000h to 0EFFFFh	070000h to 078FFFh
	SA15	0	1	1	1	1	X	X	X	64/32	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA16	1	0	0	0	0	X	X	X	64/32	100000h to 10FFFFh	080000h to 088000h
	SA17	1	0	0	0	1	X	X	X	64/32	110000h to 11FFFFh	088000h to 08FFFFh
	SA18	1	0	0	1	0	X	X	X	64/32	120000h to 12FFFFh	090000h to 098000h
	SA19	1	0	0	1	1	X	X	X	64/32	130000h to 13FFFFh	098000h to 09FFFFh
	SA20	1	0	1	0	0	X	X	X	64/32	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA21	1	0	1	0	1	X	X	X	64/32	150000h to 15FFFFh	0A8000h to 00AFFFh
	SA22	1	0	1	1	0	X	X	X	64/32	160000h to 16FFFFh	0B0000h to 0B7000h
	SA23	1	0	1	1	1	X	X	X	64/32	170000h to 17FFFFh	0B8000h to 0BFFFFh

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Bank	Sec-tor	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address										
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
Bank 1	SA24	1	1	0	0	0	X	X	X	64/32	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA25	1	1	0	0	1	X	X	X	64/32	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA26	1	1	0	1	0	X	X	X	64/32	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA27	1	1	0	1	1	X	X	X	64/32	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA28	1	1	1	0	0	X	X	X	64/32	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA29	1	1	1	0	1	X	X	X	64/32	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA30	1	1	1	1	0	X	X	X	64/32	1E0000h to 1EFFFFh	0F0000h to 0F7000h
	SA31	1	1	1	1	1	0	0	0	8/4	1F0000h to 1F1FFFh	0F8000h to 0F8FFFh
	SA32	1	1	1	1	1	0	0	1	8/4	1F2000h to 1F3FFFh	0F9000h to 0F9FFFh
	SA33	1	1	1	1	1	0	1	0	8/4	1F4000h to 1F5FFFh	0FA000h to 0FAFFFh
	SA34	1	1	1	1	1	0	1	1	8/4	1F6000h to 1F7FFFh	0FB000h to 0FBFFFh
	SA35	1	1	1	1	1	1	0	0	8/4	1F8000h to 1F9FFFh	0FC000h to 0FCFFFh
	SA36	1	1	1	1	1	1	0	1	8/4	1FA000h to 1FBFFFh	0FD000h to 0FDFFFh
	SA37	1	1	1	1	1	1	1	0	8/4	1FC000h to 1FDFFFh	0FE000h to 0FEFFFh
	SA38	1	1	1	1	1	1	1	1	8/4	1FE000h to 1FFFFFh	0FF000h to 0FFFFFh

Notes : • The address range is A_{19} : A_{-1} if in byte mode ($\overline{BYTE} = V_{IL}$) .
• The address range is A_{19} : A_0 if in word mode ($\overline{BYTE} = V_{IH}$) .

Sector Address Table (MBM29DS163BE)

Bank	Sector	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address										
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
Bank 2	SA38	1	1	1	1	1	X	X	X	64/32	1F0000h to 1FFFFFh	0F8000h to 0FFFFFh
	SA37	1	1	1	1	0	X	X	X	64/32	1E0000h to 1EFFFFh	0F0000h to 0F7FFFh
	SA36	1	1	1	0	1	X	X	X	64/32	1D0000h to 1DFFFFh	0E8000h to 0EFFFFh
	SA35	1	1	1	0	0	X	X	X	64/32	1C0000h to 1CFFFFh	0E0000h to 0E7FFFh
	SA34	1	1	0	1	1	X	X	X	64/32	1B0000h to 1BFFFFh	0D8000h to 0DFFFFh
	SA33	1	1	0	1	0	X	X	X	64/32	1A0000h to 1AFFFFh	0D0000h to 0D7FFFh
	SA32	1	1	0	0	1	X	X	X	64/32	190000h to 19FFFFh	0C8000h to 0CFFFFh
	SA31	1	1	0	0	0	X	X	X	64/32	180000h to 18FFFFh	0C0000h to 0C7FFFh
	SA30	1	0	1	1	1	X	X	X	64/32	170000h to 17FFFFh	0B8000h to 0BFFFFh
	SA29	1	0	1	1	0	X	X	X	64/32	160000h to 16FFFFh	0B0000h to 0B7FFFh
	SA28	1	0	1	0	1	X	X	X	64/32	150000h to 15FFFFh	0A8000h to 0AFFFFh
	SA27	1	0	1	0	0	X	X	X	64/32	140000h to 14FFFFh	0A0000h to 0A7FFFh
	SA26	1	0	0	1	1	X	X	X	64/32	130000h to 13FFFFh	098000h to 09FFFFh
	SA25	1	0	0	1	0	X	X	X	64/32	120000h to 12FFFFh	090000h to 097FFFh
	SA24	1	0	0	0	X	X	X	X	64/32	110000h to 11FFFFh	088000h to 08FFFFh
	SA23	1	0	0	0	0	X	X	X	64/32	100000h to 10FFFFh	080000h to 087FFFh
	SA22	0	1	1	1	1	X	X	X	64/32	0F0000h to 0FFFFFh	078000h to 07FFFFh
	SA21	0	1	1	1	0	X	X	X	64/32	0E0000h to 0EFFFFh	070000h to 077FFFh
	SA20	0	1	1	0	1	X	X	X	64/32	0D0000h to 0DFFFFh	068000h to 06FFFFh
	SA19	0	1	1	0	0	X	X	X	64/32	0C0000h to 0CFFFFh	060000h to 067FFFh
	SA18	0	1	0	1	1	X	X	X	64/32	0B0000h to 0BFFFFh	058000h to 05FFFFh
	SA17	0	1	0	1	0	X	X	X	64/32	0A0000h to 0AFFFFh	050000h to 057FFFh
	SA16	0	1	0	0	1	X	X	X	64/32	090000h to 0FFFFFh	048000h to 04FFFFh
	SA15	0	1	0	0	0	X	X	X	64/32	080000h to 08FFFFh	040000h to 047FFFh

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Bank	Sec-tor	Sector Address								Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		Bank Address										
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
Bank 1	SA14	0	0	1	1	1	X	X	X	64/32	070000h to 07FFFFh	038000h to 03FFFFh
	SA13	0	0	1	1	0	X	X	X	64/32	060000h to 06FFFFh	030000h to 037FFFh
	SA12	0	0	1	0	1	X	X	X	64/32	050000h to 05FFFFh	028000h to 02FFFFh
	SA11	0	0	1	0	0	X	X	X	64/32	040000h to 04FFFFh	020000h to 027FFFh
	SA10	0	0	0	1	1	X	X	X	64/32	030000h to 03FFFFh	018000h to 01FFFFh
	SA9	0	0	0	1	0	X	X	X	64/32	020000h to 02FFFFh	010000h to 017FFFh
	SA8	0	0	0	0	1	X	X	X	64/32	010000h to 01FFFFh	008000h to 008FFFh
	SA7	0	0	0	0	0	1	1	1	8/4	00E000h to 00FFFFh	007000h to 007FFFh
	SA6	0	0	0	0	0	1	1	0	8/4	00C000h to 00DFFFh	006000h to 006FFFh
	SA5	0	0	0	0	0	1	0	1	8/4	00A000h to 00BFFFh	005000h to 005FFFh
	SA4	0	0	0	0	0	1	0	0	8/4	008000h to 009FFFh	004000h to 004FFFh
	SA3	0	0	0	0	0	0	1	1	8/4	006000h to 007FFFh	003000h to 003FFFh
	SA2	0	0	0	0	0	0	1	0	8/4	004000h to 005FFFh	002000h to 002FFFh
	SA1	0	0	0	0	0	0	0	1	8/4	002000h to 003FFFh	001000h to 001FFFh
	SA0	0	0	0	0	0	0	0	0	8/4	000000h to 001FFFh	000000h to 000FFFh

Notes : • The address range is A_{19} : A_{-1} if in byte mode ($\overline{BYTE} = V_{IL}$) .
• The address range is A_{19} : A_0 if in word mode ($\overline{BYTE} = V_{IH}$) .

Sector Group Addresses (MBM29DS163TE) Table (Top Boot Block)

Sector Group	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	1	X	X	X	SA1 to SA3
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA2	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	1	1	1	0	0	X	X	X	SA28 to SA30
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA9	1	1	1	1	1	0	0	0	SA31
SGA10	1	1	1	1	1	0	0	1	SA32
SGA11	1	1	1	1	1	0	1	0	SA33
SGA12	1	1	1	1	1	0	1	1	SA34
SGA13	1	1	1	1	1	1	0	0	SA35
SGA14	1	1	1	1	1	1	0	1	SA36
SGA15	1	1	1	1	1	1	1	0	SA37
SGA16	1	1	1	1	1	1	1	1	SA38

Sector Group Addresses (MBM29DS163BE) Table (Bottom Boot Block)

Sector Group	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	1	X	X	X	SA8 to SA10
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA9	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	1	1	1	0	0	X	X	X	SA35 to SA37
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA16	1	1	1	1	1	X	X	X	SA38

Common Flash Memory Interface Code Table

Description	A_6 to A_0	DQ_{15} to DQ_0
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h
Primary OEM Command Set 2h : AMD/FJ standard type	13h 14h	0002h 0000h
Address for Primary Extended Table	15h 16h	0040h 0000h
Alternate OEM Command Set (00h = not applicable)	17h 18h	0000h 0000h
Address for Alternate OEM Extended Table	19h 1Ah	0000h 0000h
V_{CC} Min (write/erase) DQ_7 to DQ_4 : V, DQ_3 to DQ_0 : 100 mV	1Bh	0018h
V_{CC} Max (write/erase) DQ_7 to DQ_4 : V, DQ_3 to DQ_0 : 100 mV	1Ch	0022h
V_{PP} Min voltage	1Dh	0000h
V_{PP} Max voltage	1Eh	0000h
Typical timeout per single byte/word write 2^N µs	1Fh	0004h
Typical timeout for Min size buffer write 2^N µs	20h	0000h
Typical timeout per individual block erase 2^N ms	21h	000Ah
Typical timeout for full chip erase 2^N ms	22h	0000h
Max timeout for byte/word write 2^N times typical	23h	0005h
Max timeout for buffer write 2^N times typical	24h	0000h
Max timeout per individual block erase 2^N times typical	25h	0004h
Max timeout for full chip erase 2^N times typical	26h	0000h
Device Size = 2^N byte	27h	0015h
Flash Device Interface description	28h 29h	0002h 0000h
Max number of byte in multi-byte write = 2^N	2Ah 2Bh	0000h 0000h
Number of Erase Block Regions within device	2Ch	0002h
Erase Block Region 1 Information	2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h
Erase Block Region 2 Information	31h 32h 33h 34h	001Eh 0000h 0000h 0001h

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Description	A_6 to A_0	DQ_{15} to DQ_0
Query-unique ASCII string “PRI”	40h 41h 42h	0050h 0052h 0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0032h
Address Sensitive Unlock 0h = Required 1h = Not Required	45h	0000h
Erase Suspend 0h = Not Supported 1h = To Read Only 2h = To Read & Write	46h	0002h
Sector Protection 0h = Not Supported X = Number of sectors in per group	47h	0001h
Sector Temporary Unprotection 00h = Not Supported 01h = Supported	48h	0001h
Sector Protection Algorithm	49h	0004h
Number of Sector for Bank 2 00h = Not Supported	4Ah	0018h
Burst Mode Type 00h = Not Supported	4Bh	0000h
Page Mode Type 00h = Not Supported	4Ch	0000h
ACC (Acceleration) Supply Minimum 00h = Not Supported, DQ_7 to DQ_4 : V, DQ_3 to DQ_0 : 100 mV	4Dh	0085h
ACC (Acceleration) Supply Maximum 00h = Not Supported, DQ_7 to DQ_4 : V, DQ_3 to DQ_0 : 100 mV	4Eh	0095h
Boot Type 02h = MBM29DS163BE 03h = MBM29DS163TE	4Fh	00XXh
Program Suspend 00h = Not Supported 01h = Supported	50h	0001h

■ FUNCTIONAL DESCRIPTION

Simultaneous Operation

The device has a feature, that is capable of reading data from one bank of memory while a program or erase operation is in progress in the other bank of memory (simultaneous operation) , in addition to the conventional features (read, program, erase, erase-suspend read, and erase-suspend program) . The bank selection can be selected by bank address (A_{19} to A_{15}) with zero latency.

The device has two banks which contain
Bank 1 (8 KB × eight sectors, 64 KB × seven sectors) and Bank 2 (64 KB × twenty-four sectors) .

The simultaneous operation cannot execute multi-function mode in the same bank. “Simultaneous Operation” Table shows the combinations for simultaneous operation (refer to “Bank-to-Bank Read/Write Timing Diagram” in “■ TIMING DIAGRAM”) .

Simultaneous Operation Table

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode *
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode *	Read mode

* : Erase operation may also be supended to read from or program to a sector not being erased.

Read Mode

The device has two control functions to be satisfied to obtaining data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}-t_{OE} time) . When reading out data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from “H” or “L”.

The $\overline{RESET}$ pin must be held low during V_{CC} rampup to insure that device powers up correctly.
(Refer to “Power On/Off Timing Diagram” in “■ TIMING DIAGRAM”.)

Standby Mode

There are two ways to implement the standby mode on the device, one using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at $V_{CC} \pm 0.3$ V. Under this condition the current consumed is less than 5 μA max. During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even $\overline{CE}$ = “H”. The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at $V_{SS} \pm 0.3$ V ($\overline{CE}$ = “H” or “L”) . Under this condition the current consumed is less than 5 μA max. Once the $\overline{RESET}$ pin is taken high, the device requires t_{RH} as wake up time for outputs to be valid for read access.

In the standby mode the outputs are in the high impedance state, independently of the $\overline{OE}$ input.

Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of the device data. This mode can be useful in the application such as a handy terminal which requires low power consumption.

To activate this mode, the device automatically switches themselves to low power mode when the device addresses remain stable during access time of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on the mode. Under the mode, the current consumed is typically 1 µA (CMOS Level) .

During simultaneous operation, V_{CC} active current (I_{CC2}) is required.

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically, and the device reads the data for changed addresses.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}) , output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (10.0 V to 11.0 V) on address pin A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON'T CARES except A_0, A_1, and A_6 (A_{-1}) . (See “MBM29DS163TE/BE User Bus Operations ($\overline{BYTE}$ = V_{IH})” Table and “MBM29DS163TE/BE User Bus Operations ($\overline{BYTE}$ = V_{IL})” Table in “■ DEVICE BUS OPERATION”.)

The manufacturer and device codes may also be read via the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in “ MBM29DS163TE/BE Command Definitions” Table in “■ DEVICE BUS OPERATION”.

Word 0 ($A_0 = V_{IL}$) represents the manufacturer's code (Fujitsu = 04h) and word 1 ($A_0 = V_{IH}$) represents the device identifier code. These two bytes/words are given in MBM29DS163TE/BE Sector Group Protection Verify Autoselect Codes” Table and “Expanded Autoselect Code “ Table in “■ DEVICE BUS OPERATION”. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL}. (See “MBM29DS163TE/BE Sector Group Protection Verify Autoselect Codes” Table and “Expanded Autoselect Code “ Table in “■ DEVICE BUS OPERATION”.)

In case of applying V_{ID} on A_9, since both Bank 1 and Bank 2 enters Autoselect mode, the simultenous operation can not be executed.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Group Protection

The device features hardware sector group protection. This feature will disable both program and erase operations in any combination of twenty five sector groups of memory. (See “Sector Group Addresses (MBM29DS163TE)” Table and “Sector Group Addresses (MBM29DS163BE)” Table in “■ FLEXIBLE SECTOR-

ERASE ARCHITECTURE”.) The sector group protection feature is enabled using programming equipment at the user’s site. The device is shipped with all sector groups unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest V_{ID} = 11.5 V) , $\overline{CE}$ = V_{IL} and A_6 = A_0 = V_{IL}, A_1 = V_{IH}. The sector group addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. “Sector Address (MBM29DS163TE)” Table and “Sector Address (MBM29DS163BE)” Table in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE” define the sector address for each of the seventy one (71) individual sectors, and t“Sector Group Addresses (MBM29DS163TE)” Table and “Sector Group Addresses (MBM29DS163BE)” Table in “■ FLEXIBLE SECTOR-ERASE ARCHITECTURE” define the sector group address for each of the twenty five (25) individual group sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector group addresses must be held constant during the $\overline{WE}$ pulse. See “Sector Group Protection Timing Diagram” in “■ TIMING DIAGRAM” and ”Sector Group Protection Algorithm” in “■ FLOW CHART” for sector group protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector group addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” code at device output DQ_0 for a protected sector. Otherwise the device will produce “0” for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON’T CARES. Address locations with A_1 = V_{IL} are reserved for Autoselect manufacturer and device codes. A_{-1} requires to apply to V_{IL} on byte mode.

It is also possible to determine if a sector group is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) are the desired sector group address will produce a logical “1” at DQ_0 for a protected sector group. See “MBM29DS163TE/BE Sector Group Protection Verify Autoselect Codes” Table and “Expanded Autoselect Code “ Table in “■ DEVICE BUS OPERATION” for Autoselect codes.

Temporary Sector Group Unprotection

This feature allows temporary unprotection of previously protected sector groups of the device in order to change data. The Sector Group Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (V_{ID}) . During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once the V_{ID} is taken away from the $\overline{RESET}$ pin, all the previously protected sector groups will be protected again. Refer to “Temporary Sector Group Unprotection Timing Diagram” in “■ TIMING DIAGRAM” and ”Temporary Sector Group Unprotection Algorithm” in “■ FLOW CHART”.

Extended Sector Group Protection

In addition to normal sector group protection, the device has Extended Sector Group Protection as extended function. This function enables to protect sector group by forcing V_{ID} on $\overline{RESET}$ pin and write a command sequence. Unlike conventional procedure, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector group protection in this mode. The extended sector group protection requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then, the sector group addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set to the sector group to be protected (recommend to set V_{IL} for the other addresses pins) , and write extended sector group protection command (60h) . A sector group is typically protected in 250 µs. To verify programming of the protection circuitry, the sector group addresses pins (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40h) . Following the command write, a logical “1” at device output DQ_0 will produce for protected sector in the read operation. If the output is logical “0”, please repeat to write extended sector group protection command (60h) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to V_{IH}. (Refer to “Extended Sector Group Protection Timing Diagram” in “■ TIMING DIAGRAM” and ”Extended Sector Group Protection Algorithm” in “■ FLOW CHART”.)

$\overline{\text{RESET}}$

Hardware Reset

The device may be reset by driving the $\overline{\text{RESET}}$ pin to V_{IL}. The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least "t_{RP}" in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode "t_{READY}" after the $\overline{\text{RESET}}$ pin is driven low. Furthermore, once the $\overline{\text{RESET}}$ pin goes high, the device requires an additional "t_{RH}" before it will allow read access. When the $\overline{\text{RESET}}$ pin is low, the device will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{\text{BY}}$ output signal should be ignored during the $\overline{\text{RESET}}$ pulse. See "$\overline{\text{RESET}}$, RY/$\overline{\text{BY}}$ Timing Diagram" in "■ TIMING DIAGRAM" for the timing diagram. Refer to Temporary Sector Group Unprotection for additional functionality.

Boot Block Sector Protection

The Write Protection function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the $\overline{\text{WP}}$/ACC pin.

If the system asserts V_{IL} on the $\overline{\text{WP}}$/ACC pin, the device disables program and erase functions in the two "outermost" 8 K byte boot sectors independently of whether those sectors are protected or unprotected using the method described in "Sector Protection/Unprotection". The two outermost 8 K byte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-congfigured device.
(MBM29DS163TE : SA37 and SA38, MBM29DS163BE : SA0 and SA1)

If the system asserts V_{IH} on the $\overline{\text{WP}}$/ACC pin, the device reverts to whether the two outermost 8 K byte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in "Sector protection/unprotection".

Accelerated Program Operation

The device offers accelerated program operation which enables the programming in high speed. If the system asserts V_{ACC} to the $\overline{\text{WP}}$/ACC pin, the device automatically enters the acceleration mode and the time required for program operation will reduce to about 60%. This function is primarily intended to allow high speed program, so caution is needed as the sector group will temporarily be unprotected.

The system would use a fast program command sequence when programming during acceleration mode. Set command to fast mode and reset command from fast mode are not necessary. When the device enters the acceleration mode, the device automatically set to fast mode. Therefore, the pressent sequence could be used for programming and detection of completion during acceleration mode.

Removing V_{ACC} from the $\overline{\text{WP}}$/ACC pin returns the device to normal operation. Do not remove V_{ACC} from $\overline{\text{WP}}$/ACC pin while programming. See "Accelerated Program Timing Diagram" in "■ TIMING DIAGRAM".

■ COMMAND DEFINITIONS

The device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Some commands require Bank Address (BA) input. When command sequences are inputed to bank being read, the commands have priority over reading. “MBM29DS163TE/BE Command Definitions” Table in “■ DEVICE BUS OPERATION” defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Also the Program Suspend (B0h) and Program Resume (30h) commands are valid only while the Program operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_7 to DQ_0 and DQ_{15} to DQ_8 bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to Read/Reset mode, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remain enabled for reads until the command register contents are altered.

The device will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated by firstly writing two unlock cycles. This is followed by a third write cycle that contains the bank address (BA) and the Autoselect command. Then the manufacture and device codes can be read from the bank, and actual data of memory cell can be read from the another bank.

Following the command write, a read cycle from address (BA) 00h retrieves the manufacture code of 04h. A read cycle from address (BA) 01h for ×16 ((BA) 02h for ×8) returns the device code. (See “MBM29DS163TE/BE Sector Group Protection Verify Autoselect Codes” Table and “Expanded Autoselect Code “ Table in “■ DEVICE BUS OPERATION”.)

The sector state (protection or unprotection) will be informed by address (BA) 02h for ×16 ((BA) 04h for ×8) . Scanning the sector group addresses (A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical “1” at device output DQ_0 for a protected sector group. The programming verification should be performed by verify sector group protection on the protected sector. (See “MBM29DS163TE/BE User Bus Operations ($\overline{BYTE}$ = V_{IH})” Table and “MBM29DS163TE/BE User Bus Operations ($\overline{BYTE}$ = V_{IL})” Table in “■ DEVICE BUS OPERATION”.)

The manufacture and device codes can be allowed reading from selected bank. To read the manufacture and device codes and sector protection status from non-selected bank, it is necessary to write Read/Reset command sequence into the register and then Autoselect command should be written into the bank to be read.

If the software (program code) for Autoselect command is stored into the Flash memory, the device and manufacture codes should be read from the other bank which doesn’t contain the software.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register. To execute the Autoselect command during the operation, writing Read/Reset command sequence must precede the Autoselect command.

Byte/Word Programming

The device is programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device automatically provides adequate internally generated program pulses and verify programmed cell margin.

The system can determine the status of the program operation by using DQ_7 ($\overline{\text{Data}}$ Polling) , DQ_6 (Toggle Bit) , or RY/$\overline{\text{BY}}$. The $\overline{\text{Data}}$ Polling and Toggle Bit must be performed at the memory location being programmed.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which the device return to the read mode and addresses are no longer latched. (See "Hardware Sequence Flags" , Hardware Sequence Flags.) Therefore the device requires that a valid address to the device be supplied by the system at this particular moment. Hence $\overline{\text{Data}}$ Polling must be performed at the memory location being programmed.

Any commands written to the chip during this period are ignored. If hardware reset occurs during the programming operation, it is impossible to guarantee the data being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

"Embedded Program™ Algorithm" in "■ FLOW CHART" illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Program Suspend/Resume

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any address. Writing the Program Suspend command (B0h) during the Embedded Program operation immediately suspends the programming. The Program Suspend command may also be issued during a programming operation while an erase is suspended. The bank addresses of sector being programed should be set when writing the Program Suspend command.

When the Program Suspend command is written during a programming process, the device halts the program operation within 1 µs and updates the status bits.

After the program operation has been suspended, the system can read data from any address. The data at program-suspended address is not valid. Normal read timing and command definitions apply.

After the Program Resume command (30h) is written, the device reverts to programming. The bank addresses of sector being suspended should be set when writing the Program Resume command. The system can determine the status of the program operation using the DQ_7 or DQ_6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device in the Program Suspend mode. The device allows reading autoselect codes at the addresses within programming sectors, since the codes are not stored in the memory. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Program Resume command (address bits are "Bank Address") to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function) . The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling) , DQ_6 (Toggle Bit) , or RY/$\overline{BY}$. The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which the device returns to read the mode.

Chip Erase Time : Sector Erase Time × All sectors + Chip Program Time (Preprogramming)

“Embedded Erase™ Algorithm” in “■ FLOW CHART” illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever happens later, while the command (Data = 30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ which happens first. After time-out of “t_{TOW}” from the rising edge of the last sector erase command, the sector erase operation begins.

Multiple sectors are erased concurrently by writing the six bus cycle operations on “MBM29DS163TE/BE Command Definitions” in “■ USER BUS OPERATION”. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than “t_{TOW}” otherwise that command will not be accepted and erasure does not start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of “t_{TOW}” from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command (s) . If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first occurs within the “t_{TOW}” time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 70) .

Sector erase does not require the user to program the device prior to erase. The device automatically programs all memory locations in the sector (s) to be erased prior to electrical erase (Preprogram function) . When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling) , DQ_6 (Toggle Bit) , or RY/$\overline{BY}$.

The sector erase begins after the “t_{TOW}” time out from the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever happens first for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the device return to the read mode. $\overline{Data}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time : [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase

In case of multiple sector erase across bank boundaries, a read from bank (read-while-erase) can not performe.

“Embedded Erase™ Algorithm” in “■ FLOW CHART” illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command is ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writting the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The bank addresses of sector being erased or erase-suspended should be set when writting the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device takes a maximum of "t_{SPD}" to suspend the erase operation. When the device has entered the erase-suspended mode, the RY/$\overline{BY}$ output pin is at HIGH-Z and the DQ_7 bit is at logic "1", and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation is suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the device defaults to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the RY/$\overline{BY}$ output pin, $\overline{Data}$ polling of DQ_7 or by the Toggle Bit I (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address within bank being erase-suspended.

To resume the operation of Sector Erase, the Resume command (30h) should be written to the bank being erase suspended. Any further writes of the Resume command at this point is ignored. Another Erase Suspend command is written after the chip resumes erasing.

Extended Command

(1) Fast Mode

The device has Fast Mode function. This mode dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. The first cycle must contain the bank address. (Refer to "Embedded ProgramTM Algorithm for Fast Mode" in "■ FLOW CHART".) The V_{CC} active current is required even $\overline{CE}$ = V_{IH} during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD) . (Refer to "Embedded ProgramTM Algorithm for Fast Mode" in "■ FLOW CHART".)

(3) CFI (Common Flash Memory Interface)

The CFI (Common Flash Memory Interface) specification outlines device and host system software interrogation handshake which allows specific vendor-specified software algorithms to be used for entire families of device. This allows device-independent, JEDEC ID-independent, and forward-and backward-compatible software support for the specified flash device families. Refer to CFI specification in detail.

The operation is initiated by writing the query command (98h) into the command register. The bank address should be set when writing this command. Then the device information can be read from the bank, and an actual data of memory cell be read from the another bank. Following the command write, a read cycle from specific address retrives device information. Please note that output data of upper byte (DQ_{15} to DQ_8) is "0" in word mode (16 bit) read. Refer to the CFI code table. To terminate operation, it is necessary to write the read/reset command sequence into the register. (See "Command Flash Memory Interface Code" in "■ FLEXIBLE SECTOR-ERASE ARCHITECTURE".)

HiddenROM Region

The HiddenROM feature provides Flash memory region that the system may access through a new command sequence. This is primarily intended for customers who wish to use an Electronic Serial Number (ESN) in the device with the ESN protected against modification. Once the HiddenROM region is protected, any further modification of that region is not allowed. This ensures the security of the ESN once the product is shipped to the field.

The HiddenROM region is 64 K bytes in length and is stored at the same address of the 8 KB ×8 sectors. The MBM29DS163TE occupies the address of the byte mode 1F0000h to 1FFFFFh (word mode 0F8000h to 0FFFFFh) and the MBM29DS163BE type occupies the address of the byte mode 000000h to 00FFFFh (word mode 000000h to 007FFFh) . After the system writes the Enter HiddenROM command sequence, the system reads the HiddenROM region by using the addresses normally occupied by the boot sectors. That is, the device sends all commands that would normally be sent to the boot sectors to the HiddenROM region. This mode of operation continues until the system issues the Exit HiddenROM command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors.

HiddenROM Entry Command

The device has HiddenROM area with One Time Protect function. This area is to enter the security code and to unable the change of the code once set. Program/erase is possible in this area until it becomes protected. However once it is protected, it is impossible to unprotect, use this command with caution.

HiddenROM area is 64 K Byte and in the same address area of 8 KB sector. The address of top boot is 1F0000h to 1FFFFFh at byte mode (0F8000h to 0FFFFFh at word mode) and the bottom boot is 000000h to 00FFFFh at byte mode (000000h to 007FFFh at word mode) . These areas are normally the boot block area (8KB ×8 sector) . Therefore, write the HiddenROM entry command sequence to enter the HiddenROM area. This is called HiddenROM mode as the HiddenROM area appears.

Sector other than the boot block area could be read during HiddenROM mode. Read/program/earse of the HiddenROM area is allowed during HiddenROM mode. Write the HiddenROM reset command sequence to exit the HiddenROM mode. The bank address of the HiddenROM should be set on the third cycle of this reset command sequence.

HiddenROM Program Command

To program data to HiddenROM area, write the HiddenROM program command sequence during HiddenROM mode. This command is the same as the program command in usual except to write the command during HiddenROM mode. Therefore the detection of completion method is the same as described, using the DQ_7 data poling, DQ_6 toggle bit and RY/$\overline{BY}$ pin. Need to pay attention to the address to be programmed. If the address other than the HiddenROM area is selected to program, data of the address will be changed.

HiddenROM Erase Command

To erase the HiddenROM area, write the HiddenROM erase command sequence during HiddenROM mode. This command is same as the sector erase command in the past except to write the command during HiddenROM mode. Therefore the detection of completion method is the same as in the past, using the DQ_7 data poling, DQ_6 toggle bit and RY/$\overline{BY}$ pin. Need to pay attention to the sector address to be erased. If the sector address other than the HiddenROM area is selected, the data of the sector will be changed.

HiddenROM Protect Command

There are two methods to protect the HiddenROM area. One is to write the sector group protect setup command (60h) , set the sector address in the HiddenROM area and (A_6, A_1, A_0) = (0, 1, 0) , and write the sector group protect command (60h) during the HiddenROM mode. The same command sequence could be used because, it is just as the extension sector group protect in the past except that it is in the HiddenROM mode and it does not apply high voltage to $\overline{RESET}$ pin. Please refer to "Function Explanation Extentended Sector Group Protection" for details of extention sector group protect setting.

The other method is to apply high voltage (V_{ID}) to A_9 and $\overline{OE}$, set the sector address in the HiddenROM area and (A_6, A_1, A_0) = (0, 1, 0) , and apply the write pulse during the HiddenROM mode. To verify the protect circuit, apply high voltage (V_{ID}) to A_9, specify (A_6, A_1, A_0) = (0, 1, 0) and the sector address in the HiddenROM area, and read. When "1" appears on DQ_0, the protect setting is completed. "0" will appear on DQ_0 if it is not protected. Please apply write pulse again. The same command sequence could be used for the above method because other than the HiddenROM mode, it is the same with the sector group protect in the past. Please refer to "Function Explanation Sector Group Protection" for details of the sector group protect setting.
Other sector group will be effected if the address other than those for HiddenROM area is selected for the sector group address. Once it is protected, protection cannot be cancelled; so pay the closest attention.

Write Operation Status

Detailed in "Hardware Sequence Flags" Table are all the status flags that determine the status of the bank for the current mode operation. The read operation from the bank which does not operate Embedded Algorithm returns data of memory cells. These bits offer a method for determining whether a Embedded Algorithm is properly completed. The information on DQ_2 is address sensitive. This means that if an address from an erasing sector is consectively read, then the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consectively read. This allows users to determine which sectors are in erase and which are not. The status flag is not output from bank (non-busy bank) which does not execute Embedded Algorithm. For example, there is bank (busy bank) now executing Embedded Algorithm. When the read sequence is [1] < busy bank > , [2] < non-busy bank > , [3] < busy bank > , the DQ_6 is toggling in the case of [1] and [3]. In case of [2], the data of memory cells are outputted. In the erase-suspend read mode with the same read sequence, DQ_6 will not be toggled in the [1] and [3].
In the erase suspend read mode, DQ_2 is toggled in the [1] and [3]. In case of [2], the data of memory cell is outputted.

Hardware Sequence Flags Table

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle*
	Program Suspended Mode	Program Suspend Read (Program Suspended Sector)	Data	Data	Data	Data	Data
		Program Suspend Read (Non-Program Suspended Sector)	Data	Data	Data	Data	Data
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1*
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

* : Successive reads from the erasing or erase-suspend sector cause DQ_2 to toggle. Reading from non-erase suspend sector address indicates logic “1” at the DQ_2 bit.

Notes : • DQ_0 and DQ_1 are reserve pins for future use.
• DQ_4 is Fujitsu internal use only.

DQ_7

$\overline{\text{Data}}$ Polling

The device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read device will produce a complement of data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read device will produce true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read device will produce a “0” at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read device will produce a “1” on DQ_7. The flowchart for $\overline{\text{Data}}$ Polling (DQ_7) is shown in “$\overline{\text{Data}}$ Polling Algorithm” in “■ FLOW CHART”.

For programming, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. $\overline{\text{Data}}$ Polling must be performed at sector address of sectors being erased, not protected sectors. Otherwise, the status may be invalid.

If a program address falls within a protected sector, $\overline{\text{Data}}$ Polling on DQ_7 is active for approximately 1 µs, then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, $\overline{\text{Data}}$ Polling on DQ_7 is active for approximately 400 µs, then the bank returns to read mode.

Once the Embedded Algorithm operation is close to completion, the device data pins (DQ_7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that device is driving status information on DQ_7 at one instant of time and then that byte’s valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if device has completed the Embedded Algorithm operation and DQ_7 has a valid data, data outputs on DQ_0 to DQ_6 may be still invalid. The valid data on DQ_0 to DQ_7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is active only during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See “Hardware Sequence Flags” Table.)

See “$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram” in “■ TIMING DIAGRAM” for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ_6

Toggle Bit I

The device also features the “Toggle Bit I” as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.
During Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the device will results in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.
In programming, if the sector being written is protected, the toggle bit will toggle for about 1 µs and then stop toggling with data unchanged. In erase, device will erase all selected sectors except for ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 400 µs and then drop back into read mode, having data unchanged.
Either $\overline{CE}$ or $\overline{OE}$ toggling will cause DQ_6 to toggle.
The system can use DQ_6 to determine whether a sector is actively erased or is erase-suspended. When a bank is actively erased (that is, the Embedded Erase Algorithm is in progress) , DQ_6 toggles. When a bank enters the Erase Suspend mode, DQ_6 stops toggling. Successive read cycles during erase-suspend-program cause DQ_6 to toggle.To operate toggle bit function properly, $\overline{CE}$ or $\overline{OE}$ must be high when bank address is changed.

See "Toggle Bit during Embedded Algorithm Operation Timing Diagram" in "■ TIMING DIAGRAM" for the Toggle Bit I timing specifications and diagrams.

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count) . Under these conditions DQ_5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of device under this condition. The $\overline{\text{CE}}$ circuit will partially power down device under these conditions (to approximately 2 mA) . The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in MBM29DS163TE/BE User Bus Operations ($\overline{\text{BYTE}}$ = V_{IH})" Table and "MBM29DS163TE/BE User Bus Operations ($\overline{\text{BYTE}}$ = V_{IL})" Table at "■ DEVICE BUS OPERATION"

The DQ_5 failure condition may also appear if a user tries to program a non blank location without pre-erase. In this case the device locks out and never complete the Embedded Algorithm operation. Hence, the system never read valid data on DQ_7 bit and DQ_6 never stop toggling. Once device has exceeded timing limits, the DQ_5 bit will indicate a "1." Please note that this is not a device failure condition since device was incorrectly used. If this occurs, reset device with command sequence.

DQ_3

Sector Erase Timer

After completion of the initial sector erase command sequence sector erase time-out will begin. DQ_3 will remain low until the time-out is completed. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit I indicates device has been written with a valid erase command, DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit I. If DQ_3 is low ("0") , the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See "Hardware Sequence Flags" Table : Hardware Sequence Flags.

DQ_2

Toggle Bit II

This toggle bit II, along with DQ_6, can be used to determine whether the device is in the Embedded Erase Algorithm or in Erase Suspend.
Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the device is in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the device is in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic "1" at the DQ_2 bit.
DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows :
For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also "Toggle Bit Status" and "DQ2 vs. DQ6" in "■ TIMING DIAGRAM".
Furthermore, DQ_2 can also be used to determine which sector is being erased. When device is in the erase mode, DQ_2 toggles if this bit is read from an erasing sector.
To operate toggle bit function properly, $\overline{\text{CE}}$ or $\overline{\text{OE}}$ must be high when bank address is changed.

Reading Toggle Bits DQ_6/DQ_2

Whenever the system initially begins reading toggle bit status, it must read DQ_7 to DQ_0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ_7 to DQ_0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ_5 is high (see the section on DQ_5) . If it is the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ_5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ_5 has not gone high. The system may continue to monitor the toggle bit and DQ_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. (Refer to “Toggle Bit Algorithm” in “■ FLOW CHART”.)

Table 11 Toggle Bit Status

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle*
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle	1*

* : Successive reads from the erasing or erase-suspend sector will cause DQ_2 to toggle. Reading from non-erase suspend sector address will indicate logic “1” at the DQ_2 bit.

RY/$\overline{BY}$

Ready/Busy

The device provides a RY/$\overline{BY}$ open-drain output pin as a way to indicate to the host system that Embedded Algorithms are either in progress or has been completed. If output is low, device is busy with either a program or erase operation. If output is high, device is ready to accept any read/write or erase operation. When RY/$\overline{BY}$ pin is low, device will not accept any additional program or erase commands. If the device is placed in an Erase Suspend mode, RY/$\overline{BY}$ output will be high.

During programming, RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth write pulse. During an erase operation, RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth write pulse. RY/$\overline{BY}$ pin will indicate a busy condition during $\overline{RESET}$ pulse. Refer to “RY/$\overline{BY}$ Timing Diagram during Program/Erase Operations” and “$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram” in “■ TIMING DIAGRAM” for a detailed timing diagram. RY/$\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, RY/$\overline{BY}$ pins can be tied together in parallel with a pull-up resistor to V_{CC}.

Byte/Word Configuration

$\overline{BYTE}$ pin selects byte (8-bit) mode or word (16-bit) mode for the device. When this pin is driven high, device operates in word (16-bit) mode. Data is read and programmed at DQ_{15} to DQ_0. When this pin is driven low, device operates in byte (8-bit) mode. Under this mode, the DQ_{15}/A_{-1} pin becomes the lowest address bit, and DQ_{14} to DQ_8 bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_{15} to DQ_8 and DQ_7 to DQ_0 bits are ignored. Refer to “Word Mode Configuration Timing”, “Byte Mode Configuration Timing Diagram” and “BYTE Timing Diagram for Write Operations” in “■ TIMING DIAGRAM” for the timing diagram.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up device automatically resets internal state

machine in Read mode. Also, with its control register architecture, alteration of memory contents only occurs after successful completion of specific multi-bus cycle command sequences.
The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH}, or $\overline{WE}$ = V_{IH}. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with Respect to Ground All pins except A_9, $\overline{OE}$, and $\overline{RESET}$ *1	V_{IN}, V_{OUT}	–0.5	V_{CC} + 0.5	V
Power Supply Voltage *1	V_{CC}	–0.5	+3.0	V
A_9, $\overline{OE}$, and $\overline{RESET}$ *2	V_{IN}	–0.5	+11.5	V
$\overline{WP}$/ACC *3	V_{ACC}	–0.5	+10.5	V

*1 : Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

*2 : Minimum DC input voltage on A_9, $\overline{OE}$ and $\overline{RESET}$ pins is –0.5 V. During voltage transitions, A_9, $\overline{OE}$ and $\overline{RESET}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}-V_{CC}) does not exceed +9.0 V.Maximum DC input voltage on A_9, $\overline{OE}$ and $\overline{RESET}$ pins is +11.5 V which may positive overshoot to +12.5 V for periods of up to 20 ns.

*3 : Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may positive overshoot to +12.0 V for periods of up to 20 ns when Vcc is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ranges		Unit
		Min	Max	
Ambient Temperature	T_A	–40	+85	°C
Power Supply Voltage	V_{CC}	+1.8	+2.2	V

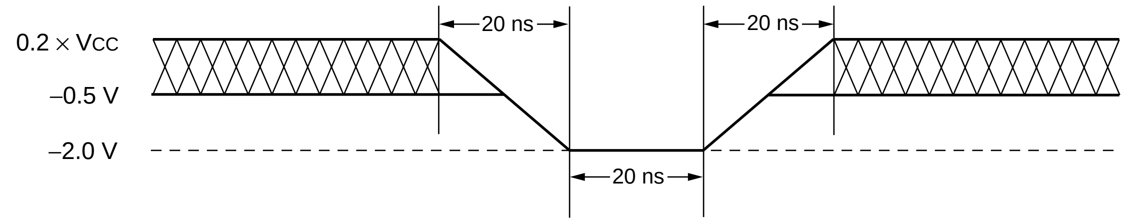
Note : Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

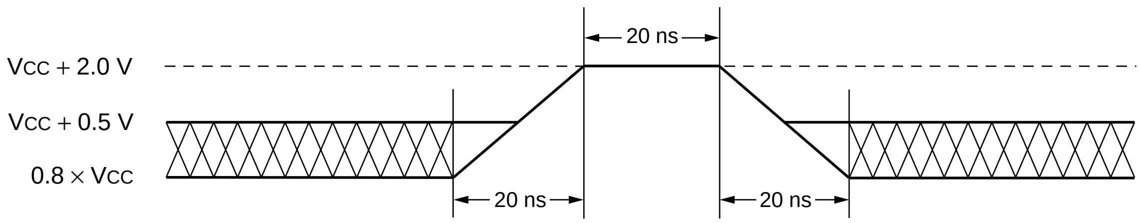
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

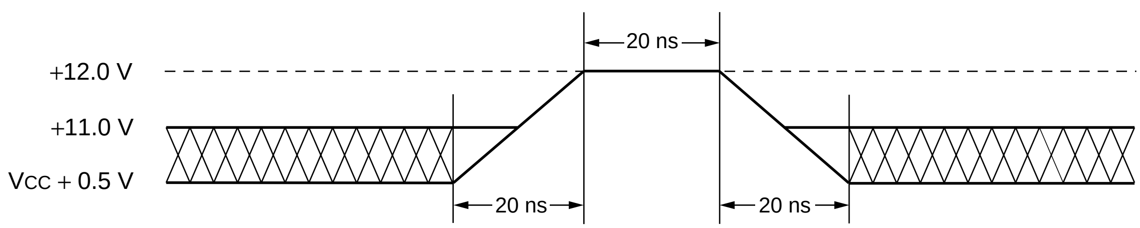
■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT



Maximum Undershoot Waveform



Maximum Overshoot Waveform 1



Note : This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Maximum Overshoot Waveform 2

■ DC CHARACTERISTICS

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		–1.0	+1.0	µA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		–1.0	+1.0	µA
A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	$V_{CC} = V_{CC}$ Max A_9, $\overline{OE}$, $\overline{RESET}$ = 11.0 V		—	35	µA
V_{CC} Active Current *1	I_{CC1}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz	Byte	—	16	mA
			Word		16	
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 1 MHz	Byte	—	4	mA
			Word		4	
V_{CC} Active Current *2	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	25	mA
V_{CC} Current (Standby)	I_{CC3}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V		—	5	µA
V_{CC} Current (Standby, Reset)	I_{CC4}	$V_{CC} = V_{CC}$ Max, $\overline{WE}$/ACC $= V_{CC} \pm$ 0.3 V, $\overline{RESET} = V_{SS} \pm 0.3$ V		—	5	µA
V_{CC} Current (Automatic Sleep Mode) *3	I_{CC5}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{SS} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V		—	5	µA
V_{CC} Active Current *5 (Read-While-Program)	I_{CC6}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte	—	25	mA
			Word	—	25	
V_{CC} Active Current *5 (Read-While-Erase)	I_{CC7}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte	—	25	mA
			Word	—	25	
V_{CC} Active Current (Erase-Suspend-Program)	I_{CC8}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	15	mA
$\overline{WP}$/ACC Accelerated Program Current	I_{ACC}	$V_{CC} = V_{CC}$ Max $\overline{WP}$/ACC $= V_{ACC}$ Max		—	10	mA
Input Low Level	V_{IL}	—		–0.5	$0.2 \times V_{CC}$	V
Input High Level	V_{IH}	—		$0.8 \times V_{CC}$	$V_{CC} + 0.3$	V
Voltage for $\overline{WP}$/ACC Sector Protection/Unprotection and Program Acceleration *4	V_{ACC}	—		8.5	9.5	V
Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$) *4	V_{ID}	—		10.0	11.0	V
Output Low Voltage Level	V_{OL}	$I_{OL} = 100$ µA, $V_{CC} = V_{CC}$ Min		—	0.1	V
Output High Voltage Level	V_{OH}	$I_{OH} = –100$ µA		$V_{CC} – 0.1$	—	V

*1 : I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2 : II_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3 : Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

*4 : Applicable for only V_{CC} applying.

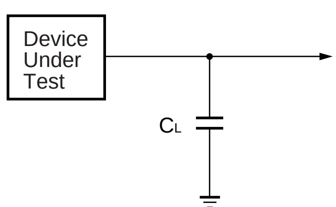
*5 : Embedded Algorithm (program or erase) is in progress. (@5 MHz)

■ AC CHARACTERISTICS

• Read Only Operations Characteristics

Parameter	Symbol		Condition	Value *		Unit
	JEDEC	Standard		Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	100	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	100	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	100	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	35	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	30	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	30	ns
Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	µs
$\overline{CE}$ or $\overline{BYTE}$ Switching Low or High	—	t_{ELFL} t_{ELFH}	—	—	5	ns

* : Test Conditions :
Output Load : $C_L = 30$ pF
Input rise and fall times : 5 ns
Input pulse levels : 0.0 V or 2.0 V
Timing measurement reference level
Input : $0.5 \times V_{CC}f$
Output : $0.5 \times V_{CC}f$



Note : $C_L = 30$ pF including jig capacitance

• **Write/Erase/Program Operations**

Parameter		Symbol JEDEC	Symbol Standard	Value *1 Min	Value *1 Typ	Value *1 Max	Unit
Write Cycle Time		t_{AVAV}	t_{WC}	100	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling		—	t_{ASO}	15	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	50	—	—	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling		—	t_{AHT}	0	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	50	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	—	ns
	Toggle and $\overline{Data}$ Polling			10	—	—	ns
$\overline{CE}$ High During Toggle Bit Polling		—	t_{CEPH}	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling		—	t_{OEPH}	20	—	—	ns
Read Recover Time Before Write		t_{GHWL}	t_{GHWL}	0	—	—	ns
Read Recover Time Before Write		t_{GHEL}	t_{GHEL}	0	—	—	ns
$\overline{CE}$ Setup Time		t_{ELWL}	t_{CS}	0	—	—	ns
$\overline{WE}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	ns
$\overline{CE}$ Hold Time		t_{WHEH}	t_{CH}	0	—	—	ns
$\overline{WE}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	50	—	—	ns
$\overline{CE}$ Pulse Width		t_{ELEH}	t_{CP}	50	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	35	—	—	ns
$\overline{CE}$ Pulse Width High		t_{EHEL}	t_{CPH}	35	—	—	ns
Programming Operation	Byte	t_{WHWH1}	t_{WHWH1}	—	8	—	µs
	Word			—	16	—	µs
Sector Erase Operation*1		t_{WHWH2}	t_{WHWH2}	—	1	—	s
V_{CC} Setup Time		—	t_{VCS}	50	—	—	µs
Rise Time to V_{ID}*2		—	t_{VIDR}	500	—	—	ns
Rise Time to V_{ACC}*3		—	t_{VACCR}	500	—	—	ns
Voltage Transition Time*2		—	t_{VLHT}	4	—	—	µs
Write Pulse Width*2		—	t_{WPP}	100	—	—	µs
$\overline{OE}$ Setup Time to $\overline{WE}$ Active*2		—	t_{OESP}	4	—	—	µs
$\overline{CE}$ Setup Time to $\overline{WE}$ Active*2		—	t_{CSP}	4	—	—	µs
Recover Time From RY/$\overline{BY}$		—	t_{RB}	0	—	—	ns
$\overline{RESET}$ Pulse Width		—	t_{RP}	500	—	—	ns

(Continued)

(Continued)

Parameter	Symbol		Value *1			Unit
	JEDEC	Standard	Min	Typ	Max	
$\overline{\text{RESET}}$ High Level Period Before Read	—	t_{RH}	200	—	—	ns
$\overline{\text{BYTE}}$ Switching Low to Output High-Z	—	t_{FLQZ}	—	—	30	ns
$\overline{\text{BYTE}}$ Switching High to Output Active	—	t_{FHQV}	—	—	90	ns
Program/Erase Valid to RY/$\overline{\text{BY}}$ Delay	—	t_{BUSY}	—	—	90	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	90	ns
Erase Time-out Time	—	t_{TOW}	50	—	—	µs
Erase Suspend Transition Time	—	t_{SPD}	—	—	20	µs
Power On / Off Time	—	t_{PS}	—	—	100	ns

*1 : Does not include the preprogramming time.

*2 : For Sector Group Protection operation.

*3 : For Accelerated Program operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limit			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	1	10	s	Excludes programming time prior to erasure
Word Programming Time	—	16	360	µs	Excludes system-level overhead
Byte Programming Time	—	8	300	µs	
Chip Programming Time	—	—	50	s	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycle	—

■ TSOP (1) PIN CAPACITANCE

Parameter	Symbol	Test Setup	Typ	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$	6.0	7.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8.5	12.0	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	8.0	11.0	pF
$\overline{WP}$/ACC Pin Capacitance	C_{IN3}	$V_{IN} = 0$	21.5	22.5	pF

Notes : • Test conditions $T_A = +25$ °C, f = 1.0 MHz
• DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

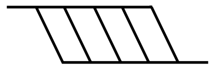
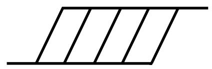
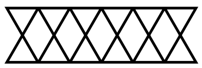
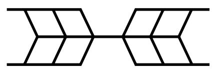
■ FBGA PIN CAPACITANCE

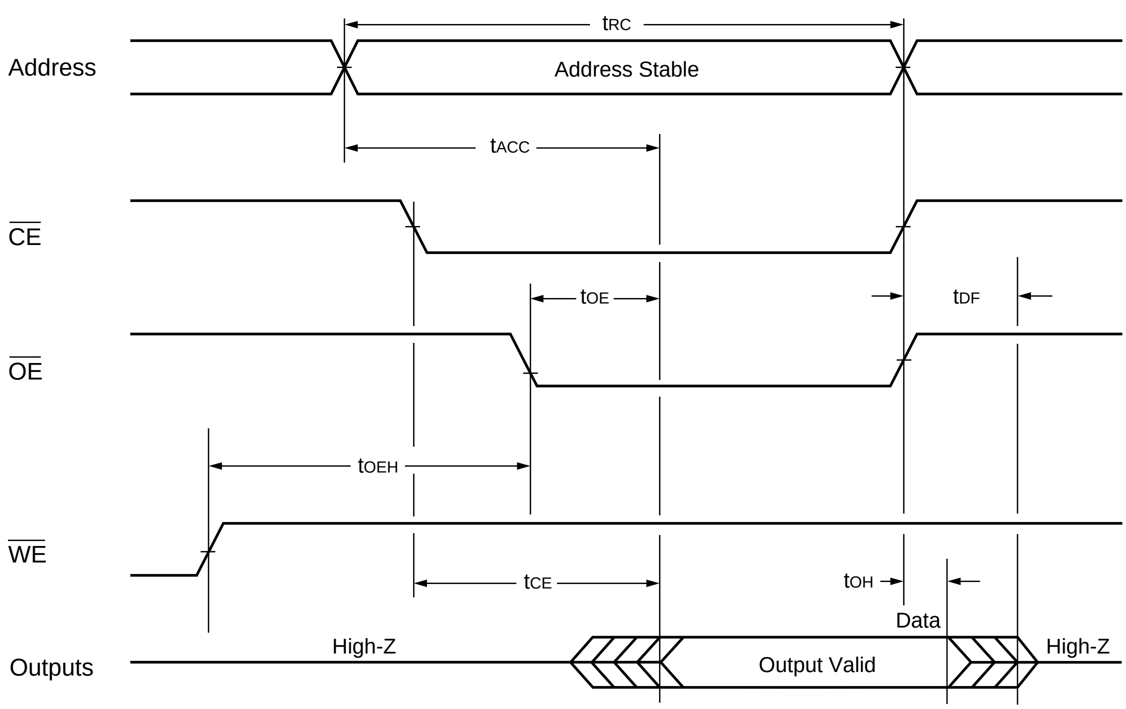
Parameter	Symbol	Test Setup	Typ	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$	6.0	7.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8.5	12.0	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	8.0	10.0	pF
$\overline{WP}$/ACC Pin Capacitance	C_{IN3}	$V_{IN} = 0$	17.0	18.0	pF

Notes : • Test conditions $T_A = +25$ °C, f = 1.0 MHz
• DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

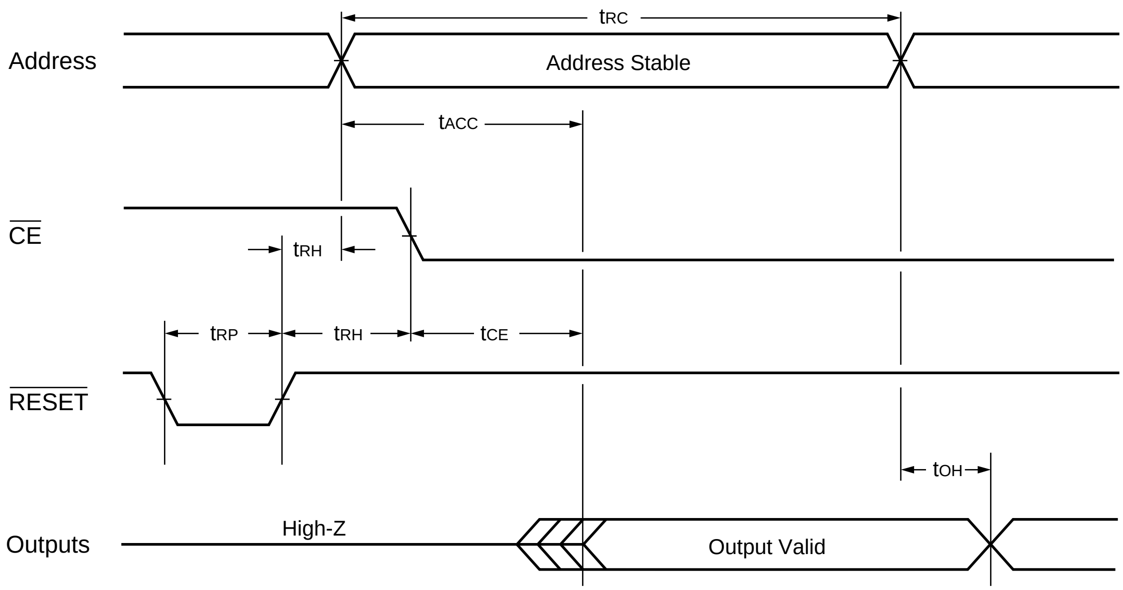
■ TIMING DIAGRAM

• **Key to Switching Waveforms**

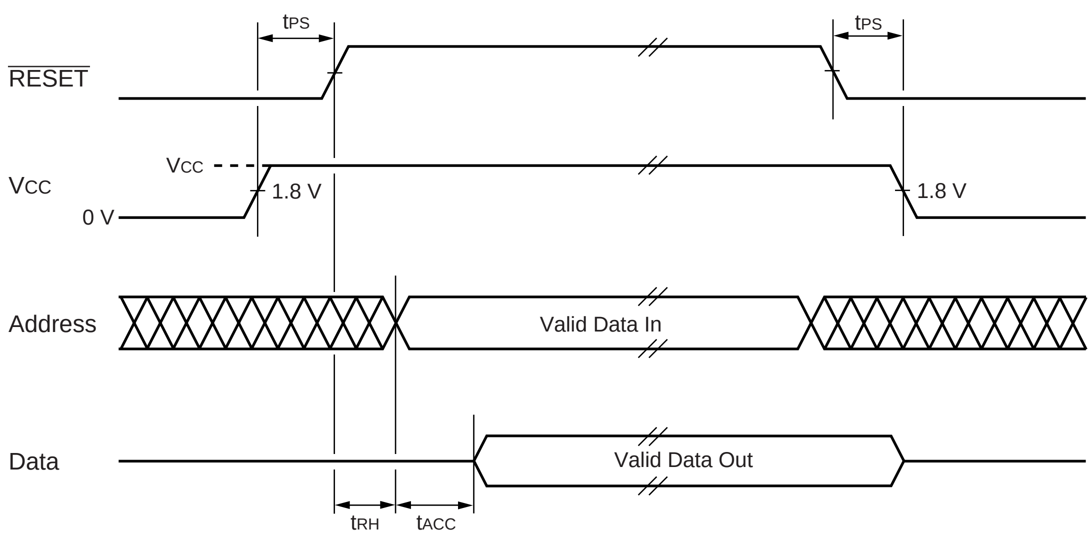
WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Change from H to L
	May Change from L to H	Will Change from L to H
	"H" or "L" Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State



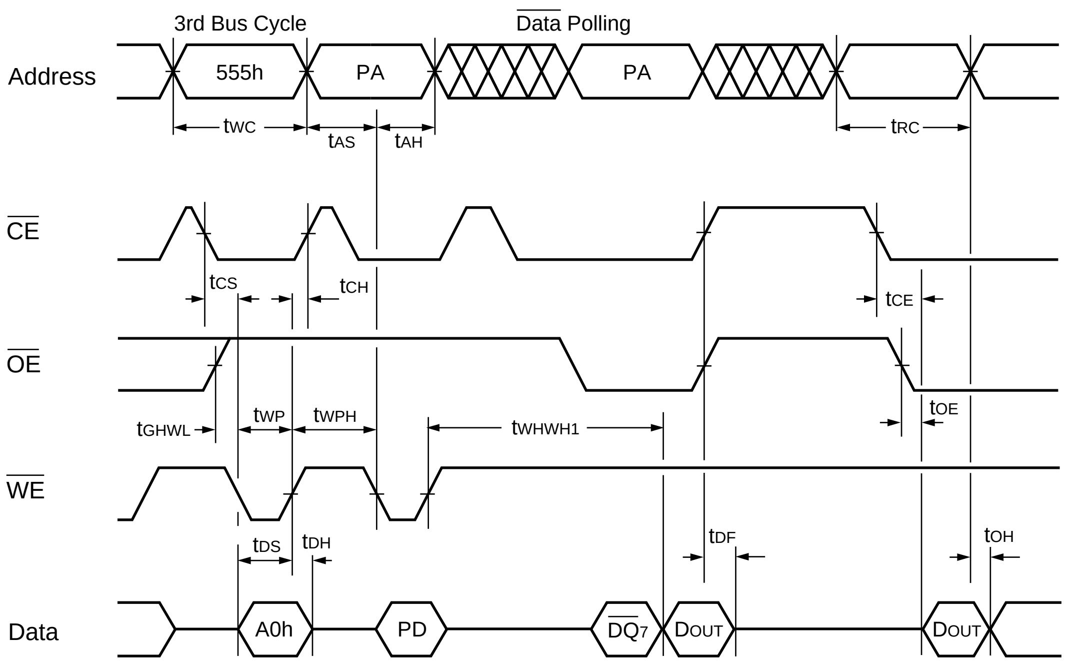
Read Operation Timing Diagram



Hardware Reset/Read Operation Timing Diagram

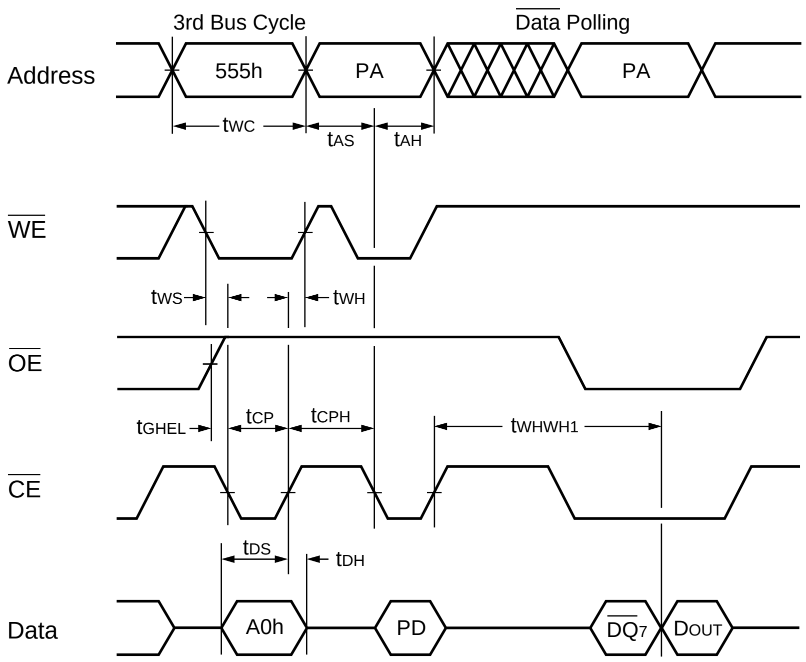


Power On/Off Timing Diagram



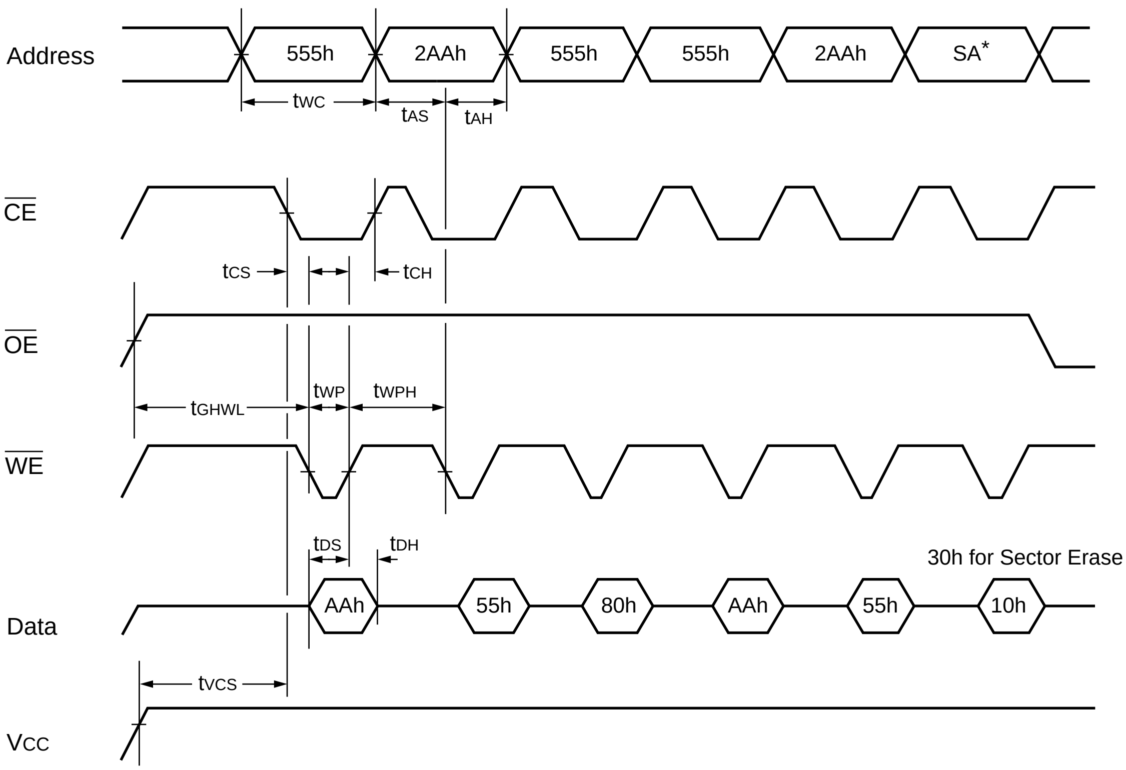
Notes :
- PA is address of the memory location to be programmed.
- PD is data to be programmed at byte address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates the last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode (the addresses differ from ×8 mode) .

Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram



Notes : • PA is address of the memory location to be programmed.
- PD is data to be programmed at byte address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates the last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode (the addresses differ from ×8 mode) .

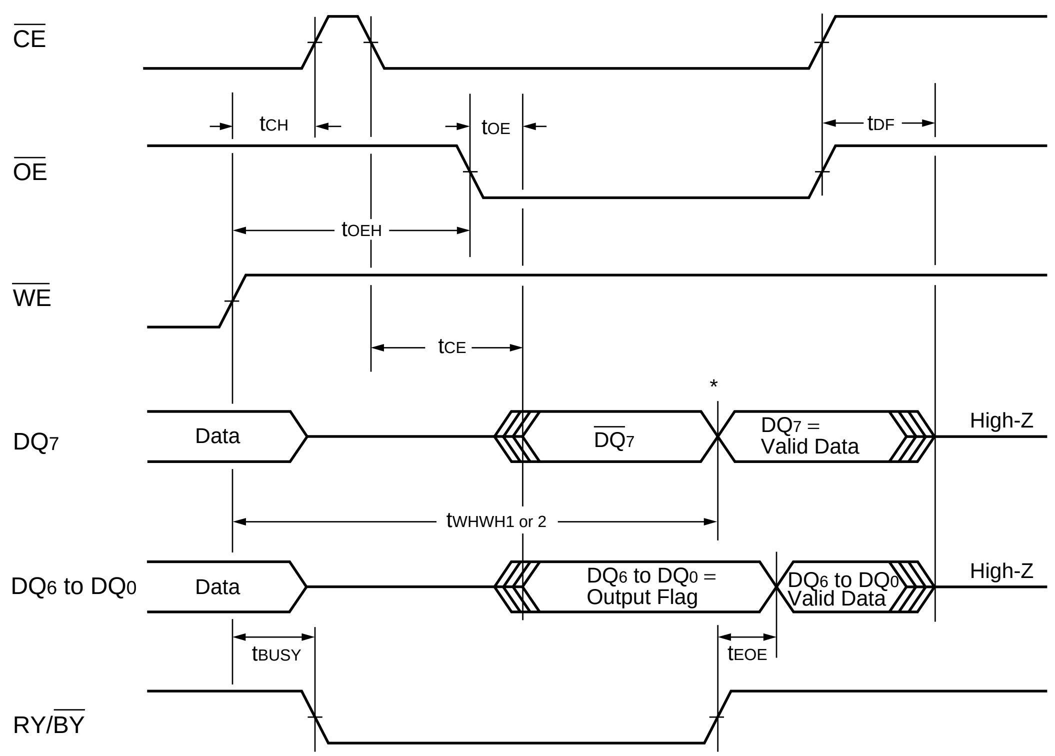
Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram



* : SA is the sector address for Sector Erase. Addresses = 555h (Word) , AAAh (Byte) for Chip Erase.

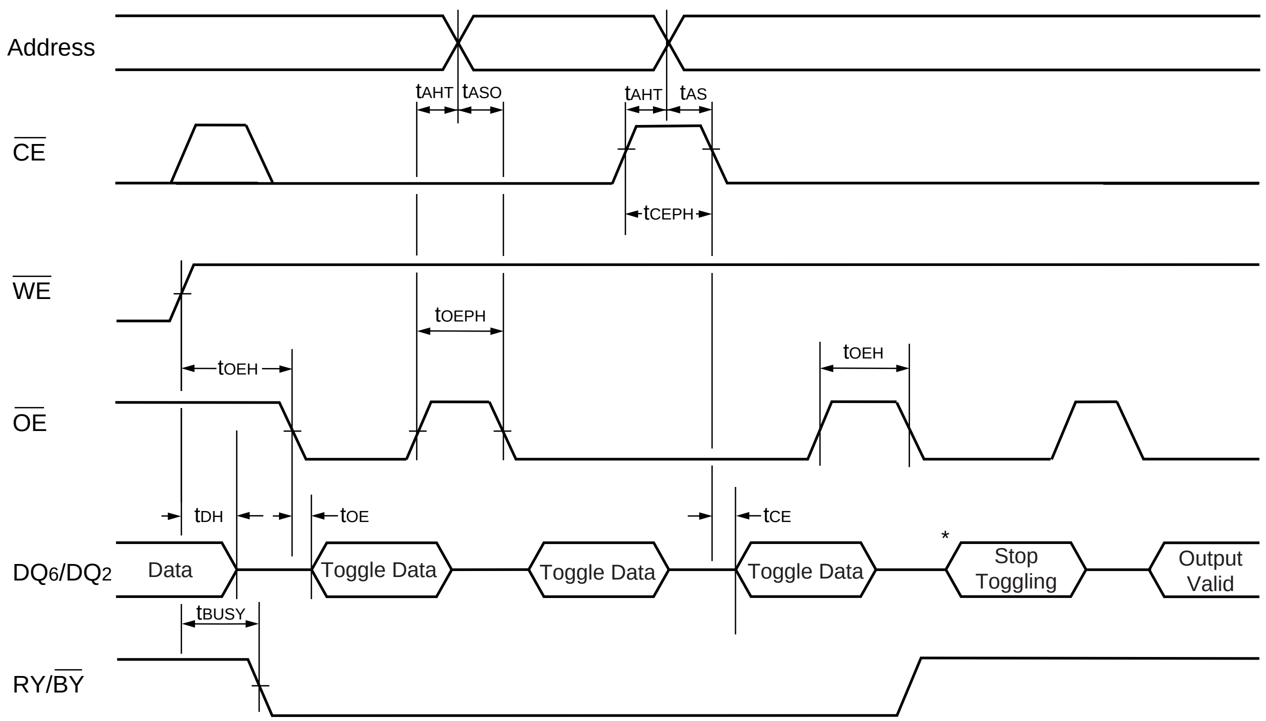
Note: These waveforms are for the ×16 mode (the addresses differ from ×8 mode) .

Chip/Sector Erase Operation Timing Diagram



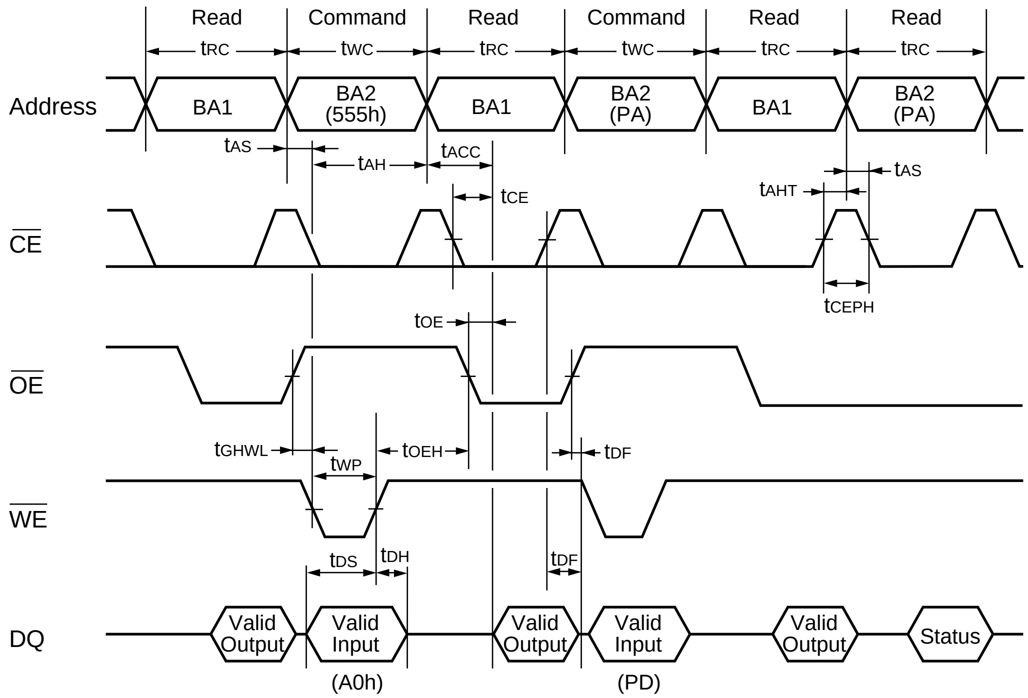
* : DQ_7 = Valid Data (the device has completed the Embedded operation) .

Data Polling during Embedded Algorithm Operation Timing Diagram



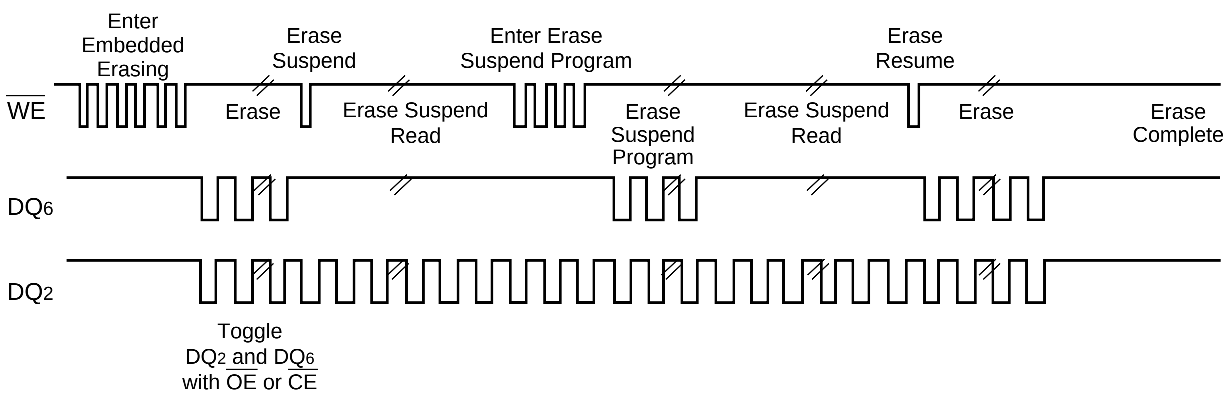
* : DQ_6 stops toggling (the device has completed the Embedded operation) .

Toggle Bit I during Embedded Algorithm Operation Timing Diagram



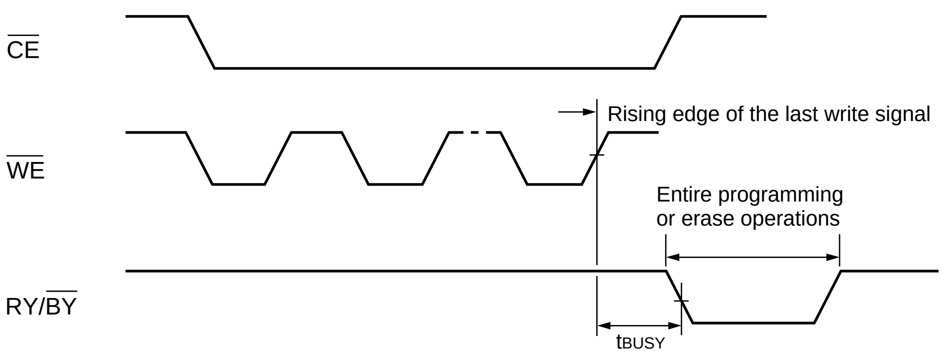
Notes : • This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
• BA1 : Address corresponding to Bank 1
• BA2 : Address corresponding to Bank 2

Bank-to-Bank Read/Write Timing Diagram

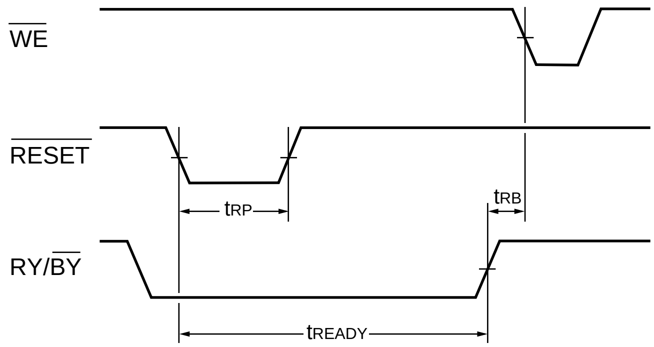


Note : DQ_2 is read from the erase-suspended sector.

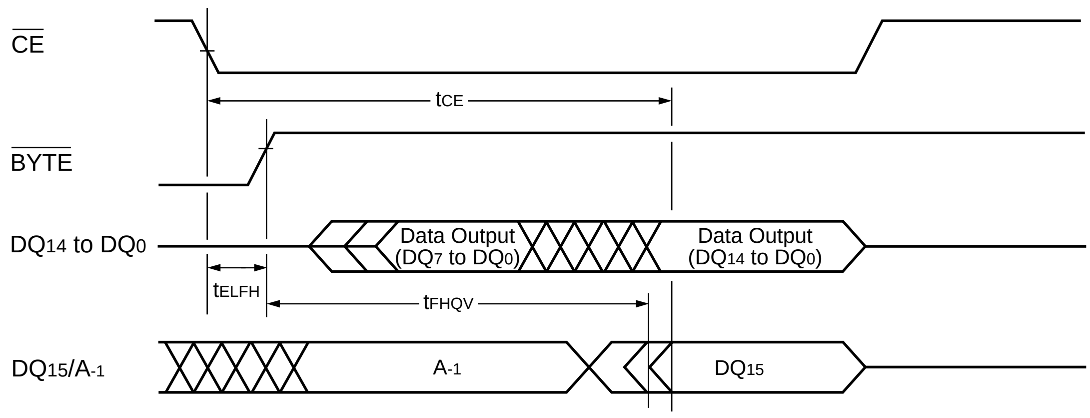
DQ_2 vs. DQ_6



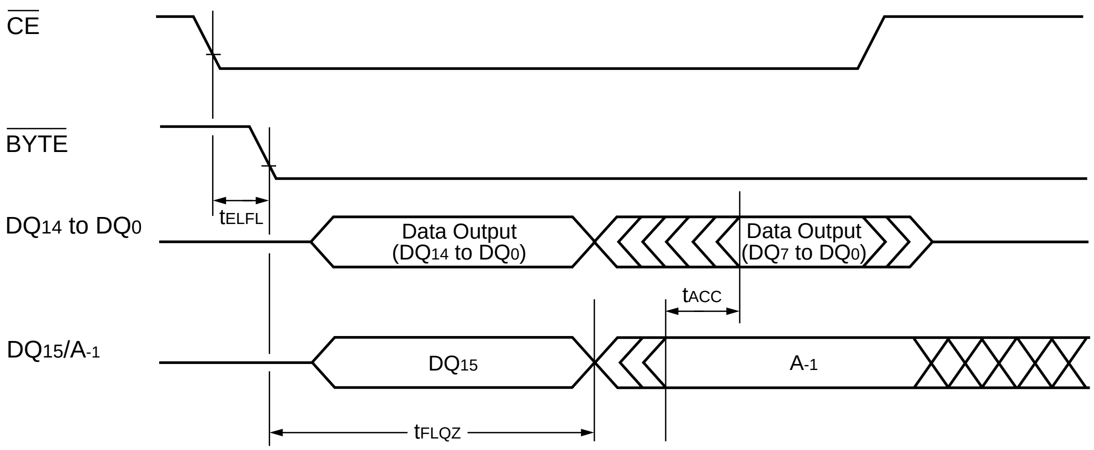
RY/BY Timing Diagram during Program/Erase Operations



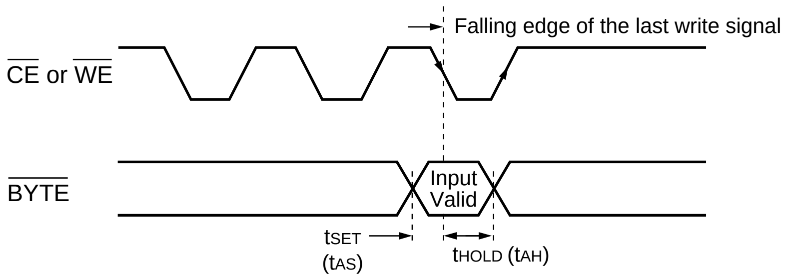
RESET, RY/BY Timing Diagram



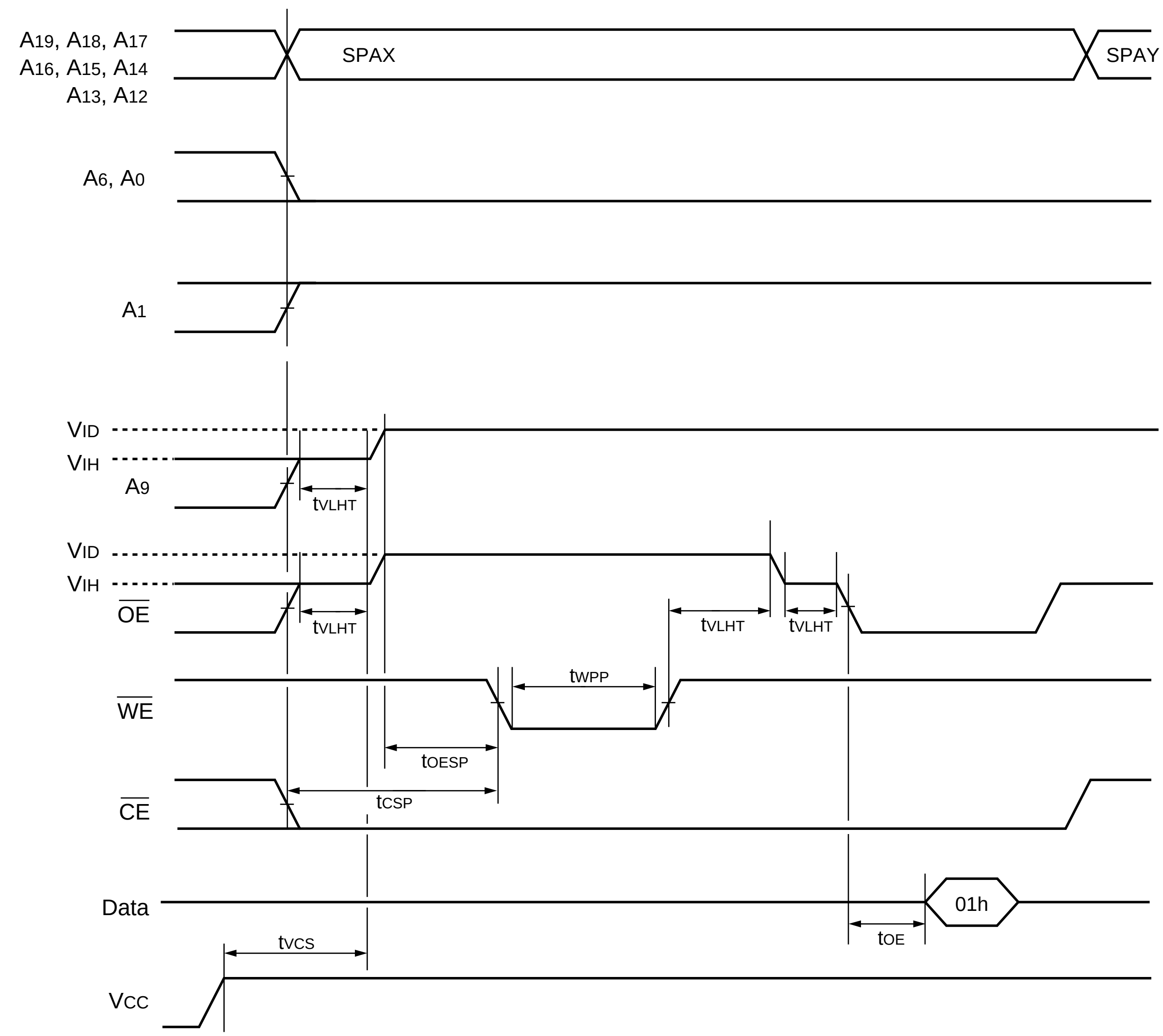
Word Mode Configuration Timing Diagram



Byte Mode Configuration Timing Diagram



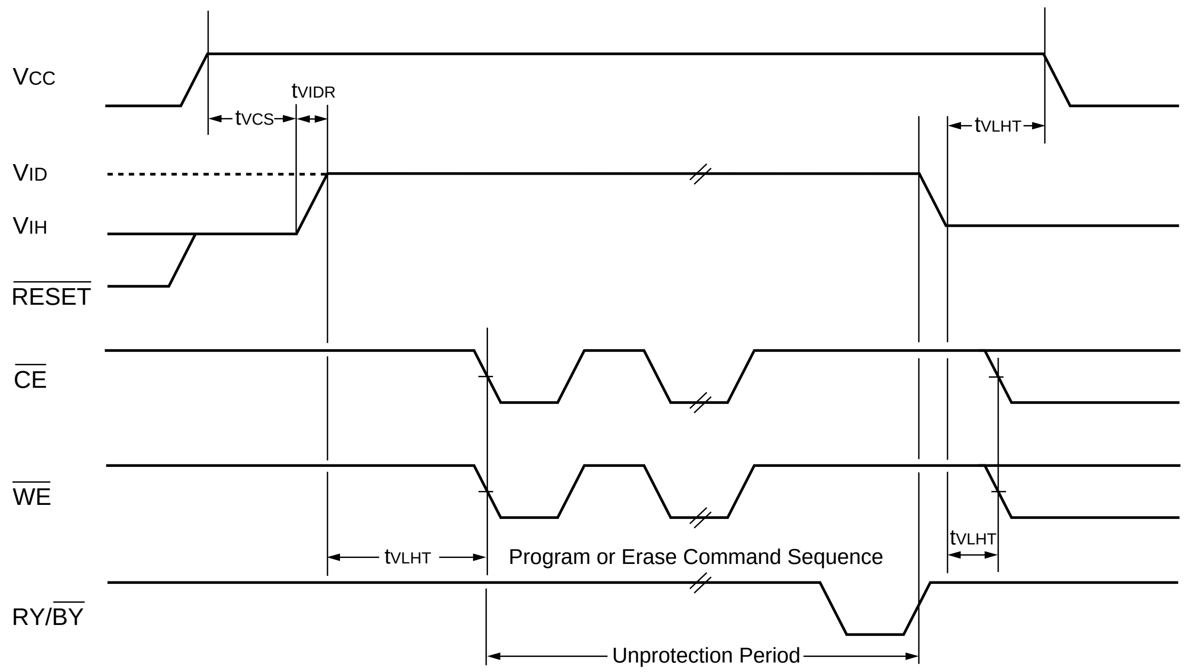
BYTE Timing Diagram for Write Operations



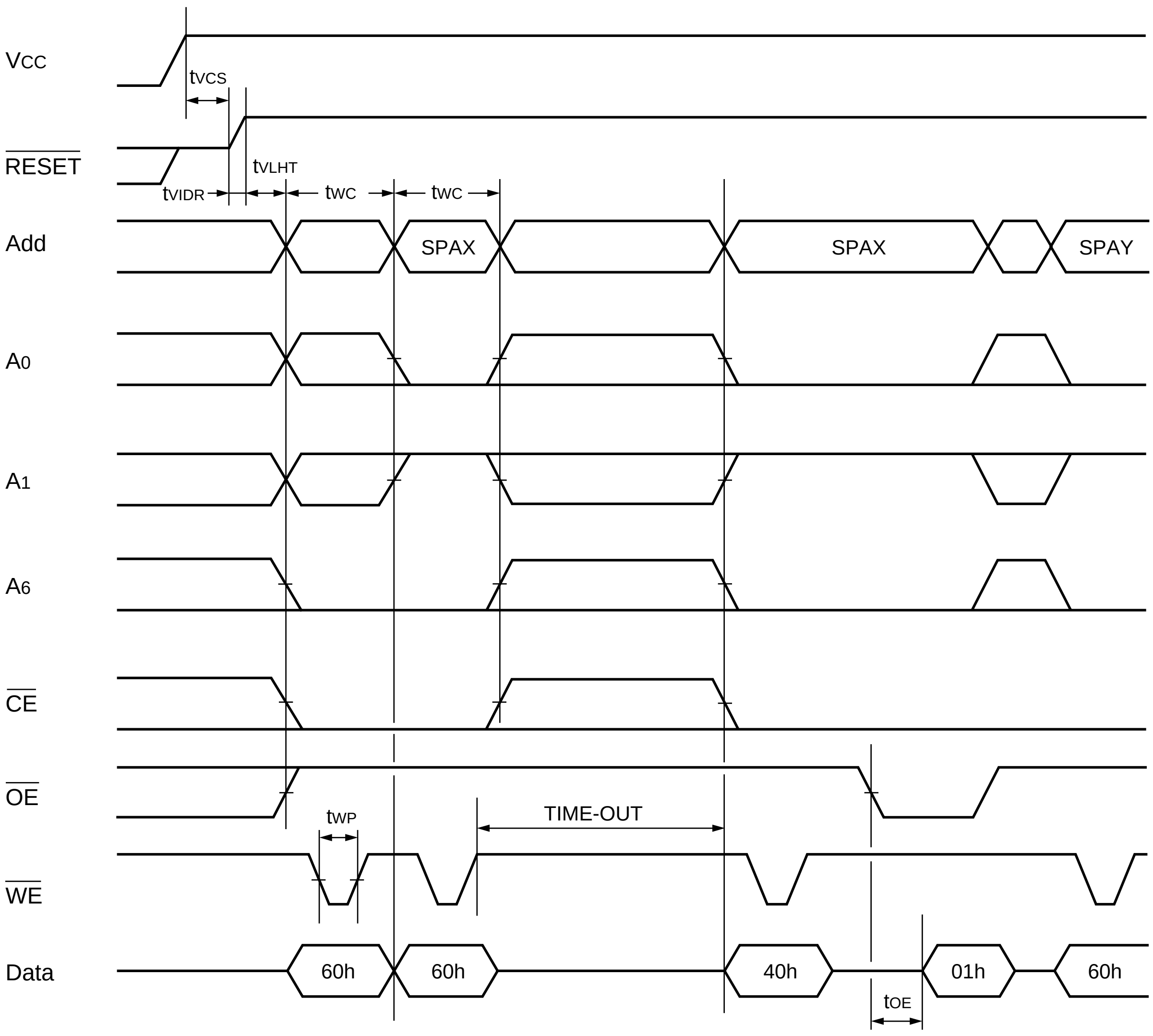
SPAX : Sector Group Address to be protected
SPAY : Sector Group Address to be protected

Note : A_{-1} is V_{IL} on byte mode.

Sector Group Protection Timing Diagram

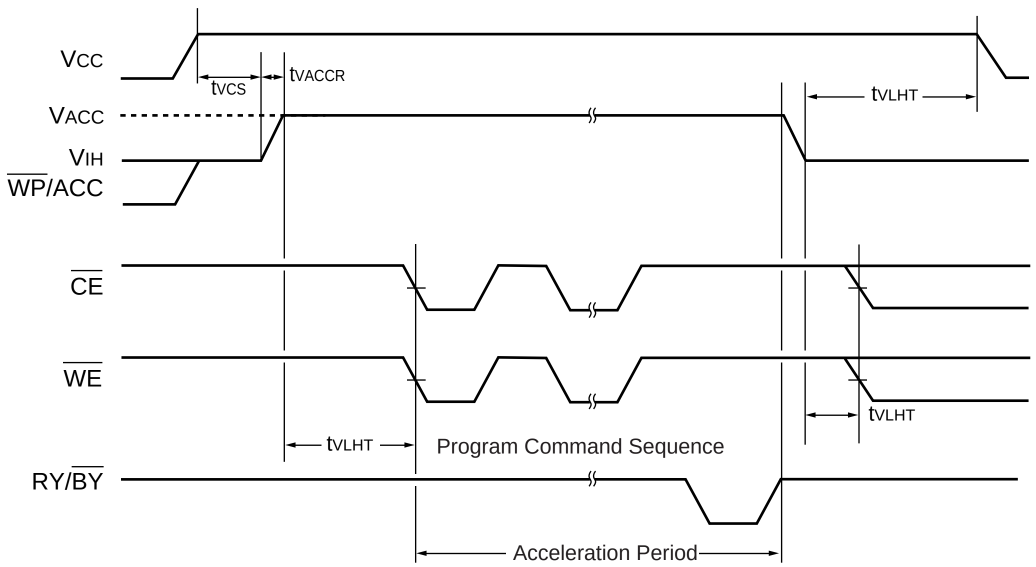


Temporary Sector Group Unprotection Timing Diagram



SPAX : Sector Group Address to be protected
SPAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 250 µs (Min)

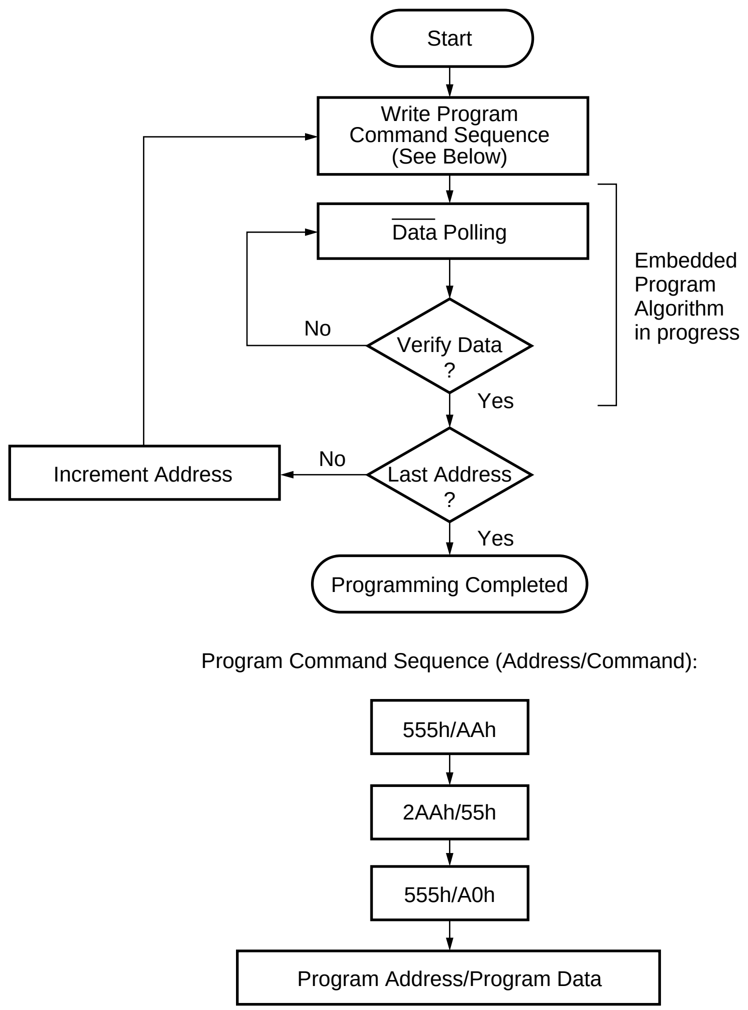
Extended Sector Group Protection Timing Diagram



Accelerated Program Timing Diagram

■ FLOW CHART

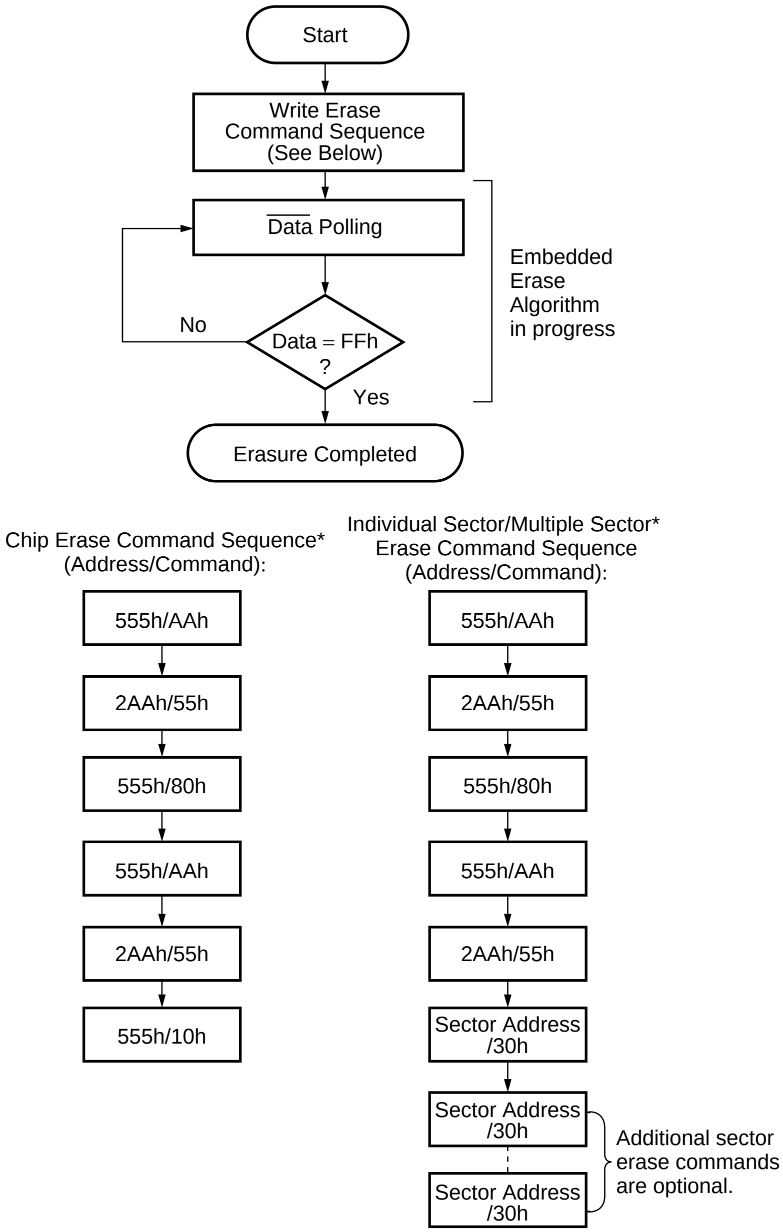
EMBEDDED ALGORITHM



Notes : • The sequence is applied for × 16 mode.
• The addresses differ from × 8 mode.

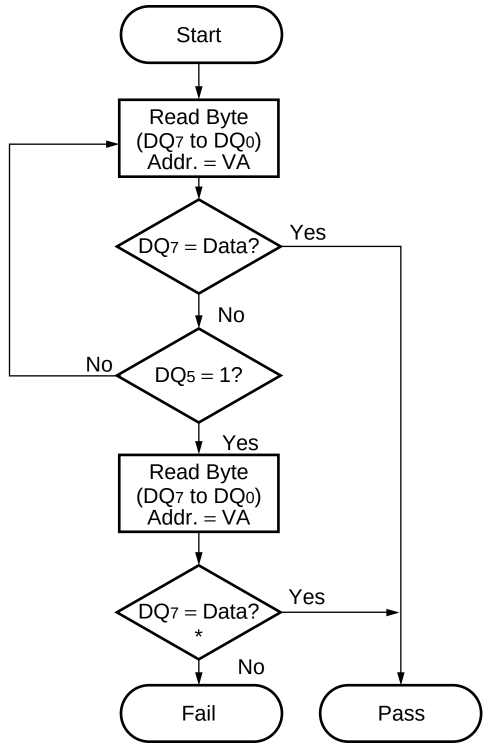
Embedded Program™ Algorithm

EMBEDDED ALGORITHM



* : • The sequence is applied for × 16 mode.
• The addresses differ from × 8 mode.

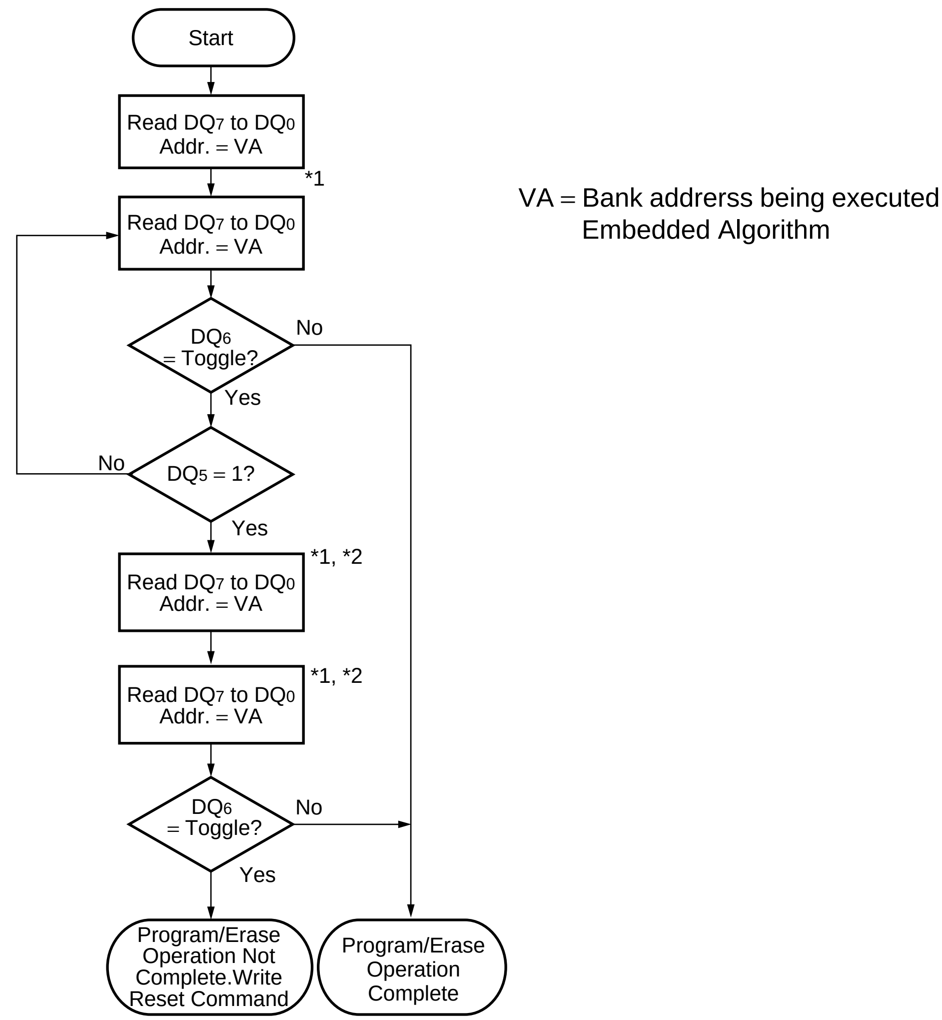
Embedded Erase™ Algorithm



VA = Address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple erases operation
= Any of the sector addresses within the sector not being protected during sector erase or multiple sector erases operation

* : DQ_7 is rechecked even if DQ_5 = “1” because DQ_7 may change simultaneously with DQ_5.

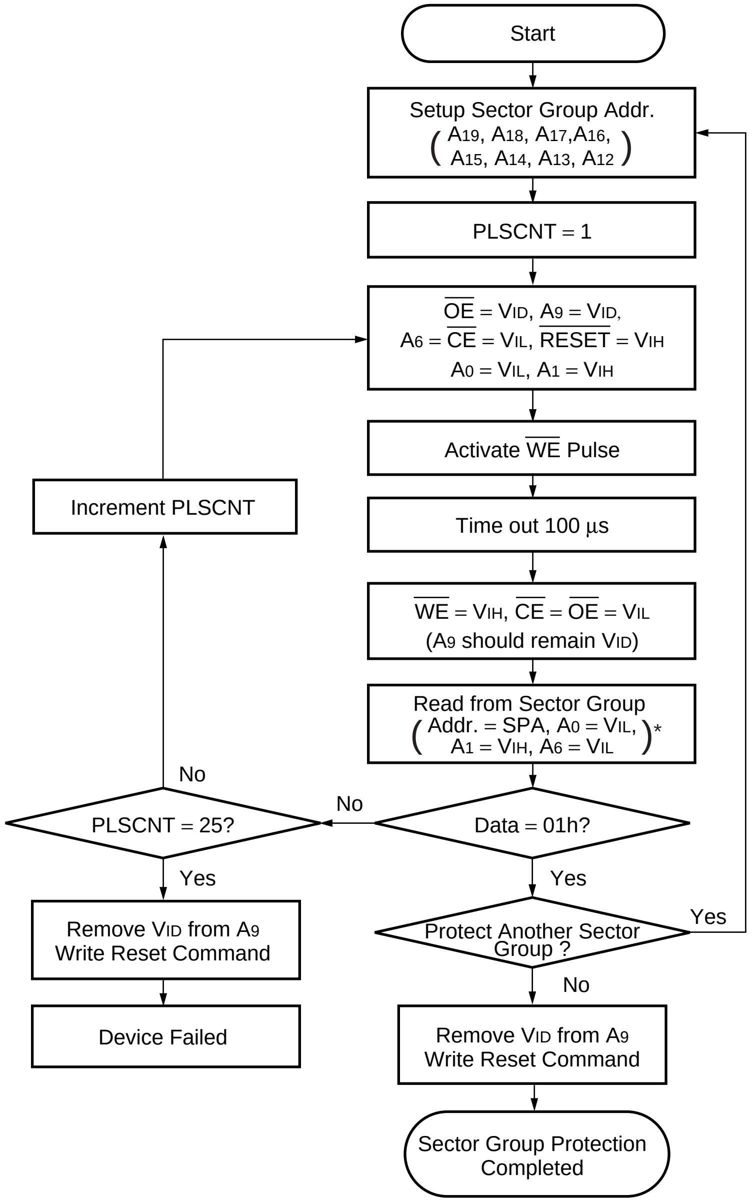
$\overline{\text{Data}}$ Polling Algorithm



*1 : Read toggle bit twice to determine whether it is toggling.

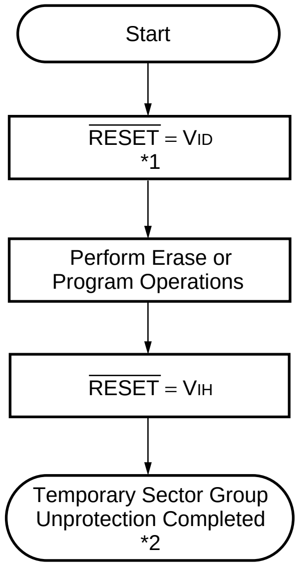
*2 : Recheck toggle bit because it may stop toggling as DQ_5 changes to “1”.

Toggle Bit Algorithm



* : A_{-1} is V_{IL} on byte mode.

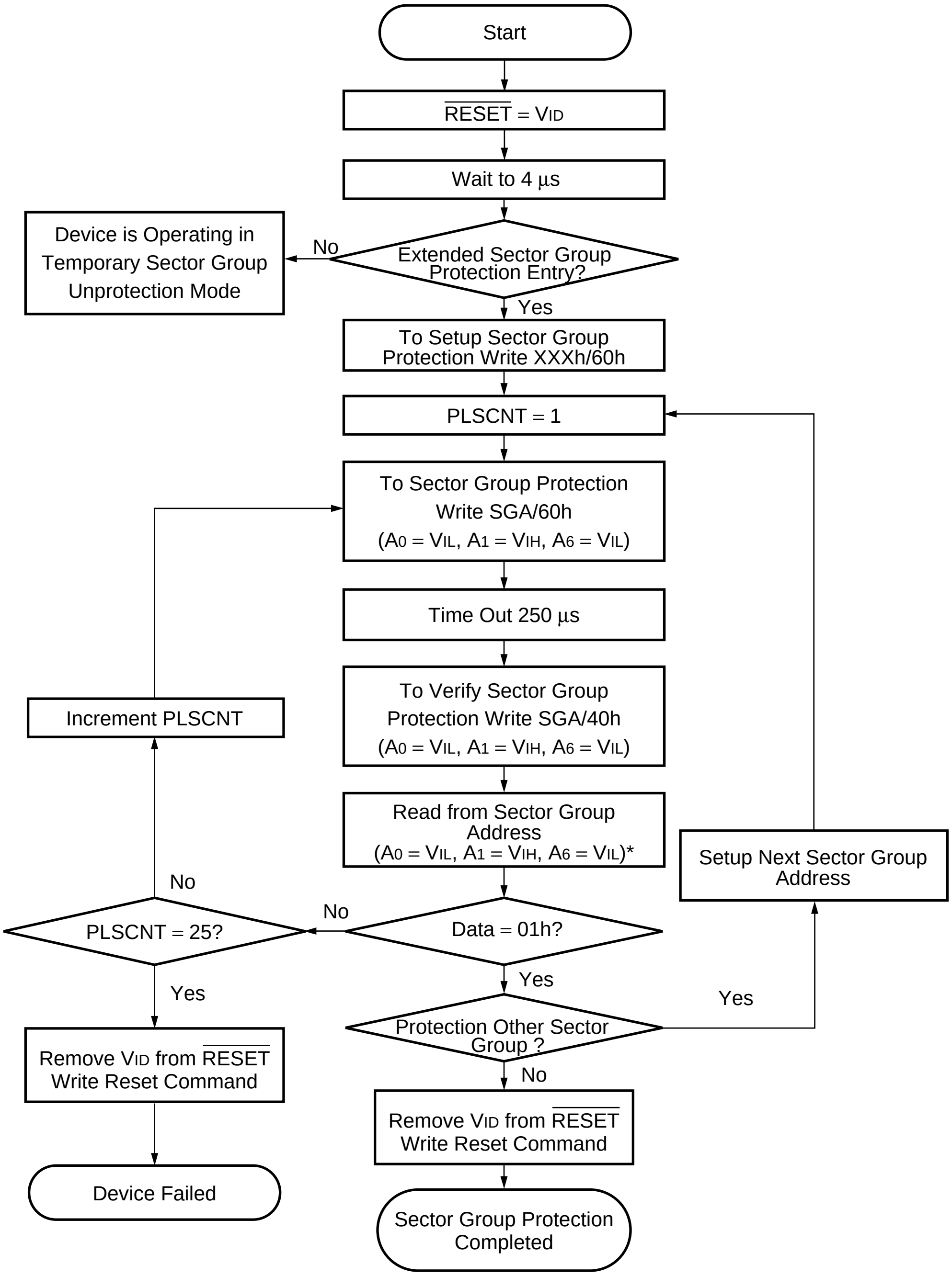
Sector Group Protection Algorithm



*1 : All protected sectors are unprotected.

*2 : All previously protected sectors are protected once again.

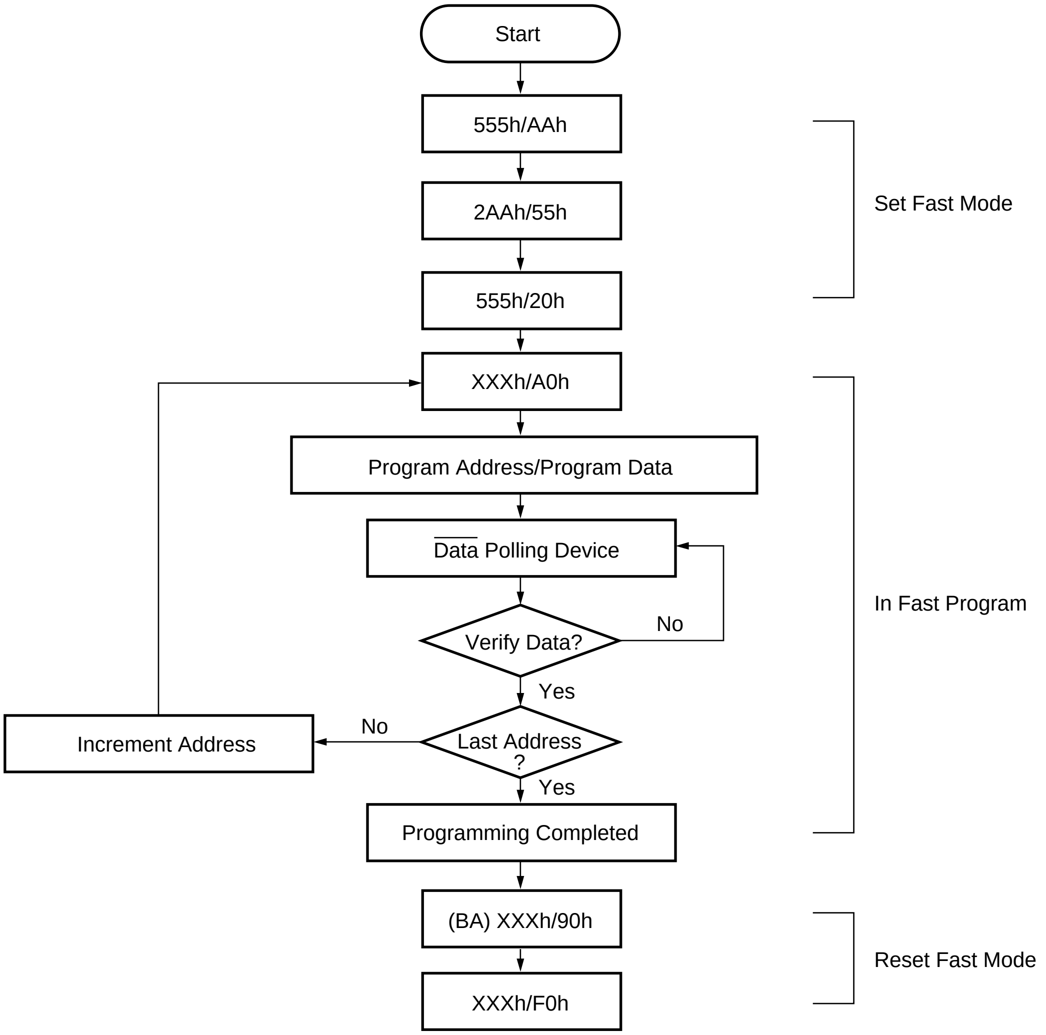
Temporary Sector Group Unprotection Algorithm



* : A_{-1} is V_{IL} on byte mode.

Extended Sector Group Protection Algorithm

FAST MODE ALGORITHM



Embedded Programming™ Algorithm for Fast Mode

■ ORDERING INFORMATION

Standard Products

Fujitsu standard products are available in several packages. The order number is formed by a combination of :

MBM29DS163 T E 10 TN

PACKAGE TYPE
TN = 48-Pin Thin Small Outline Package (TSOP) Normal Bend
TR = 48-Pin Thin Small Outline Package (TSOP) Reverse Bend
PBT = 48-Ball Fine pitch Ball Grid Array Package (FBGA)

SPEED OPTION
See Product Selector Guide

DEVICE REVISION

BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
MBM29DS163
16 Mega-bit (2 M × 8-Bit or 1 M × 16-Bit) CMOS Flash Memory
1.8 V-only Read, Program, and Erase

Valid Combinations		
MBM29DS163TE/BE	10	TN TR PBT

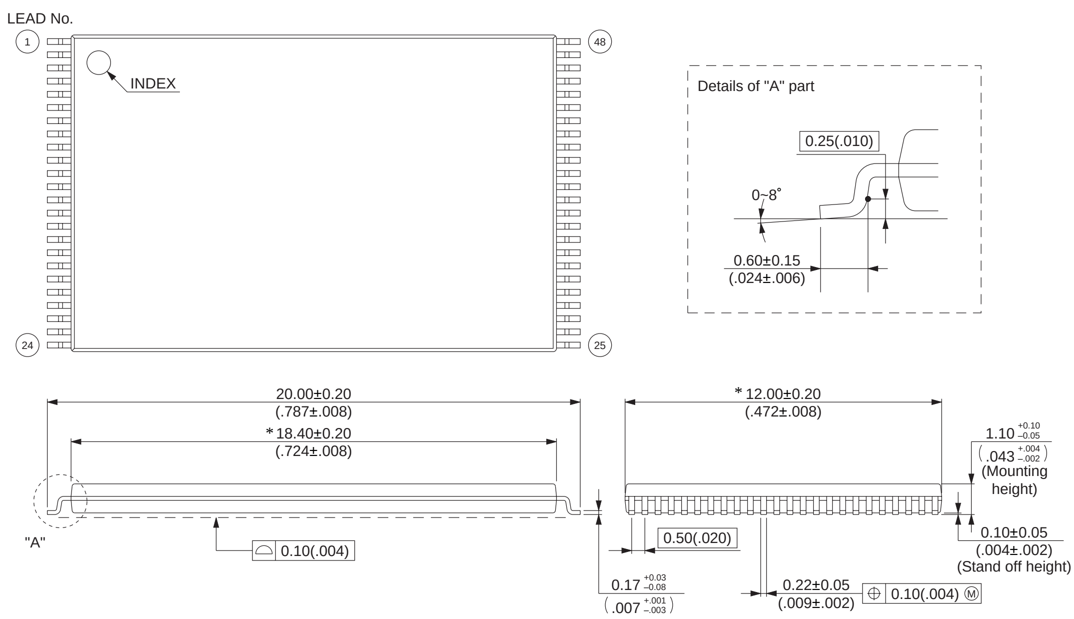
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Fujitsu sales office to confirm availability of specific valid combinations and to check on newly released combinations.

■ PACKAGE DIMENSIONS

48-pin plastic TSOP(1)
(FPT-48P-M19)

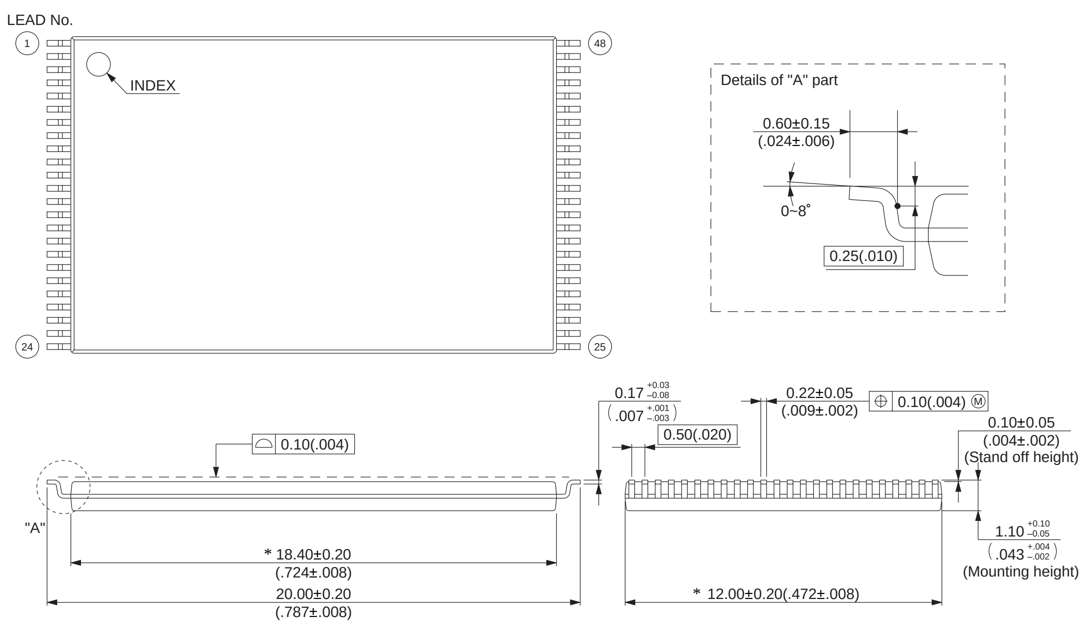
Note 1) * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15(.006)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches)

48-pin plastic TSOP(1)
(FPT-48P-M20)

Note 1) * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15(.006)Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

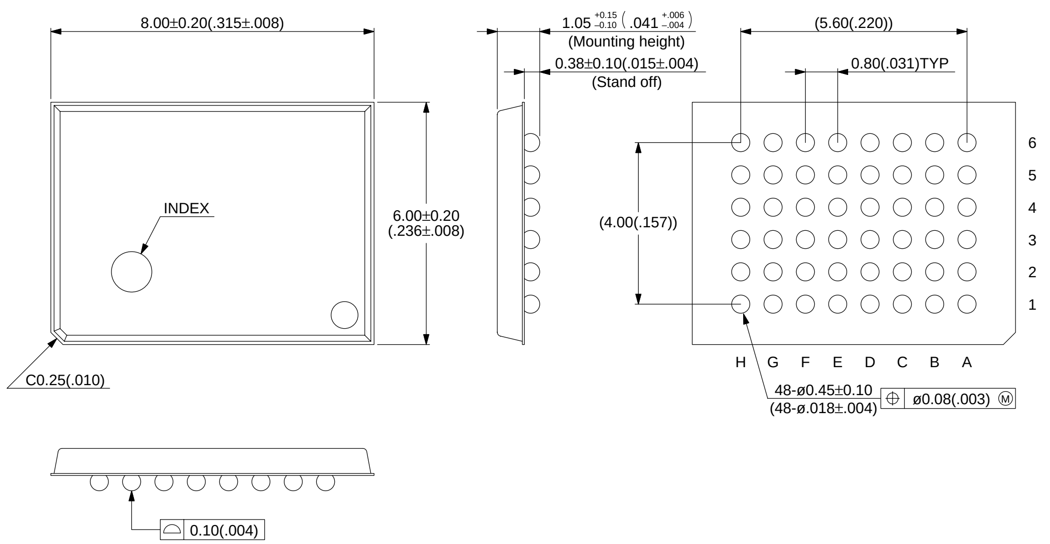


Dimensions in mm (inches)

(Continued)

(Continued)

48-pin plastic FBGA
(BGA-48P-M11)



Dimensions in mm (inches)

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