FUJITSU

CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY

MBM27C1028-15
MBM27C1028-20
MBM27C1028-25

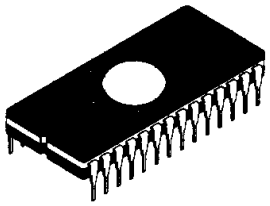
CMOS 1,048,576 BIT UV ERASABLE READ ONLY MEMORY (EPROM)

September 1988
Edition 1.0

The Fujitsu MBM27C1028 EPROM is a high speed read-only static memory that is UV-erasable and reprogrammable. The devices contains 1,048,576 programmable or reprogrammable bits organized in a 131,072-byte/8 bit or 65,536-word/16-bit format. The MBM27C1028 has a mulitplexed address and data pin which permits the device to reduce the number of pin-count for portable system where compact circuit layout is required. The MBM27C1028 can then be housed in a 28-pin DIP or a 32-pad LCC with a transparent lid; when the lid is properly exposed to an ultraviolet light source, a previously programmed bit pattern is erased in approximately 15-to-21 minutes. A new bit pattern can then be written into memory.

The MBM27C1028 EPROM is fabricated using CMOS double polysilicon gate technology with stacked single transistor gate cells. The MBM27C1028 is an excellent choice for system development work and in other applications where program changes are frequently necessary. Once programmed, the device requires only a single +5V power supply; the current requirements are exceptionally low in both the active and standby modes of operation.

- 65,536 word/16 bit organization with on chip decoding
- 16-bit or 8-bit organization capability using a control signal
- On-chip latches for address
- Easy and simple memory expansion via $\overline{OE}$ pin
- Three-state output for word-OR capability
- TTL-compatible inputs/outputs
- Fast access time:
  MBM27C1028-15 = 150ns (max.)
  MBM27C1028-20 = 200ns (max.)
  MBM27C1028-25 = 250ns (max.)
- Single +5V(±10%) power supply with low current drain:
  Active operation = 30mA (max)
  Standby operation = 0.1mA (max)
- Programming voltage: +12.5V(±0.3V)
- Programming capability with Quick Pro™ algorithm
- No interface to be required to MBL8086 and MBL80168
- JEDEC approved pin assignments
- Standard package:
  28-pin Ceramic (Cerdip) DIP Package : suffix = Z
  32-pad Frit seal LCC Package : suffix = TV



CERAMIC PACKAGE
DIP-28C-C01

LCC-32C-F01 See Page 11

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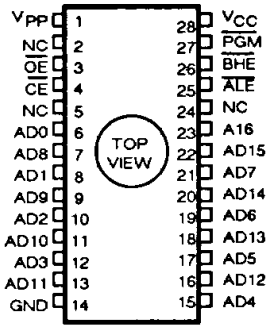
PIN ASSIGNMENT



LCC : See page 11

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7.0	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +14.0	V
All Inputs, I/Os Voltage with Respect to GND	V_{IN}, $V_{I/O}$	-0.6 to V_{CC}+0.3	V
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Storage Temperature	T_{STG}	-65 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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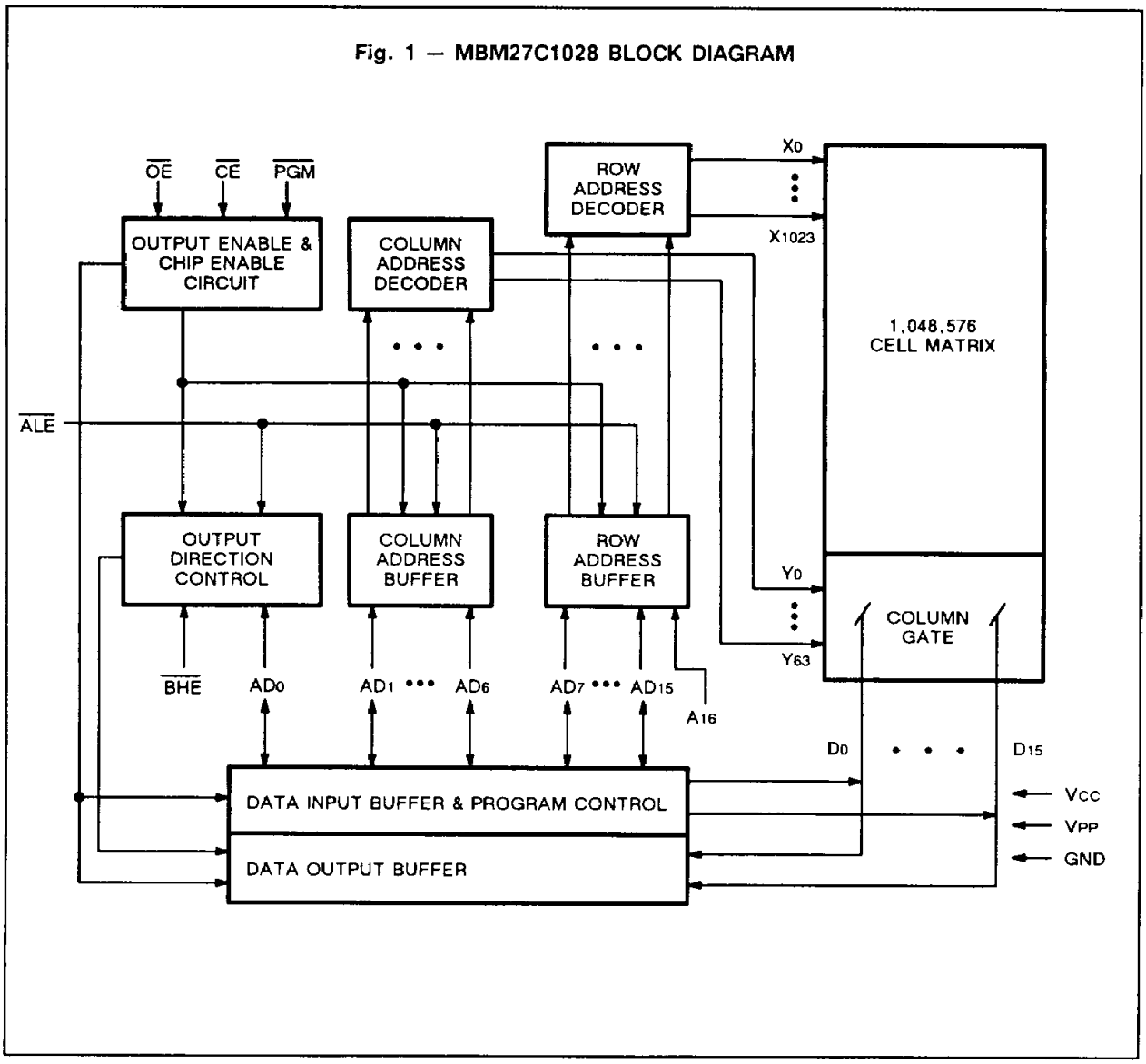
Fig. 1 — MBM27C1028 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}		6	8	pF
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		8	12	pF

PIN DESCRIPTION

Symbol	Pin No. (Pad No.)	Function
V_{PP}	1 (2)	+12.5V programming voltage
NC	2,5,24 (1,3,6,12,17,26,28)	No connection
$\overline{OE}$	3 (4)	Output enable. When $\overline{OE}$ and $\overline{CE}$ are active low and the $\overline{PGM}$ strove is active High; all proper output lines (Either "AD0 to AD15" or "AD0 to AD7" are enabled.
$\overline{CE}$	4 (5)	Chip enable. When active low, the device is enabled for data read and programming operations.
AD0 to AD15	6-13,15-22 (7-11,13-15,18-25)	Address/Data. When $\overline{OE}$ is High, all ADs work as address input line. When Low, all ADs work as data output line.
GND	14 (16)	Circuit ground
A16	23 (27)	Address line (MSB)
$\overline{ALE}$	25 (29)	Address latch enable. When $\overline{CE}$ is Low and $\overline{ALE}$ is High, the address from input buffer is transffer to address decoder by falling edge of $\overline{ALE}$.
$\overline{BHE}$	26 (30)	Bus high enable. When $\overline{BHE}$ is Low in conjection with AD0, a word/16-bit data is available. When $\overline{BHE}$ is High, a byte/8-bit data is avairable.
$\overline{PGM}$	27 (31)	Program Control/Output Enable. When active Low, programming data from the input buffer is written into a specified of memory provided the following conditions are met: VPP=12.5V; VCC=6V, CE=ALE=Low; OE=High.
VCC	28 (32)	+5V Power supply

FUNCTIONAL TRUTH TABLE

Mode \ Pin Name	AD_0	AD_1 - AD_{15}	A_{16}	$\overline{ALE}$	$\overline{BHE}$	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}	GND
STANDBY	High-Z	High-Z	X*1	X	X	V_{IH}	X	X	5V	5V	0V
READ ADDRESS LATCH	X*2	A_{IN}	A_{IN}	↓	X*2	V_{IL}	V_{IH} / X	X / V_{IL}	5V	5V	0V
READ	D_{OUT}*2	D_{OUT}*2	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IH}	5V	5V	0V
OUTPUT DISABLE	High-Z	High-Z	X	VIL	X	VIL	V_{IH} / X	X / V_{IL}	5V	5V	0V
PROGRAM ADDRESS LATCH	V_{IL}	A_{IN}	A_{IN}	↓	V_{IL}	V_{IL}	V_{IH}	V_{IH}	6V	12.5V	0V
PROGRAM	D_{IN}	D_{IN}	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IL}	6V	12.5V	0V
RROGRAM VERIFY	D_{OUT}	D_{OUT}	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IH}	6V	12.5V	0V
PROGRAM INHIBIT	High-Z	High-Z	X	X	X	V_{IH}	X	X	6V	12.5V	0V

Note *1: X can be either V_{IL} or V_{IH}.

*2: See below.

AD0 and $\overline{BHE}$ should be basically used to enable for the lower and upper byte of the data, respectivery. But when both AD0 and $\overline{BHE}$ are high, it enable to transfer the upper byte data to lower byte bus, AD0 to AD7; thus, if $\overline{BHE}$ pulled High, the MBM27C1028 can be used for byte wide/8-bit memory, organized 128K words by 8 bit.

AD0	$\overline{BHE}$	AD0 to AD7	AD8 to AD15
V_{IL}	V_{IL}	D0 to D7	D8 to D15
V_{IL}	V_{IH}	D0 to D7	High-Z
V_{IH}	V_{IL}	High-Z	D8 to D15
V_{IH}	V_{IH}	D8 to D15	High-Z

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{CC}-0.6	V_{CC}	V_{CC} +0.6	V
Operating Temperature	T_A	0		70	°C

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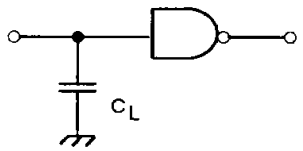
DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Load Current V_{IN} = 5.5V)	$\|I_{LI}\|$			10	µA
Output Leakage Current (V_{OUT}=5.5V)	$\|I_{LO}\|$			10	µA
V_{PP} Supply Current	I_{PP_1}		1	100	µA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{SB_1}		0.3	1	mA
V_{CC} Standby Current ($\overline{CE}$ =V_{CC} +0.3V)	I_{SB_2}		1	100	µA
V_{CC} Active Current ($\overline{CE}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC_1}		10	30	mA
V_{CC} Operation Current (f = 4MHz, I_{OUT} = 0mA)	I_{CC_2}		8	30	mA
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = -400 µA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = -100 µA)	V_{OH2}	V_{CC}-0.7			V

Fig. 2 — AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input pulse levels:	0.45V TO 2.4V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs
	0.8V and 2.0V for outpust
Output Load:	1 TTL gate and C_L =100pF



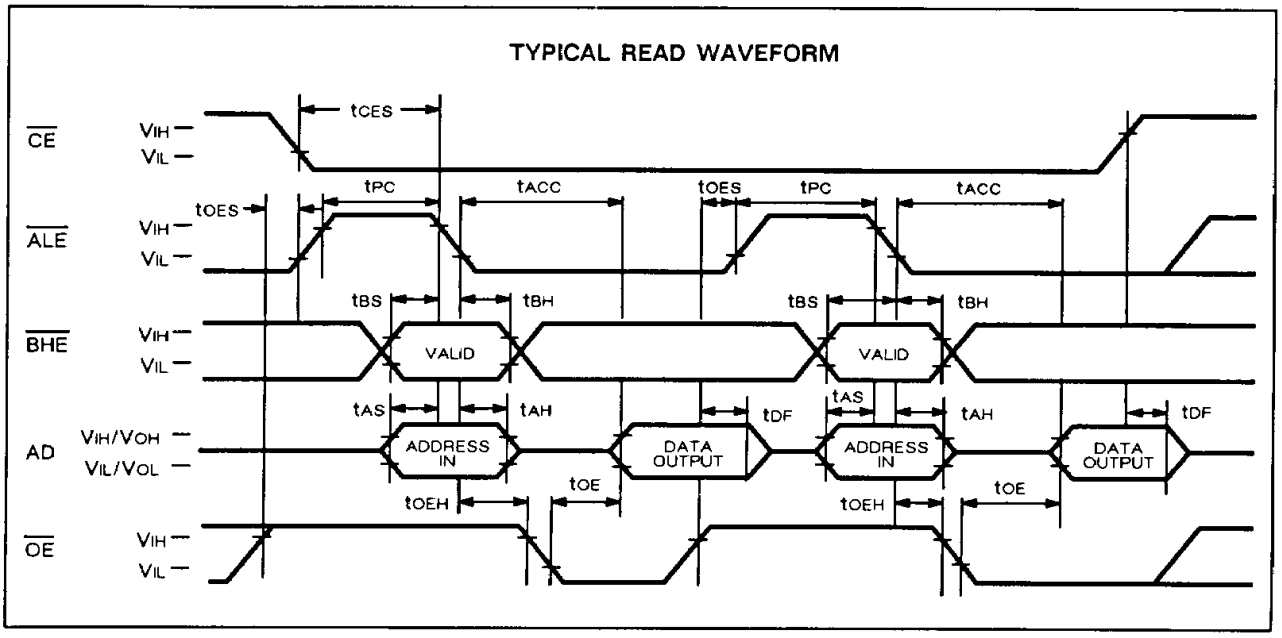
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C1028-15			MBM7C1028-20			MBM27C1028-25			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$\overline{ALE}$ Active to Output Valid ($\overline{CE}$=$\overline{OE}$=V_{IL}, $\overline{PGM}$=V_{IH})	t_{ACC}			150			200			250	ns
$\overline{ALE}$ Precharge Time ($\overline{CE}$=V_{IL})	t_{PC}	60			75			100			ns
$\overline{CE}$ Setup Time	t_{CES}	60			75			100			ns
Address Setup Time	t_{AS}	20			25			30			ns
Address Hold Time	t_{AH}	20			25			30			ns
$\overline{BHE}$ Setup Time	t_{BS}	20			25			30			ns
$\overline{BHE}$ Hold Time	t_{BH}	20			25			30			ns
$\overline{OE}$ Setup Time	t_{OES}	0			0			0			ns
$\overline{OE}$ Hold Time	t_{OEH}	20			25			30			ns
$\overline{OE}$ to Output Valid*1 ($\overline{PGM}$=V_{IH})	t_{OE}	0		70	0		70	0		100	ns
$\overline{PGM}$ to Output Valid*1 ($\overline{OE}$=V_{IL})	t_{PGM}	0		70	0		70	0		100	ns
Ooutput Disable to Output Float*3	t_{DF}	0		60	0		60	0		60	ns

NOTE: *1 $\overline{OE}$ ($\overline{PGM}$) may be delayed up to t_{ACC}-t_{OE} (t_{PGM}) after the falling edge of $\overline{ALE}$.
*2 t_{DF} is specified from $\overline{CE}$, $\overline{OE}$ or $\overline{PGM}$ or $\overline{ALE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

TYPICAL READ WAVEFORM



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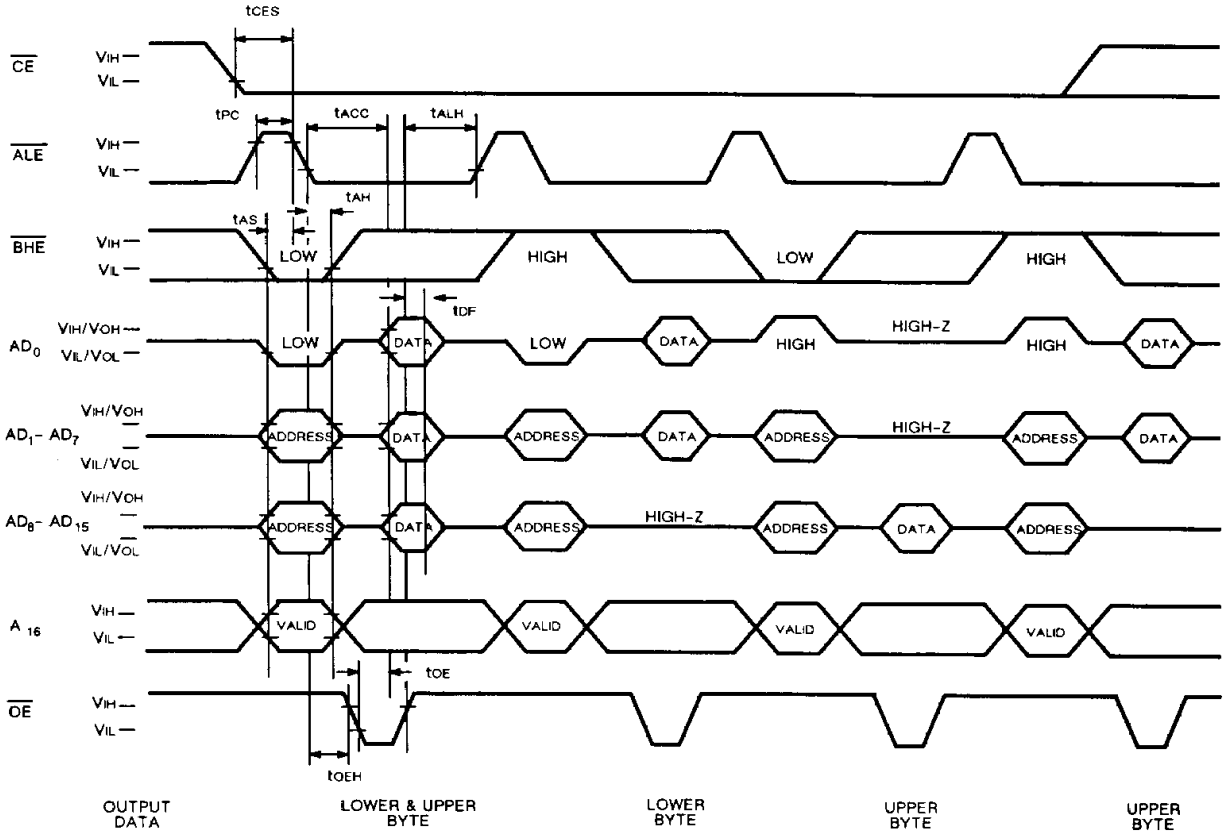
READ WAVEFORM



PROGRAMMING / ERASING INFORMATION

PROGRAMMING

When the MBM27C1028 is shipped the factory, all memory cells (1,048,576 bits) are set to High state (logic 1). During the programming procedure, affected bit cells are set to the Low state (logic 0).

The MBM27C1028 is programmed with a fast programming algorithm design by Fujitsu called Quick Pro™. When +12.5V(±0.3V) is applied to Vpp, +6V(±0.25V) is applied to Vcc, $\overline{CE}$ = V_{IL}, $\overline{PGM}$ and $\overline{OE}$ = V_{IH}, the programming mode is initiated. Next, the proper address in conjection with $\overline{BHE}$ are input by falling edge of $\overline{ALE}$, and the data pattern is applied to the input buffer (Figure1). When both address (and $\overline{BHE}$) and data are stable, a 0.5ms negative pulse is applied to the $\overline{PGM}$. Upon verification of written data read out by $\overline{OE}$ an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complate the programming of one byte. Refer to the PROGRAMMING FLOWCHART that follows for step-by-step programming procedures.

Caution

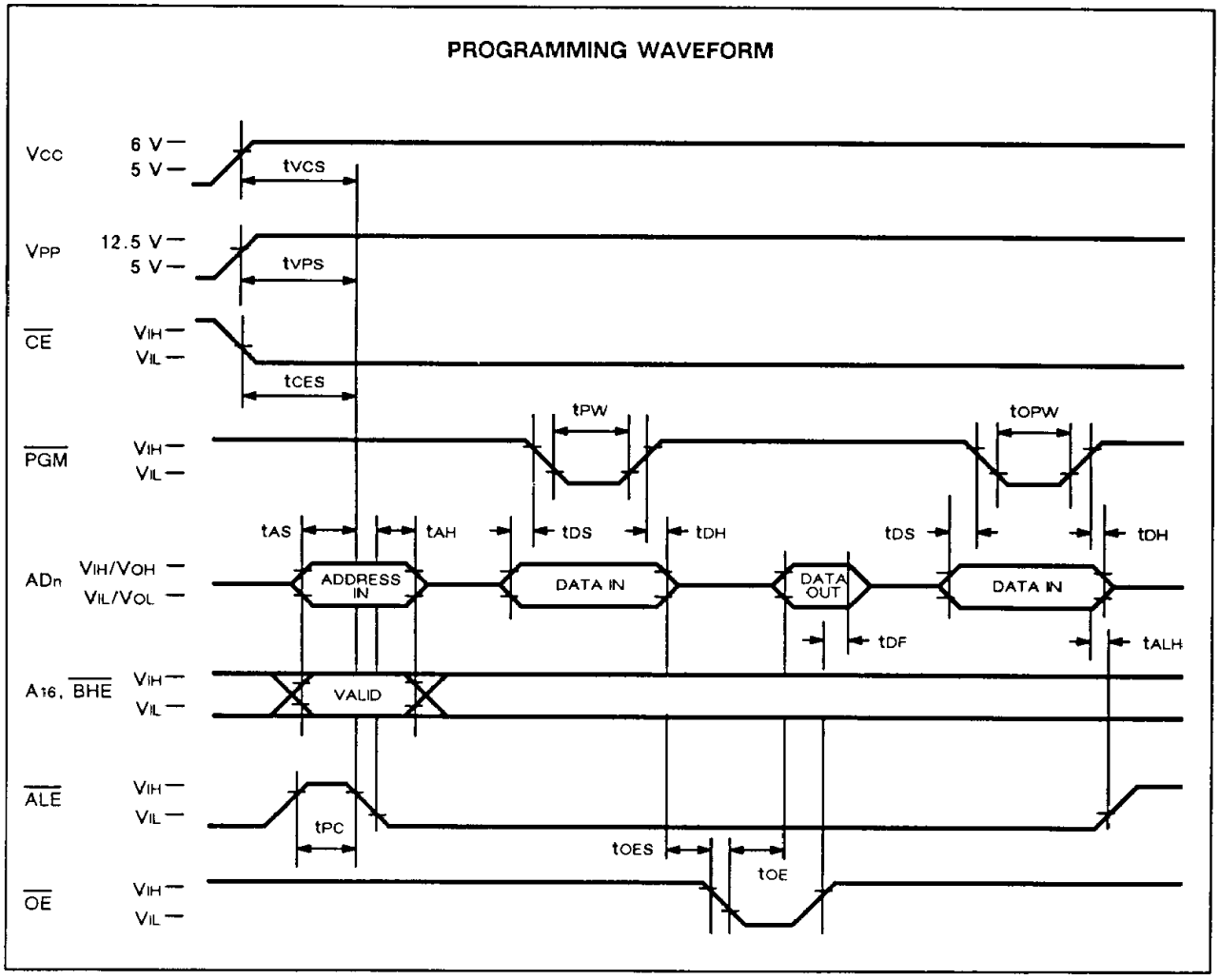
The width of one programming pulse must not exceed 40ms; thus, a continuous TTL low-level voltage should not be applied to the $\overline{PGM}$. Also, a 0.1µF capacitor must be connected between V_{PP} and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

ERASING

In order to clear all memory cells of programmed contents, the MBM27C1028 must be exposed to an ultraviolet light source. To completely erase the memory (restore all cells to a logic 1 state), a dosage of 15Wsec/cm^2 is required. The required exposure can be obtained by using a UV-lamp with a wavelength of 253.7nm with an intensity of 12mW/cm^2. Remove all filters from the lamp and clean the transparent lid of the MBM27C1028 with a non-abrasive cleaner. Hold the MBM27C1028 approximately one inch from the light source for 15-to-21 mimute. (Note. The MBM27C1028 and other similar devices can be erased by light sources with longer wavelength; however, the erasing time is much greater. Nonetheless, exposure to fluorescents or sunlight will severely degrade and eventually erase the memory. When used in a lighted environment, it is recommended that the transparent window be covered with an opaque label.)

PROGRAMMING / ERASING INFORMATION (Cont'd)

PROGRAMMING WAVEFORM



DC CHARACTERISTICS DURING PROGRAMMING

(T_A= 25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Input Low Level	V_{IL}	-0.1		0.8	V
Input Load Current	I_{LI}	-10		10	μA
V_{CC} Supply Current ($\overline{CE}$=V_{IH})	I_{SB3}			1	mA
V_{CC} Supply Current ($\overline{CE}$=V_{CC}± 0.3 V)	I_{SB4}		1	100	μA
V_{PP} Supply Current ($\overline{CE}$=V_{IL})	I_{CC3}			30	mA
V_{PP} Supply Current ($\overline{CE}$=$\overline{PGM}$=V_{IL}, OE=V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{PGM}$=V_{IH})	I_{PP3}			5	mA
Output Low Level (I_{OL}=2.1mA)	V_{OL}			0.45	V
Output High Level (I_{OH}=-400 μA)	V_{OH}	2.4			V

AC CHARACTERISTICS DURING PROGRAMMING

(T_A= 25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
V_{CC} Setup Time	t_{VCS}	4			μS
V_{PP} Setup Time	t_{VPS}	4			μS
$\overline{CE}$ Setup Time	t_{CES}	4			μS
Address Setup Time	t_{AS}	1			μS
Address Hold Time	t_{AH}	1			μS
$\overline{ALE}$ Precharge Time	t_{PC}	2			μS
$\overline{ALE}$ Low Hold Time	t_{ALH}	2			μS
Data Setup Time	t_{DS}	2			μS
Data Hold Time	t_{DH}	2			μS
$\overline{OE}$ Setup Time	t_{OES}	2			μS
$\overline{OE}$ to Output Valid	t_{OE}			100	ns
$\overline{OE}$ to Output Float	t_{DF}			60	ns
Programming Pulse Width	t_{PW}	0.475	0.50	0.525	ms
Over Programming Pulse Number	n	1		25	times

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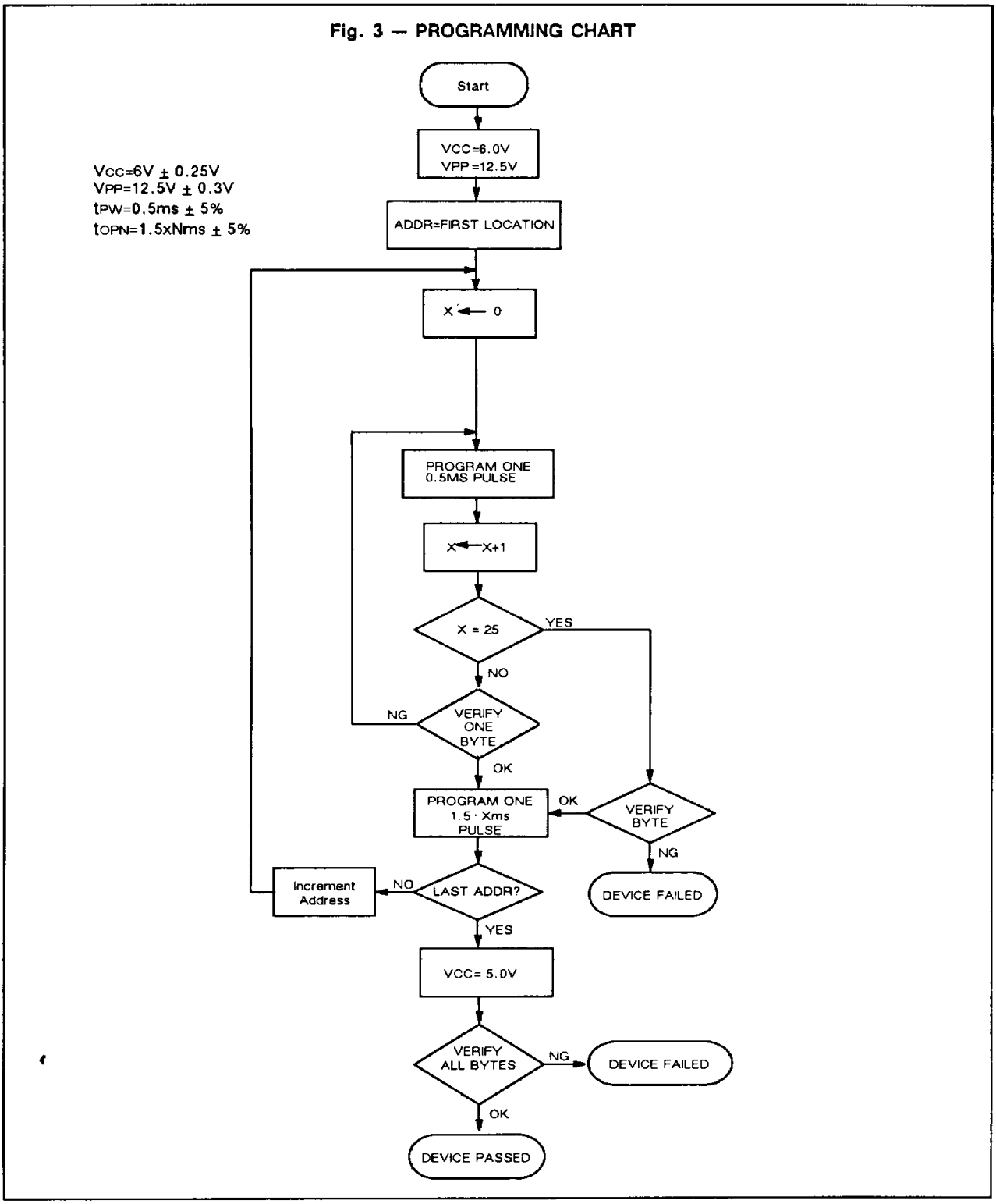
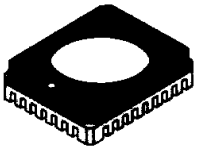
Fig. 3 — PROGRAMMING CHART

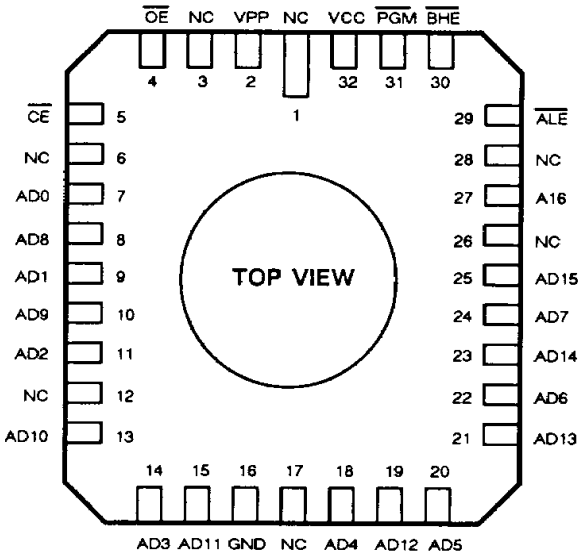


PACKAGE DIMENSIONS

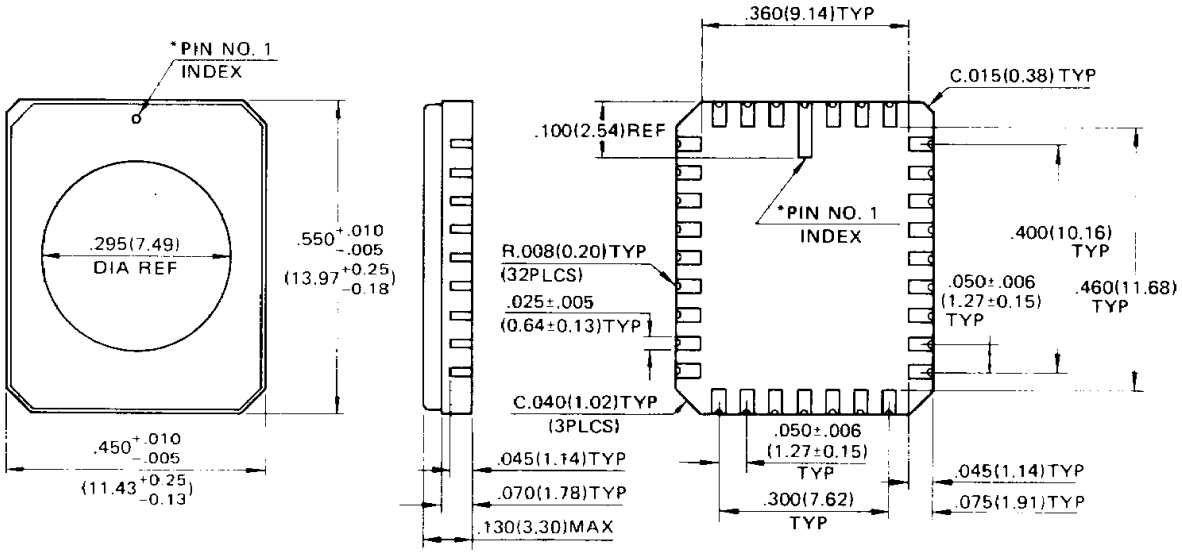


LCC-32C-F01

PIN ASSIGNMENT



32-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(Case No.: LCC-32C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in inches and (millimeters)

PACKAGE DIMENSIONS

28-PIN CERAMIC DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-C01)