FUJITSU
MICROELECTRONICS

MBM2732-35
MBM2732-45

UV ERASABLE 32,768-BIT READ ONLY MEMORY

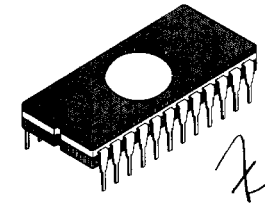
NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MBM2732A.

DESCRIPTION

The Fujitsu MBM2732 is a high speed 32,768-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

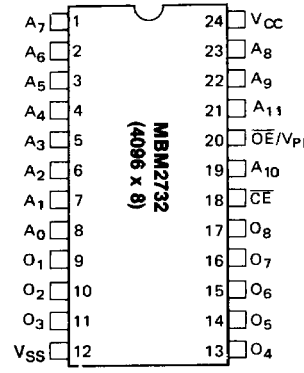
A 24-pin dual-in-line package with a transparent lid is used to package the MBM2732. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM2732 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 4096 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



CERDIP PACKAGE
DIP-24C-C02

PIN ASSIGNMENT



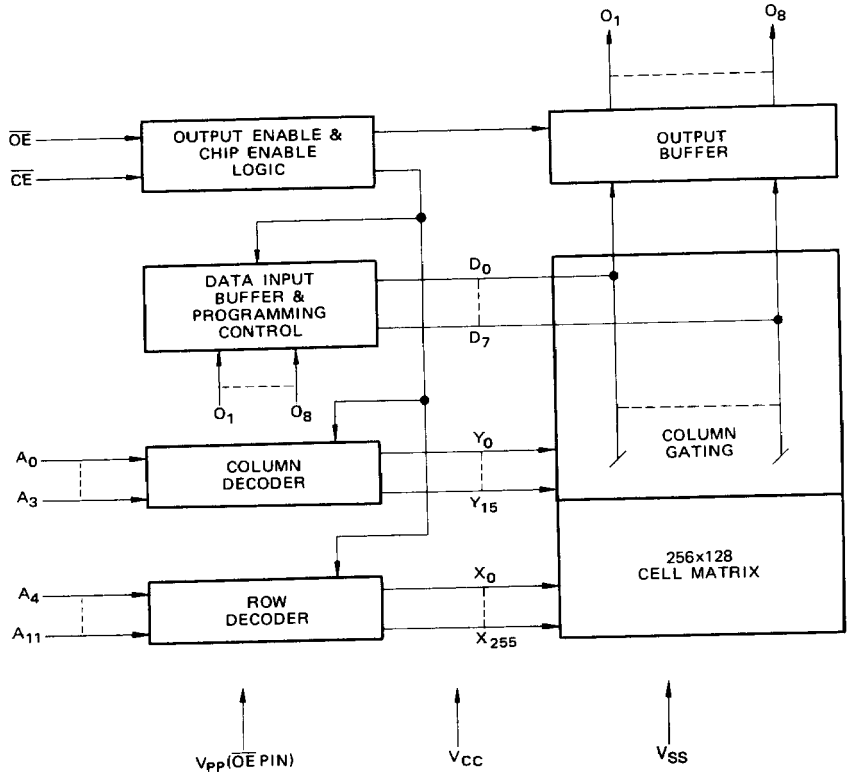
FEATURES

- **4096 words by 8-bits organization, fully decoded**
- **Simple programming requirements**
- **Single location programming**
- **Programs with one 50ms pulse**
- **Low power requirement:**
  825mW max (active)
  165mW max (standby)
- **No clocks required (fully static operation)**
- **TTL compatible inputs and outputs**
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Fast access time:**
  MBM2732-35 350ns
  MBM2732-45 450ns
- **Single +5V operation**
- **Standard 24-pin DIP package**
- **Pin compatible with Intel 2732**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MBM2732A.

Fig. 1 — MBM2732 BLOCK DIAGRAM



CAPACITANCE

(T_A = 25°C; f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (Except $\overline{OE}/V_{PP}$, V_{IN} = 0V)	C_{IN1}	—	4	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance (V_{IN} = 0V)	C_{IN2}	—	14	20	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	12	pF

NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MBM2732A.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs (Except $\overline{OE}/V_{PP}$) with Respect to V_{SS}	V_{IN}, V_{OUT}	−0.3 to +7	V
Output Enable/Program Input with Respect to V_{SS}	$\overline{OE}/V_{PP}$	−0.3 to +26.5	V
V_{CC} with Respect to V_{SS}	V_{CC}	−0.3 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONS AND PIN CONNECTIONS $V_{CC}(24) = +5$, $V_{SS}(12) = GND$

Mode \ Function (Pin No.)	Address Input (1~8,19,21~23)	Data I/O (9~11,13~17)	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	I_{CC} Supply (24)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	I_{CC2}
Stand By	Don't Care	High Z	V_{IH}	Don't Care	I_{CC1}
Program	A_{IN}	D_{IN}	V_{IL}	V_{PP}	I_{CC2}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	I_{CC2}
Program Inhibit	Don't Care	High Z	V_{IH}	V_{PP}	I_{CC1}

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS} = GND)

Parameter		Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage(1)	MBM2732-35	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	MBM2732-45		4.75	5.0	5.25		
Supply Voltage		V_{SS}	—	GND	—	V	
Input High Voltage		V_{IH}	2.0	—	V_{CC} +1	V	
Input Low Voltage		V_{IL}	−0.1	—	0.8	V	

Note: (1) V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC CHARACTERISTICS

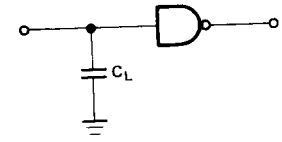
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.5V)	I_{LO}	—	—	10	μA
V_{CC} Supply Current (Standby)	I_{CC1}	—	—	30	mA
V_{CC} Supply Current (Active)	I_{CC2}	—	—	150	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MBM2732A.

Fig. 2 — AC TEST CONDITIONS (Including Programming)

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Time:	≤ 20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF

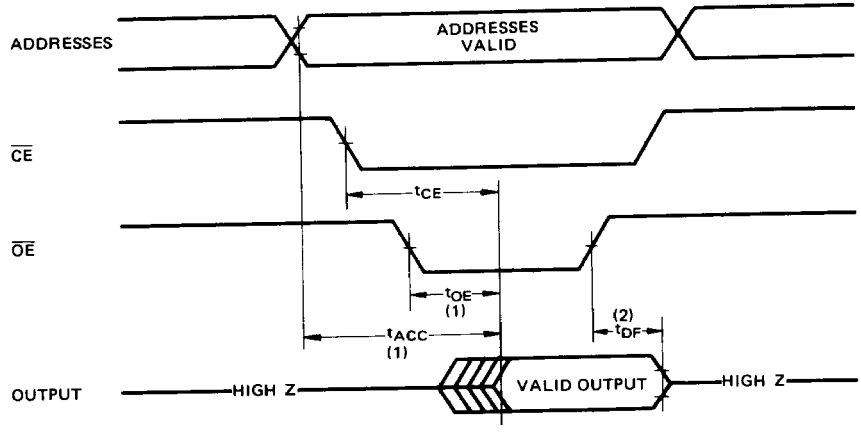


AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM2732-35			MBM2732-45			Unit
		Min	Typ	Max	Min	Typ	Max	
Address to Output Delay	t_{ACC}	—	—	350	—	—	450	ns
Chip Enable to Output Delay	t_{CE}	—	—	350	—	—	450	ns
Output Enable to Output Delay	t_{OE}	—	—	120	—	—	120	ns
Address to Output Hold	t_{OH}	0	—	—	0	—	—	ns
Output Enable High to Output Float	t_{DF}	0	—	100	0	—	100	ns

READ OPERATION TIMING DIAGRAM



Note: (1) $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

(2) t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

PROGRAMMING / ERASING INFORMATION

Memory Cell Description

The MBM2732 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 14). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 15). In the initial state the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 15.

Fig. 14 — MEMORY CELL

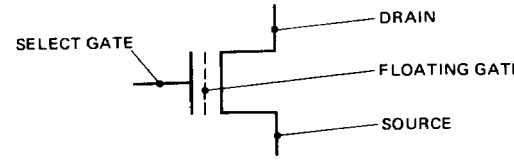
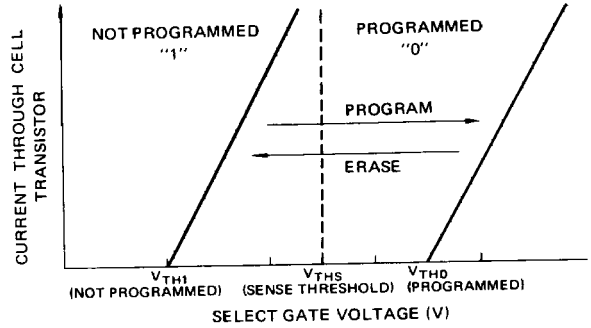


Fig. 15 — MEMORY CELL THRESHOLD SHIFT



Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM2732 has all 32,768 bits in the "1", or high state. "0's" are loaded into the MBM2732 through the procedure of programming.

The programming mode is entered when +25V is applied to the $\overline{OE}/V_{PP}$ pin. A 0.1μF capacitor between $\overline{OE}/V_{PP}$ and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL low-level pulse is applied to the $\overline{CE}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied for each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{CE}$ input is prohibited when programming.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 2732 to an ultraviolet light source. A dosage of 15 W-second/cm² is required to completely erase an MBM2732. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm² for 15 to 20 minutes. The MBM2732 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM2732 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM2732, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

NOT RECOMMENDED FOR NEW DESIGNS. SEE PART NUMBER MBM2732A.

PROGRAMMING / ERASING INFORMATION (continued)

DC Characteristics

(T_A = 25°C, V_{CC}(1) = 5V ±5%, V_{PP}(1,2) = 25V ± 1V, V_{SS} = GND

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}	—	—	10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = V_{IL}, $\overline{OE}/V_{PP}$ = V_{PP})	I_{PP}	—	—	30	mA
V_{CC} Supply Current	I_{CC2}	—	—	150	mA
Input Low Level	V_{IL}	−0.1	—	0.8	V
Input High Level	V_{IH}	2.0	—	V_{CC} +1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage During Verify (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

Note: (1) V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

(2) V_{PP} must not be greater than 26 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket when V_{PP} = 25 volts. Also, during $\overline{CE}$ = V_{IL}, V_{PP} must not be switched from V_{IL} to 25 volts or vise-versa.

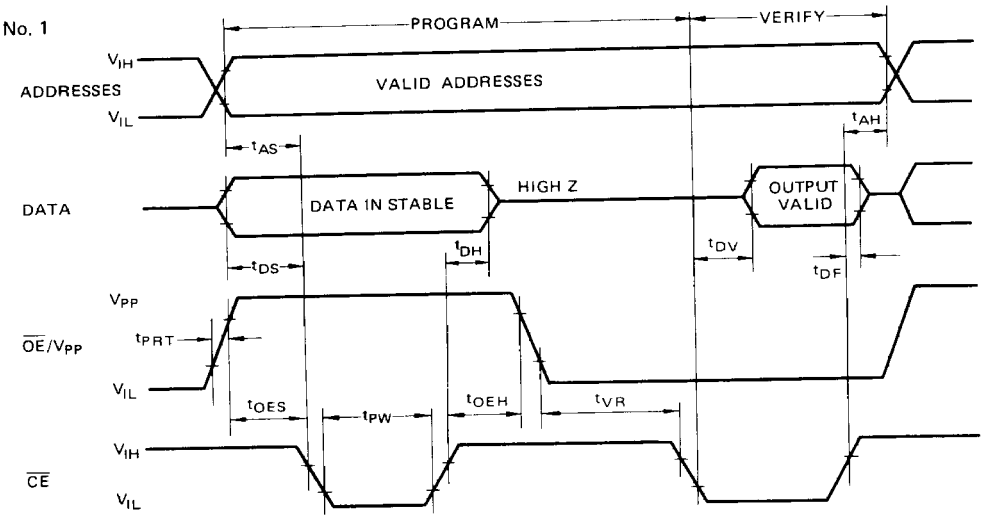
AC Characteristics

(T_A = 25°C)

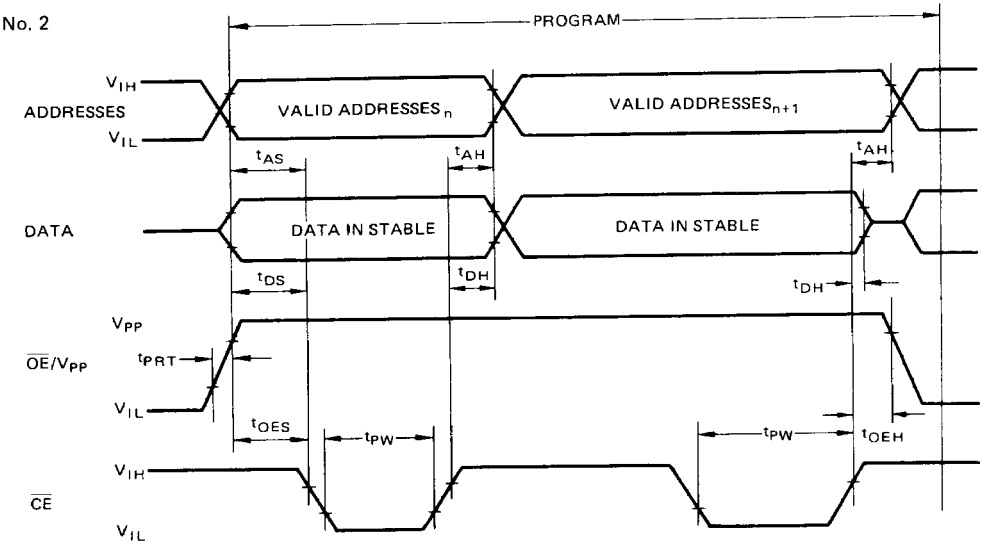
Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2	—	—	μs
Output Enable Setup Time	t_{OES}	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
Address Hold Time	t_{AH}	0	—	—	μs
Output Enable Hold Time	t_{OEH}	2	—	—	μs
Data Hold Time	t_{DH}	2	—	—	μs
Chip Enable to Output Float Delay ($\overline{OE}$ = V_{IL})	t_{DF}	0	—	120	ns
Chip Enable to Data Valid Time ($\overline{CE}$ = V_{IL}, $\overline{OE}/V_{PP}$ = V_{IL})	t_{DV}	—	—	1	μs
Program Pulse Width	t_{PW}	45	50	55	ms
Program Pulse Rise Time	t_{PRT}	50	—	—	ns
V_{PP} Recovery Time	t_{VR}	2	—	—	μs

PROGRAMMING WAVEFORMS

No. 1



No. 2



Note: In PROGRAMMING WAVEFORMS No. 2, Address Hold Time t_{AH} must be more than 2 μs.