MOS Memories

FUJITSU

MBM27256-20-X, MBM27256-25-X, MBM27256-30-X, MBM27256-30-W

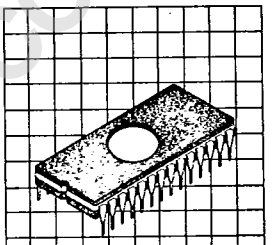
MOS 262,144-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

The Fujitsu MBM27256-X and MBM27256-W are high speed 262,144-bit static NMOS erasable and electrically reprogrammable read only memories. It is especially well suited for applications where rapid turnaround and/or bit pattern experimentation are important.

A 28-pin Dual-In-Line package with a transparent lid is used to package the MBM27256-X and MBM27256-W. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27256-X and MBM27256-W are fabricated using NMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package
DIP-28C-C01

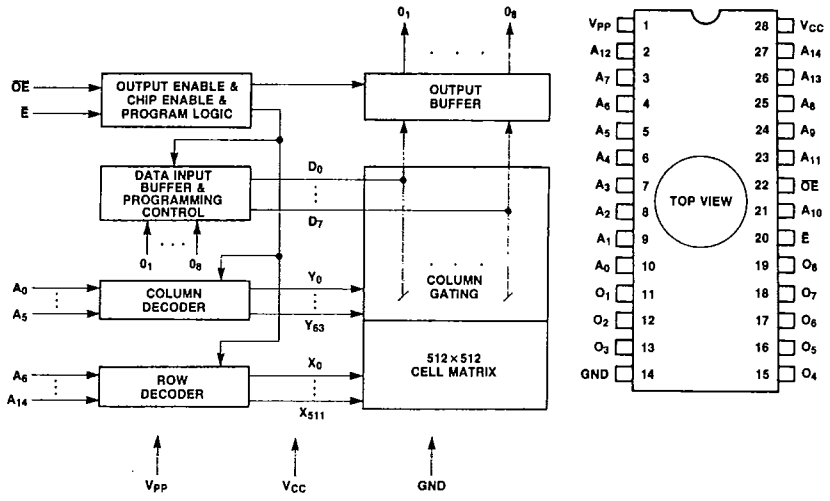
Features

- 32,768 words × 8-bit organization, fully decoded
- Single location programming
- Programmable utilizing the faster programming algorithm
- Program voltage: 12.5V
- Low power requirement
  MBM27256-X active: 630 mW
  MBM27256-W active: 650 mW
  Standby: 237 mW
- No clocks required (fully static operation)
- Fast access time:
  200 ns max. (MBM27256-20-X)
  250 ns max. (MBM27256-25-X)
  300 ns max. (MBM27256-30-X)
  300 ns max. (MBM27256-30-W)
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Single +5V supply, ±5% tolerance
- Standard 28-pin DIP package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MBM27256-20-X
MBM27256-25-X
MBM27256-30-X
MBM27256-30-W

MBM27256 Block Diagram and Pin Assignment



Absolute Maximum Ratings
(see Note)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	−65 to +135* −50 to +95	°C
Storage Temperature	T_{STG}	−65 to +150* −65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
Voltage on A_9 with Respect to GND	V_{A9}	−0.6 to +13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	−0.6 to +14	V
Supply Voltage with Respect to GND	V_{CC}	−0.6 to +7	V

Note: *MBM27256-W

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Functions and Pin Connections

	Function (Pin No.)						
Mode	Address Input (2 ~ 10, 21, 23 ~ 27)	Data I/O (11 ~ 13, 15 ~ 19)	$\overline{E}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	OUT	V_{IL}	V_{IL}	+5 V	+5 V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	+5 V	+5 V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	+5 V	+5 V	GND
Program	A_{IN}	IN	V_{IL}	V_{IH}	+6 V	+12.5 V	GND
Program Verify	A_{IN}	OUT	Don't Care	V_{IL}	+6 V	+12.5 V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	V_{IH}	+6 V	+12.5 V	GND

MBM27256-20-X
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MBM27256-30-W

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

Recommended Operating Conditions
(Reference to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*1	V_{CC}	4.75	5.0	5.25	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} −0.6		V_{CC} +0.6	V
Input High Voltage	V_{IH}	2.0		V_{CC} +1	V
Input Low Voltage	V_{IL}	−0.1		0.8	V
Operating Temperature	T_A	−40 −55*2		+85 +125*2	°C

Notes: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.
*2 MBM27256-30-W

DC Characteristics
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.25V)	I_{LO}			10	μA
V_{CC} Standby Current ($\overline{E}$ = V_{IH})	I_{CC1}			45	mA
V_{CC} Active Current ($\overline{E}$ = V_{IL})	I_{CC2}			120	mA
V_{PP} Supply Current (V_{PP} = V_{CC} ± 0.6V)	I_{PP1}			5	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4			V

AC Characteristics
(Recommended operating conditions unless otherwise noted)

		MBM27256-20-X			MBM27256-25-X			MBM27256-30-X MBM27256-30-W			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Address Access Time*1 ($\overline{E}$ = $\overline{OE}$ = V_{IL})	t_{ACC}			200			250			300	ns
$\overline{E}$ to Output Delay ($\overline{OE}$ = V_{IL})	t_E			200			250			300	ns
$\overline{OE}$ to Output Delay*1 ($\overline{E}$ = V_{IL})	t_{OE}			75			100			120	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		105	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{E}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{E}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

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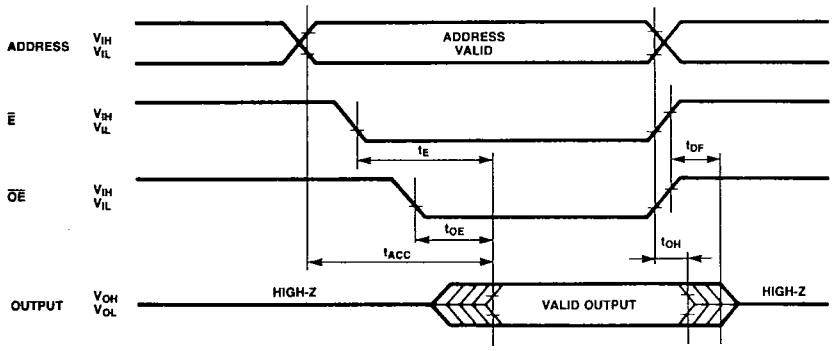
MBM27256-30-W

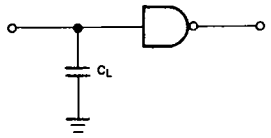
Operation Timing Diagram



AC Test Conditions

(including programming)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



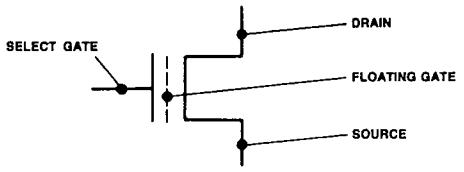
MBM27256-20-X
MBM27256-25-X
MBM27256-30-X
MBM27256-30-W

Programming/ Erasing Information

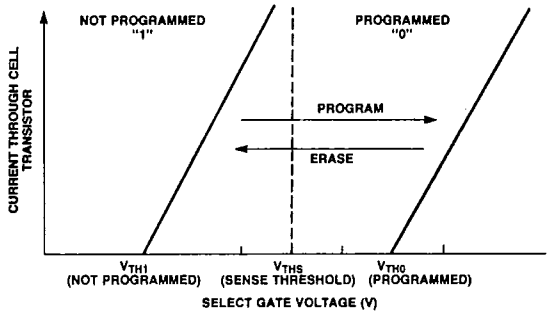
Memory Cell Description

The MBM27256 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Memory Cell diagram). The top gate is connected to the row decorder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Memory Cell Threshold Shift). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate. Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in the Memory Cell Threshold Shift Diagram.

Memory Cell



Memory Cell Threshold Shift



Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27256 has all 262,144-bits in the "1", or high state. "0's" are loaded into the MBM27256 through the procedure of programming.

The MBM27256 is programmed with a fast programming algorithm called QuickPro™ designed by Fujitsu. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{E}$ and $\overline{OE}$ are V_{IH}. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The eight bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 ms programming pulse is applied to $\overline{E}$ and after that one additional pulse, which is 3 times as wide as previous pulse, is applied to $\overline{E}$ to accomplish the programming.

Procedure of QuickPro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{E}$ = V_{IH}.
3) Clear the programming pulse counter (X←0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1 ms Typ.) to $\overline{E}$.
6) Increment the counter (X←X + 1).
7) Compare the number (= X) of applied programming pulse with 25 and then verify the programmed data: If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X = 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{E}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G←G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify all programmed data: If the verification succeeds, the programming completes. If any programmed data is not the same as input data, the device fails.

A continuous TTL low level should not apply to $\overline{E}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

MBM27256-20-X
MBM27256-25-X
MBM27256-30-X
MBM27256-30-W

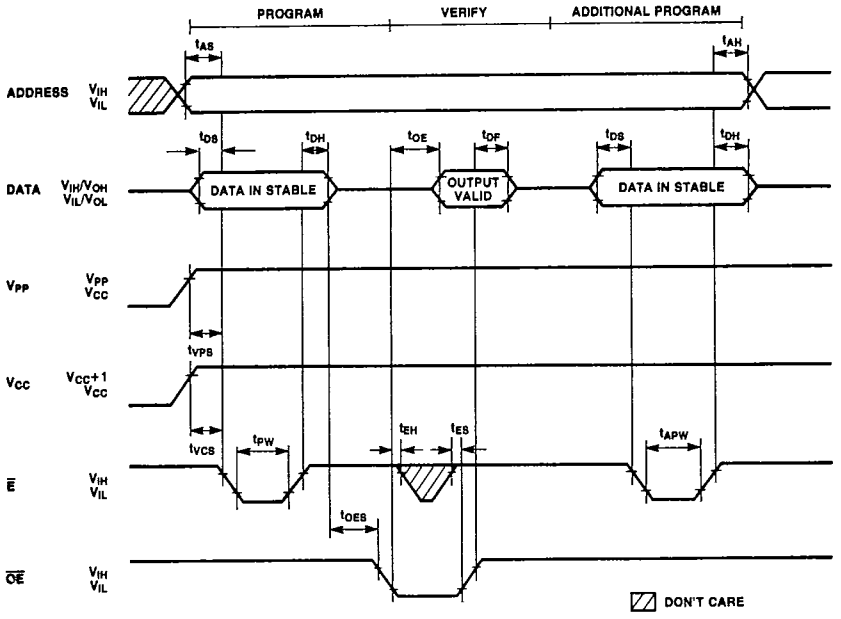
Programming/Erasing Information (Continued)

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27256 to an ultraviolet light source. A dosage of 15 W-seconds/cm² is required to completely erase an MBM27256. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm² for 15 to 20 minutes. The MBM27256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27256 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM27256, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Programming Waveform



MBM27256-20-X
MBM27256-25-X
MBM27256-30-X
MBM27256-30-W

DC Characteristics

(T_A = 25±5°C, V_{CC} *1 = 6V±0.25V, V_{PP} *2 = 12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{IL}			10	μA
V_{PP} Supply Current ($\overline{E}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{OE}$ = V_{IL})	I_{PP3}			5	mA
V_{CC} Supply Current	I_{CC}			100	mA
Input Low Level	V_{IL}	−0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OL} = −400μA)	V_{OH}	2.4			V

Notes: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out of or put into a socket with V_{PP} = 12.5 volts. Also, during E = V_{IL}, V_{PP} must not be switched from 5 to 12.5 volts or vice-versa.

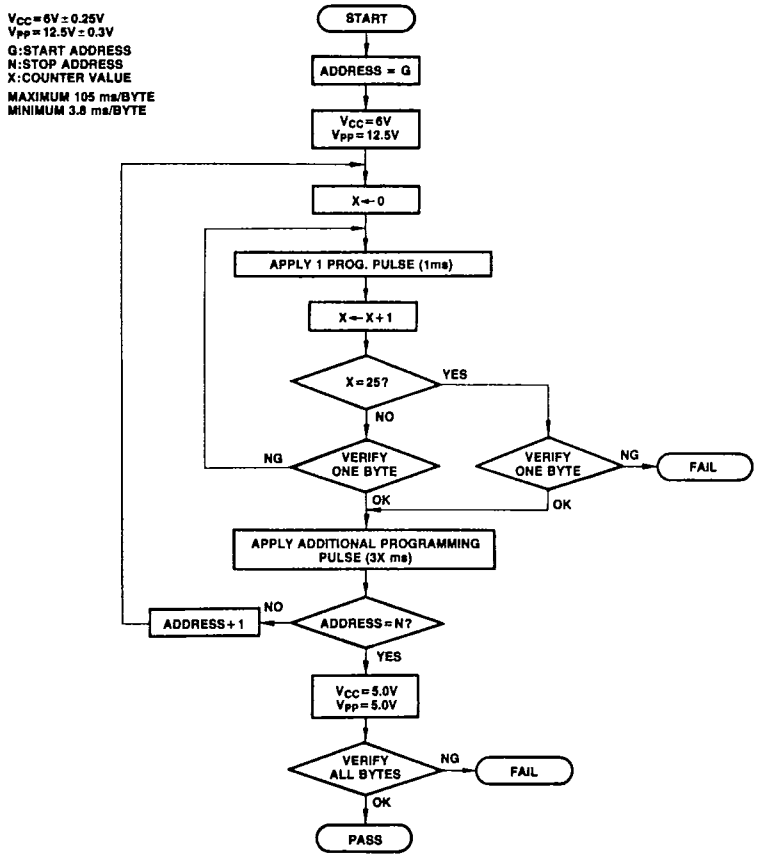
AC Characteristics

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Chip Enable Setup Time	t_{ES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VPS}	2			μs
V_{CC} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Chip Enable Hold Time	t_{EH}	2			μs
Output Enable to Output Valid	t_{OE}			120	ns
Output Disable to Output Float Delay	t_{DF}			105	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Programming Pulse Number		1		20	times
Additional Programming Pulse Width	t_{APW}	2.85		63	ms

Programming/Erasing Information
(Continued)

Programming Flow Chart



MBM27256-20-X
MBM27256-25-X
MBM27256-30-X
MBM27256-30-W

Package Dimensions

Dimensions in inches (millimeters)

28-Lead Ceramic (CERDIP with Transparent Lid) Dual In-Line Package (Case No.: DIP-28C-C01)