Technical Product Brief

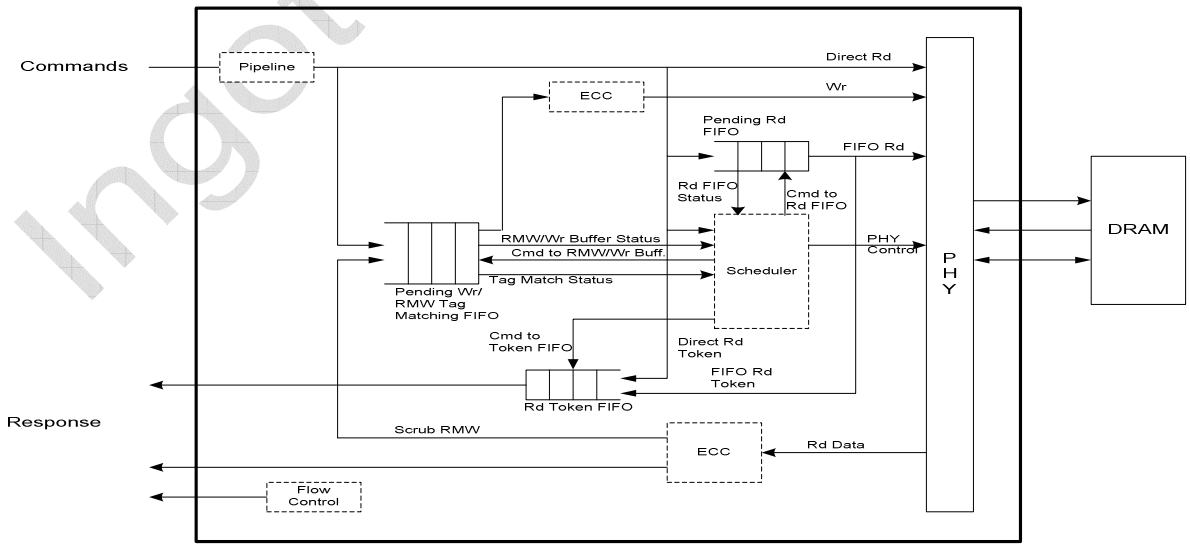
IP4001 DDR1/DDR2
DRAM Intelligent Memory Manager

Ingot Systems, via a proprietary approach we call Electronic Design Solutions (EDS) technology, can create a customized Intellectual Property (IP) Core tailored for a specific application. An EDS is the embodiment of our years of experience creating systems and integrated circuit designs for our customers. It is a world class design environment that makes it easy for us to create custom-tailored ASIC/SoC and FPGA IP Cores for target applications. The Intelligent Memory Manager is just one of the advanced IP Cores we can create using our EDS technology.

The IP4001 DDR1/DDR2 DRAM Intelligent Memory Manager is a flexible and advanced solution for ASIC/SoC and FPGA designers who need to get the ultimate performance out of their memory interface using the least amount of silicon area. Much more than a standard memory controller, our Intelligent Memory manager provides a library of features and functions we can select from and customize to squeeze the most bandwidth out of any DDR1/DDR2 DRAM in your system. We have an in depth understanding of the way memory is used at the system level so we can better construct an optimal solution to specific application needs. Engineering development support is included with the purchase of any Ingot IP Core to make sure we tailor your solution for a 'seamless fit'. This technical product brief will describe the list of library functions available in the Intelligent Memory Manger- the ones we will typically select from when constructing you specific solution. A companion document, our Intelligent Memory Manager solutions guide, gives some example solutions for several different system applications. Review that document for more details on some typical customization options available with our Intelligent Memory Manager.

Intelligent Memory Manager Features

The Ingot Intelligent Memory Manager (IMM) is designed to provide ultra-low latencies while delivering the highest possible performance. The IMM is designed with high frequency operation in mind and can support 400MHz clock speeds (800 Mbps) in 90nm and 0.13um process. The IMM implements advanced scheduling algorithms to optimize access to the DRAM, sophisticated request merging and bypass optimizations for high performance, and multiple priorities to differentiate between critical and non-critical accesses.



IP4001 DDR1/DDR2 Intelligent Memory Manager

The IMM is well suited for use in mission critical applications. It is available with a variety of ECC functions for various DRAM bus widths, and with an optional fault tolerance feature can withstand the failure of an entire DRAM device. For increased pin efficiency the core supports partial-burst transactions in DDR2 using inline RMW operations, avoiding the need for data mask pins.

An extensive list of features of the Intelligent Memory Manager is given below. Virtually all of these features can be customized (included, excluded or modified) for a specific application in order to provide the best 'fit' for a specific application. Ingot's proprietary EDS technology gives us a level of flexibility previously unavailable from IP Core vendors.

Features

- Complete DDR1 and DDR2 support
- Fully digital design for the entire controller including the "DRAM PHY"
- 400MHz clock speed (800 Mbps/pin data rate) in 90nm and 0.13um process.
- Ultra-low latency for read to open page
- Support for out of order read request fulfillment
- Support for delayed writes
- Support for write combining
- Support for scheduler bypass for lowest possible latency
- Support for efficient partial burst transactions in DDR2
- Ability to service read requests from store of pending write transactions
- Full OCD support
- Software override for DRAM initialization and programming
- Fully programmable DRAM parameters
- Sophisticated PHY with standard cell based DLL
- Clean partitioning between scheduler and PHY allowing use of third party or customer's PHY
- Multiple priorities
- ECC support with automatic scrubbing.
- X32, x40, x64, x72, and x80 DIMM support
- Support for tolerating full DRAM chip failure
- Support for automatic DRAM power down and self refresh during idle
- Optional support for RDQS for deep rank configurations
- Core available as-is or customized to your requirement using Ingot's design services

Physical Characteristics

- 100K gates + memory for the high performance version
- Fully synchronous 400MHz design
- PHY Available in both the simple 1X and the high performance 2X clocking versions.
- Fully digital DLL for locking to DQS

Deliverables

- Verilog netlist
- Encrypted verilog simulation models
- Full controller specification documentation
- Complete testbench with coverage points
- Testplan and testbench documentation
- DRAM protocol checkers
- Primetime timing scripts
- Support for spice simulation of I/O's
- Backend support for PHY layout

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