ESDA14V2-1BF3

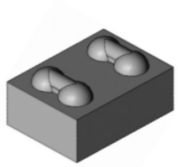
Single-line bidirectional Transil™ array for ESD protection

Features

- ESD Protection: IEC61000-4-2 level 4
- Low leakage current
- Very small PCB area < 0.4 mm²
- 400 micron pitch

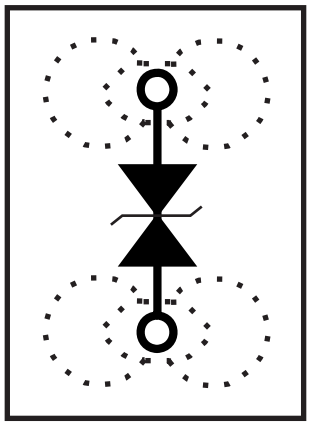
Complies with the following standards

- IEC61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)



Flip Chip
(2 bumps)

Figure 1. Schematic diagram (top view)



Applications

Where transient overvoltage protection of ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communications systems and cellular phones
- Video equipment

Description

The ESDA14V2-1BF3 is a monolithic bidirectional diode designed to protect 1 line against ESD transients.

The device is ideally suited for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage: IEC61000-4-2 air discharge IEC61000-4-2 contact discharge		 ±15 ±8	kV
P_{PP}	Peak pulse power dissipation (8/20 µs) (1)	$T_{j\ initial} = T_{amb}$	50	W
T_j	Junction temperature		125	°C
T_{stg}	Storage temperature range		- 55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C
T_{op}	Operating junction temperature range		-40 to +125	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Figure 2. Electrical characteristics (definitions)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current @ V_{RM}
R_D	Dynamic resistance
αT	Voltage - temperature coefficient
C_{line}	Line capacitance

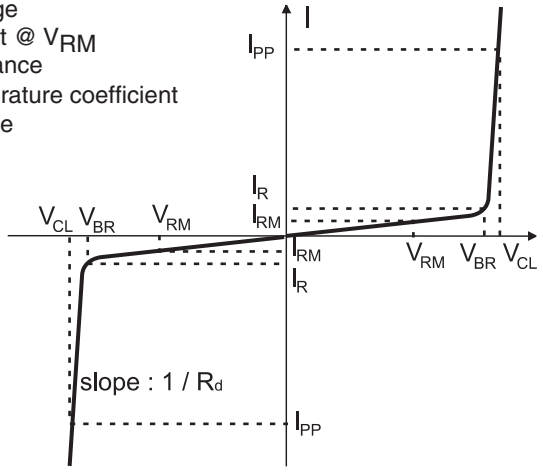


Table 2. Electrical characteristics (values, T_{amb} = 25 °C)

Symbol	Test condition	Min.	Typ.	Max	Unit
V_{BR}	I_R = 1 mA	14.2	-	18.0	V
I_{RM}	V_{RM} = 12 V	-	-	0.5	µA
	V_{RM} = 3 V	-	-	0.1	
R_d	Square pulse, I_{PP} = 3 A t_p = 2.5 µs	-	2.2	-	Ω
αT	$\Delta V_{BR} = \alpha T(T_{amb}$ - 25 °C) x V_{BR} (25 °C)	-	-	6.5	10^{-4}/°C
C_{line}	V_R = 0 V, F = 1 MHz, V_{osc} = 30 mV	-	10	-	pF

Figure 3. Relative variation of peak pulse power versus initial junction temperature

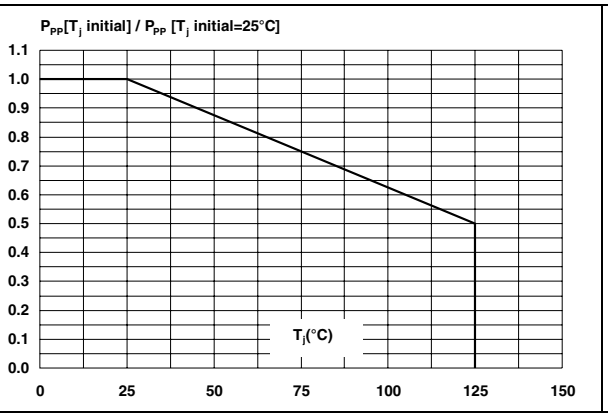


Figure 4. Peak pulse power versus exponential pulse duration

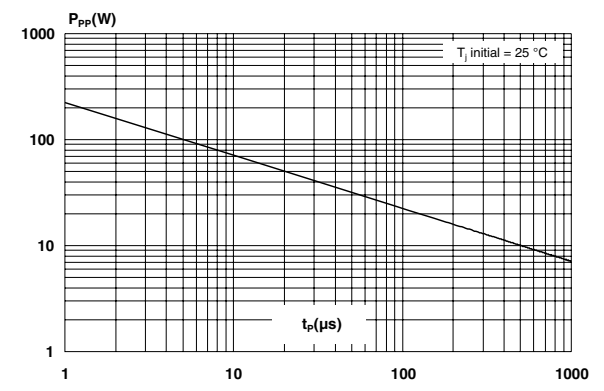


Figure 5. Clamping voltage versus peak pulse current (square pulse, typical values)

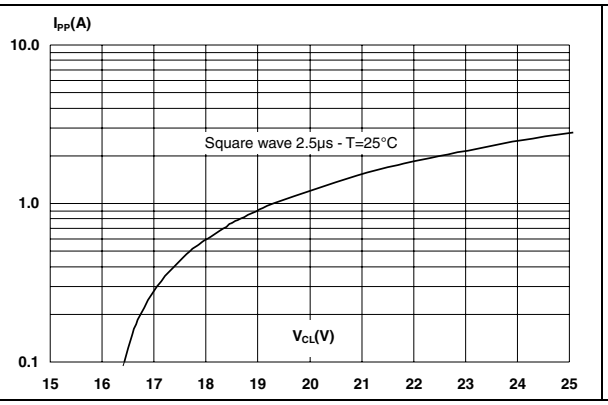


Figure 6. Junction capacitance versus reverse applied voltage (typical values)

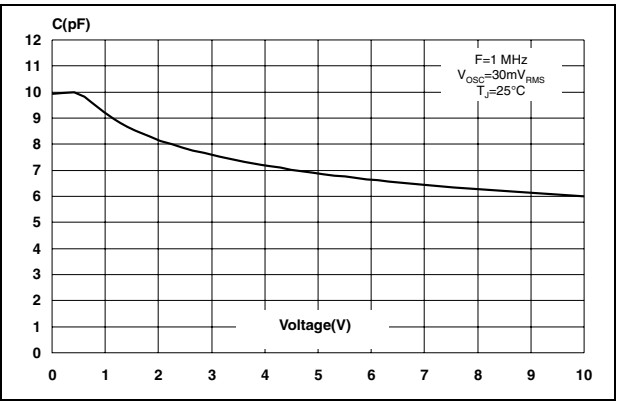


Figure 7. Relative variation of leakage current versus junction temperature (typical values)

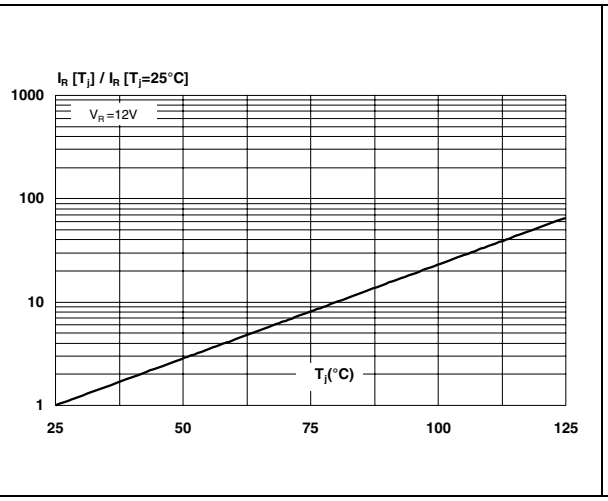


Figure 8. S21 attenuation measurements

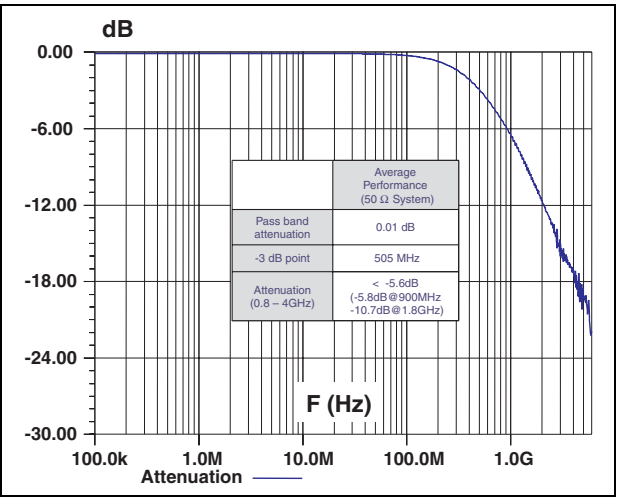


Figure 9. ESD response to IEC61000-4-2 (+15 kV air discharge)

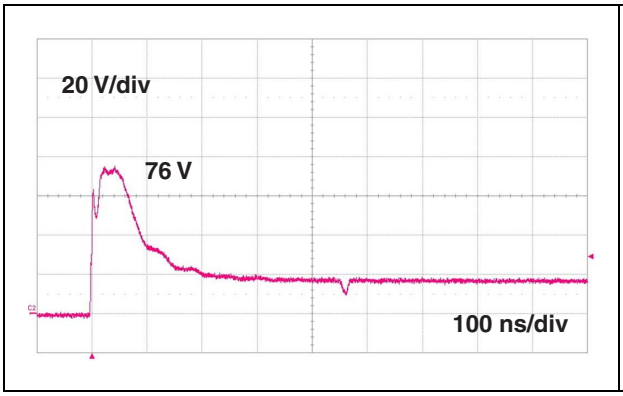
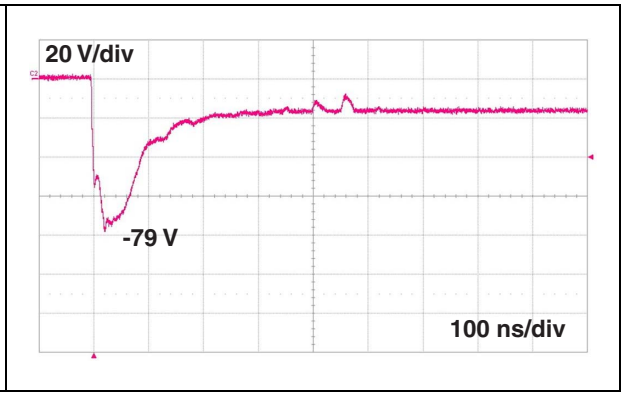
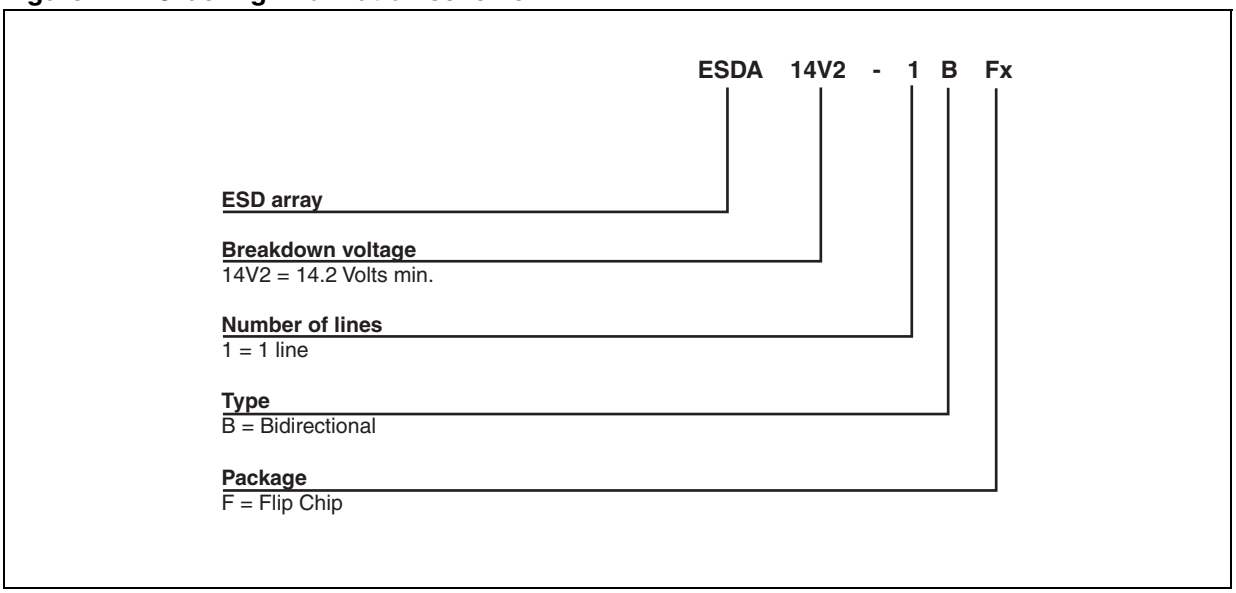


Figure 10. ESD response to IEC61000-4-2 (-15 kV air discharge)



2 Ordering information scheme

Figure 11. Ordering information scheme



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 12. Package dimensions

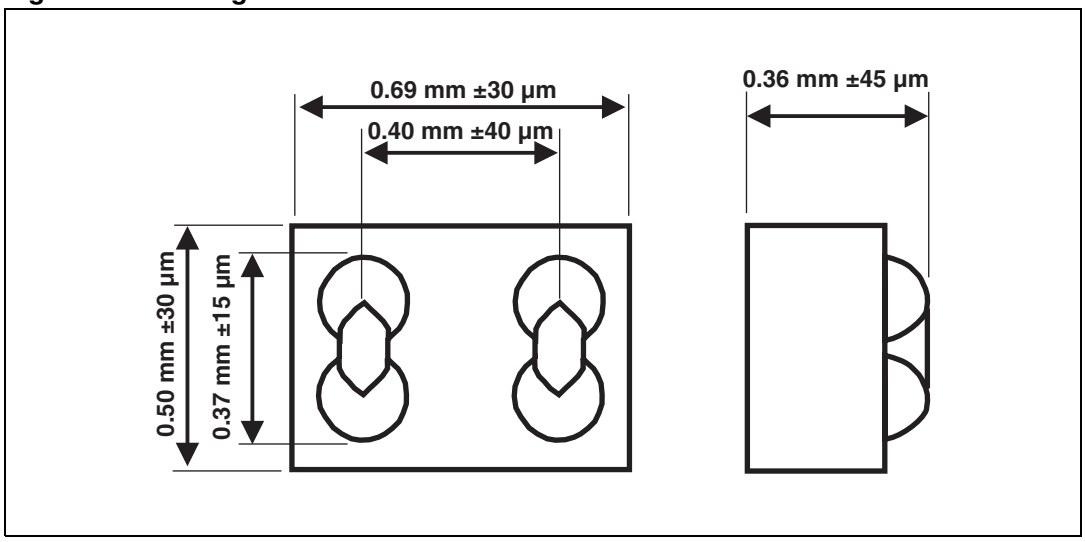
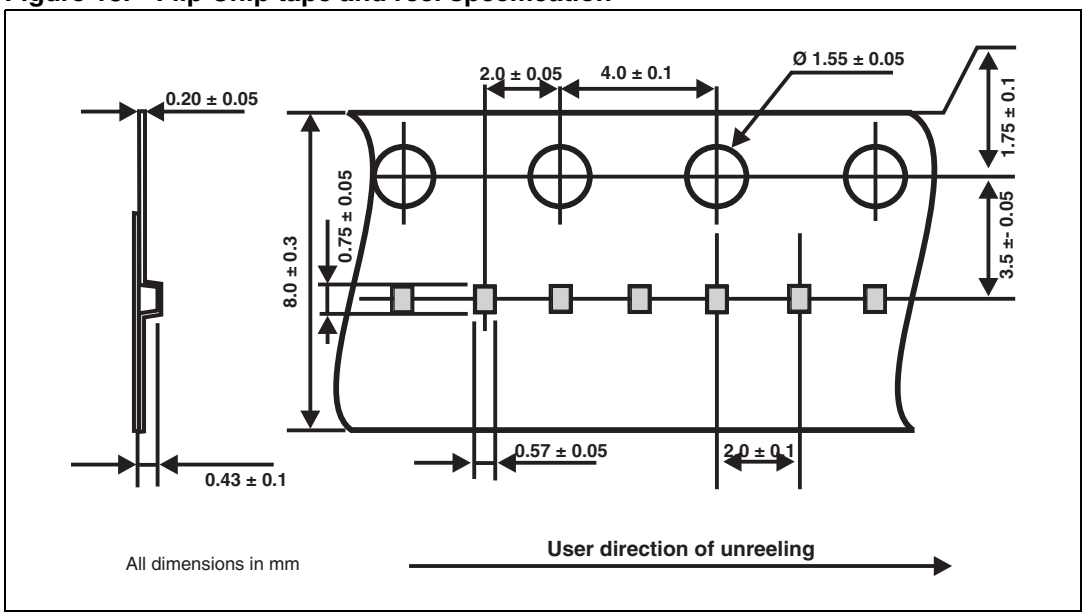


Figure 13. Flip Chip tape and reel specification



4 PCB recommendations

4.1 Design

For optimum electrical performance and highly reliable solder joints, STMicroelectronics recommends the PCB design recommendations listed in *Table 3*.

Table 3. PCB design recommendations for solder bar pitch 400 µm

For NSMD PCB non solder mask defined	Oblong pad: 370 x 180 µm – Micro via SSBU allowed – Micro via SBU to be avoided – Micro via SBU filled (under qualification)
	Track: – Only one track per pad – Maximum track width = 100 µm Track layout must be symmetrical to the die axis (to homogenize stress and welding attraction during reflow assembly)
For SMD PCB solder mask defined	Oblong pad: – Micro via SSBU allowed – Micro via SBU to be avoided – Micro via SBU filled (under qualification)
PCB Pad Finishing	Cu – Ni (2-6 µm) - Au (0.2 µm max)

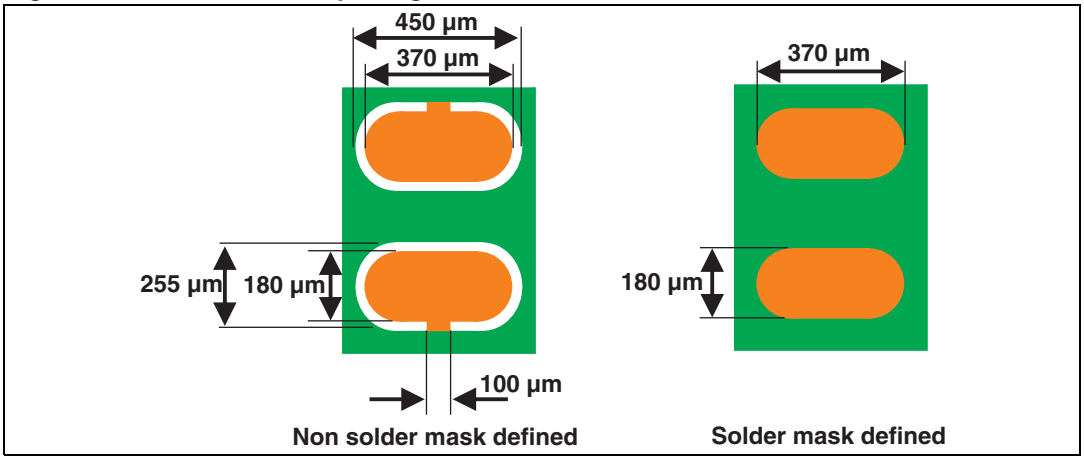
Note: A gold layer finishing on the PCB pad that is too thick (0.2 µm maximum) is not recommended (low joint reliability).

To optimize the natural self centering effect of CSP on the PCB, PCB pad positioning and size have to be properly designed (see *Figure 14*)

Micro vias

An alternative to routing on the top surface is to route out on buried layers. To achieve this, the pads are connected to the lower layers using micro vias. Only SSBU via technology is approved.

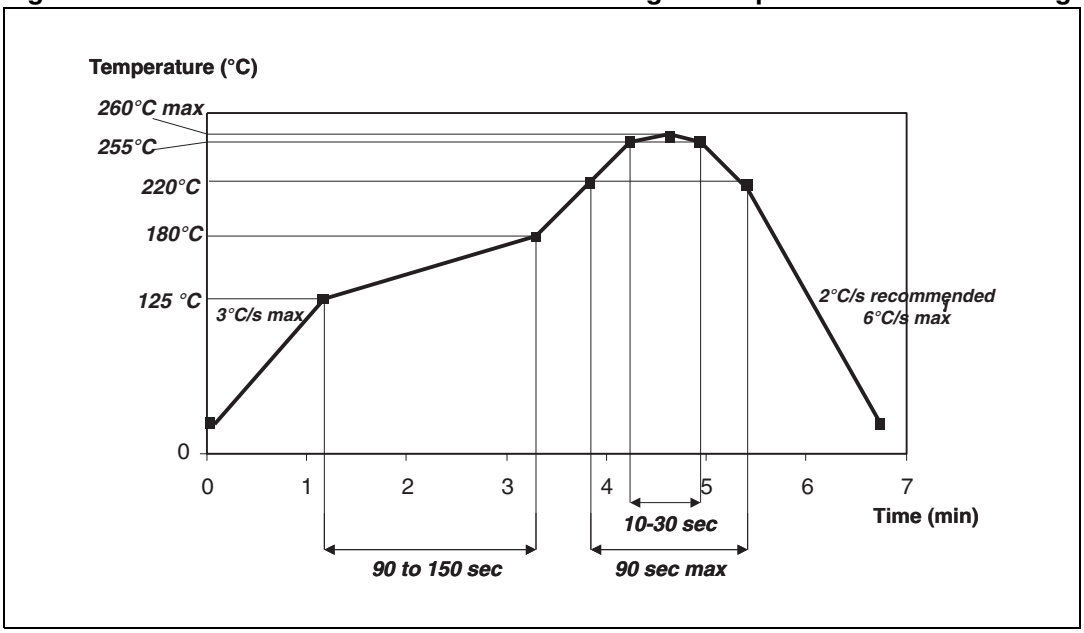
Figure 14. Solder mask opening



4.2 Assembly

For chip scale package mounting on the PCB, STMicroelectronics recommends the use of a solder stencil aperture of 330 x 330 µm² maximum and a typical stencil thickness of 75 or 80 µm. Chip scale packages are fully compatible with the use of near eutectic 95.5 Sn, 4 Ag, 0.5 Cu solder paste with no-clean flux. ST's recommendations for chip scale package board mounting are illustrated on the soldering reflow profile shown in *Figure 15*.

Figure 15. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Dwell time in the soldering zone (with temperature higher than 220 °C) has to be kept as short as possible to prevent component and substrate damages. Peak temperature must not exceed 260 °C. Controlled atmosphere (N2 or N2H2) is recommended during the whole reflow, especially above 150 °C.

Chip scale packages are able to withstand three times the previous recommended reflow profile in order to be compatible with a double reflow when SMDs are mounted on both sides of the PCB and one additional repair.

A maximum of three soldering reflows are allowed for these lead-free packages (with repair step included).

The use of a no-clean flux is highly recommended to avoid any cleaning operation. To prevent any bump cracks, ultrasonic cleaning methods are not recommended.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDA14V2-1BF3	None	Flip Chip	0.37 mg	15 000	Tape and reel 7”

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
25-Jun-2009	1	Initial release.

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