ESDAxxSC5
ESDAxxSC6

Application Specific Discretes
A.S.D.

QUAD TRANSIL ARRAY FOR ESD PROTECTION

APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

-COMPUTERS

- PRINTERS
- COMMUNICATION SYSTEMS
- GSM HANDSETS AND ACCESSORIES
- OTHER TELEPHONE SET

FEATURES

- 4 UNIDIRECTIONAL TRANSIL FUNCTIONS
- LOW LEAKAGE CURRENT: I_R max. < 20 µA at V_{BR}
- 500 W PEAK PULSE POWER (8/20 µs)

DESCRIPTION

The ESDAxxSC5 and ESDAxxSC6 are monolithic voltage suppressors designed to protect components which are connected to data and transmission lines against ESD.

They clamp the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transient.

BENEFITS

High ESD protection level : up to 25 kV

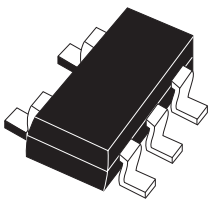
High integration

Suitable for high density boards

COMPLIES WITH THE FOLLOWING STANDARDS:

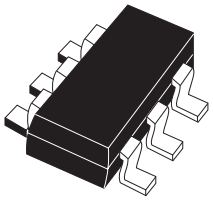
IEC61000-4-2 : level 4

MIL STD 883C-Method 3015-6 : class3
(human body model)



SOT23-5L (SC-59)

ESDAxxSC5

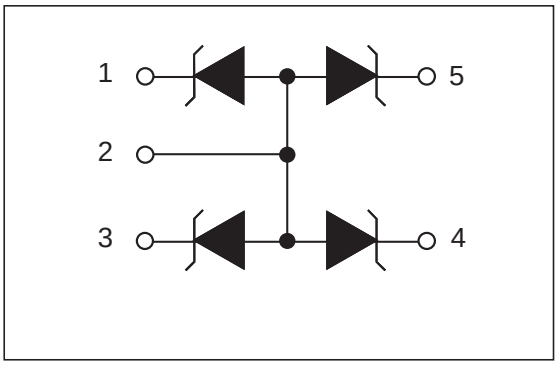


SOT23-6L (SC-59)

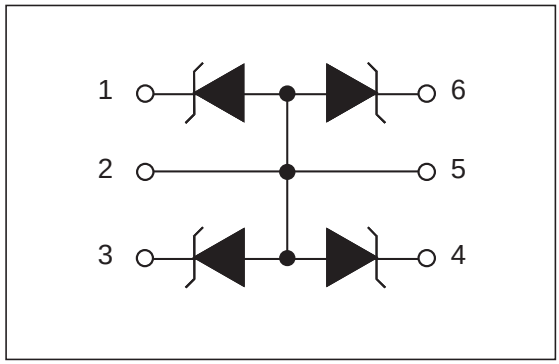
ESDAxxSC6

FUNCTIONAL DIAGRAM

SOT23-5L



SOT23-6L



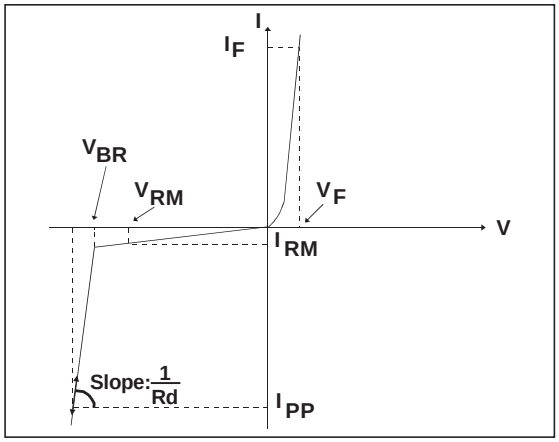
ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Symbol	Test conditions	Value	Unit
V_{PP}	ESD discharge - MIL STD 883C - Method 3015-6 IEC61000-4-2 air discharge IEC61000-4-2 contact discharge	25 16 9	kV
P_{PP}	Peak pulse power (8/20µs) note1	500	W
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature range	-55 to +150	°C
T_L	Lead solder temperature (10 second duration)	260	°C
T_{op}	Operating temperature range	-40 to +125	°C

note 1 : 300 W for ESDA14V2SC5 AND ESDA14V2SC6
note 2: Evolution of functional parameters is given by curves.

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Capacitance
Rd	Dynamic resistance
V_F	Forward voltage drop



Types	V_{BR} @ I_R			I_{RM} @ V_{RM}		Rd	αT	C	V_F @ I_F	
	min.	max.		max.		typ. note 1	max. note 2	typ. 0V bias	max.	
	V	V	mA	µA	V	mΩ	10^{-4}/°C	pF	V	mA
ESDA5V3SC5 ESDA5V3SC6	5.3	5.9	1	2	3	230	5	280	1.25	200
ESDA6V1SC5 ESDA6V1SC6	6.1	7.2	1	20	5.25	350	6	190	1.25	200
ESDA14V2SC5 ESDA14V2SC6	14.2	15.8	1	5	12	650	10	100	1.25	200
ESDA25SC6	25	30	1	1	24	1000	10	60	1.2	10

note 1 : Square pulse, Ipp = 15A, tp=2.5µs.
note 2 : $\Delta V_{BR} = \alpha T^* (Tamb - 25°C) * V_{BR} (25°C)$

CALCULATION OF THE CLAMPING VOLTAGE

USE OF THE DYNAMIC RESISTANCE

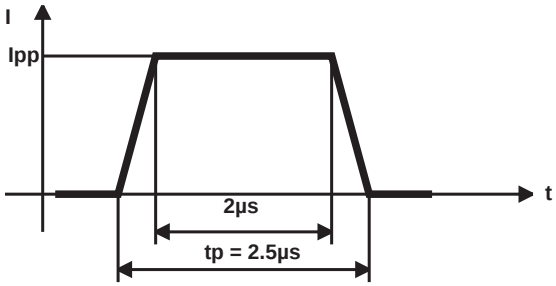
The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage V_{CL}. This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

$$V_{CL} = V_{BR} + Rd\ I_{PP}$$

Where Ipp is the peak current through the ESDA cell.

DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical 8/20µs and 10/1000µs surges.



2.5µs duration measurement wave.

As the value of the dynamic resistance remains stable for a surge duration lower than 20µs, the 2.5µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.

Fig. 1: Peak power dissipation versus initial junction temperature.

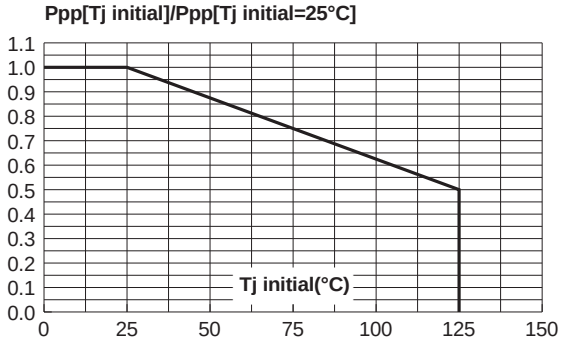


Fig. 2: Peak pulse power versus exponential pulse duration (Tj initial = 25 °C).

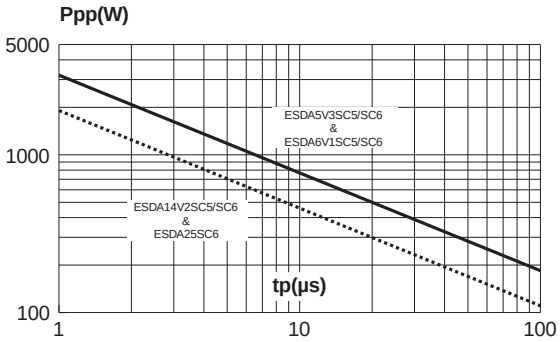


Fig. 3: Clamping voltage versus peak pulse current (Tj initial = 25 °C).
Rectangular waveform tp = 2.5 µs.

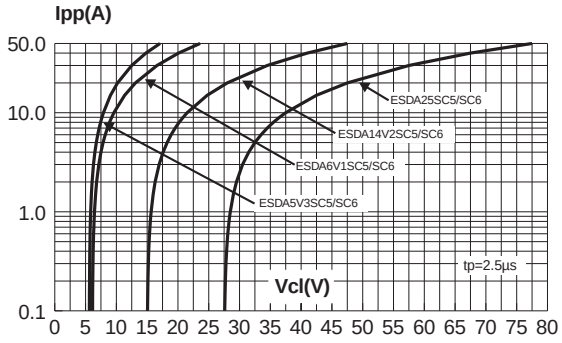


Fig. 4: Capacitance versus reverse applied voltage (typical values).

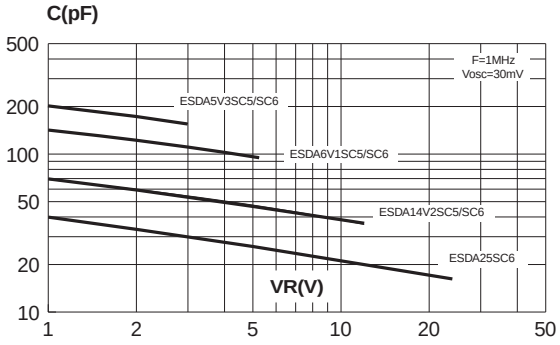


Fig. 5: Relative variation of leakage current versus junction temperature (typical values).

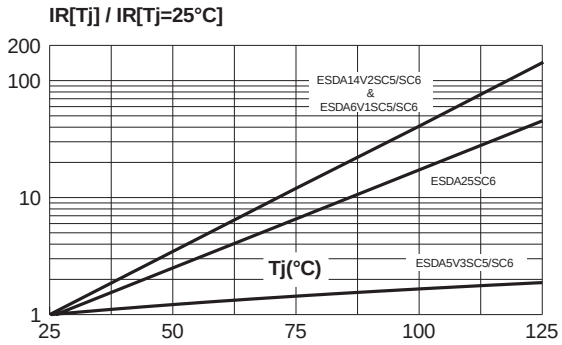
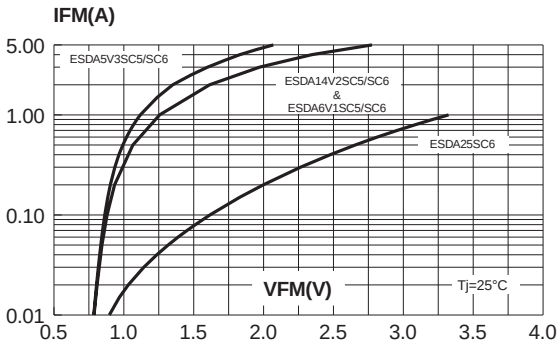


Fig. 6: Peak forward voltage drop versus peak forward current (typical values).



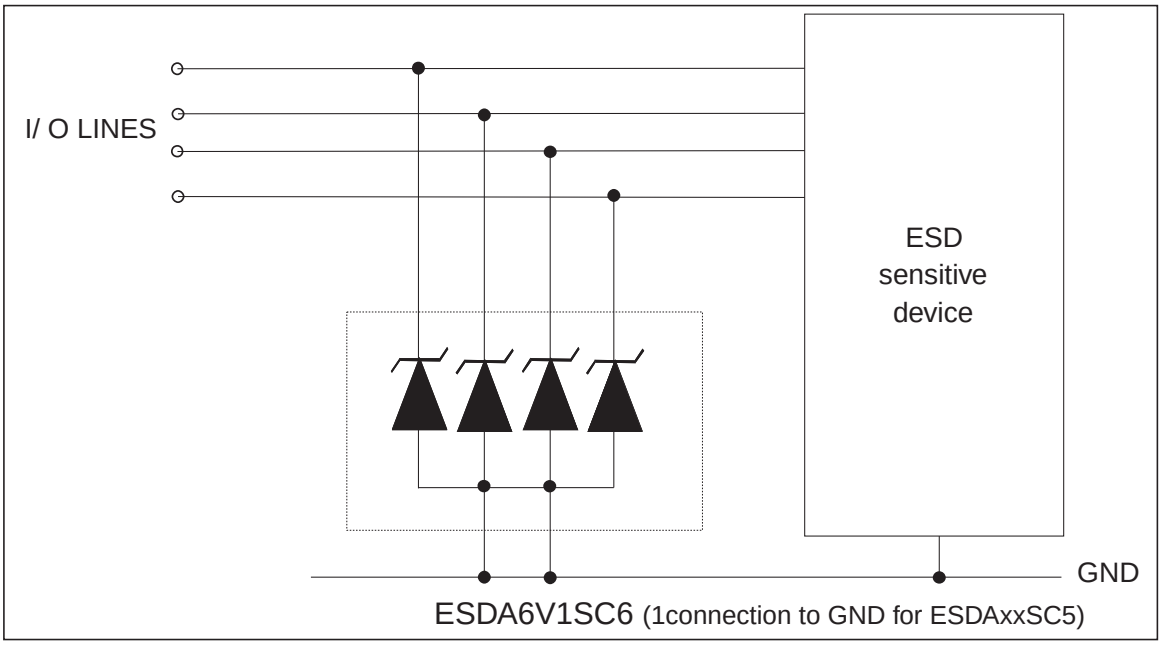
ESD protection by ESDAXXXSCX

Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

Transient Voltage Suppressors (TVS) are an ideal choice for ESD protection. They are capable of clamping the incoming transient overvoltage to a low enough level such that damage to the protected semiconductor is prevented.

Surface mount TVS arrays offer the best choice for minimal lead inductance.

They serve as parallel protection elements, connected between the signal line and ground. As the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the transient current to ground.



ESDA6V1SC6 (1connection to GND for ESDAxxSC5)

The ESDAxxSCx array is the ideal board level protection of ESD sensitive semiconductor components.

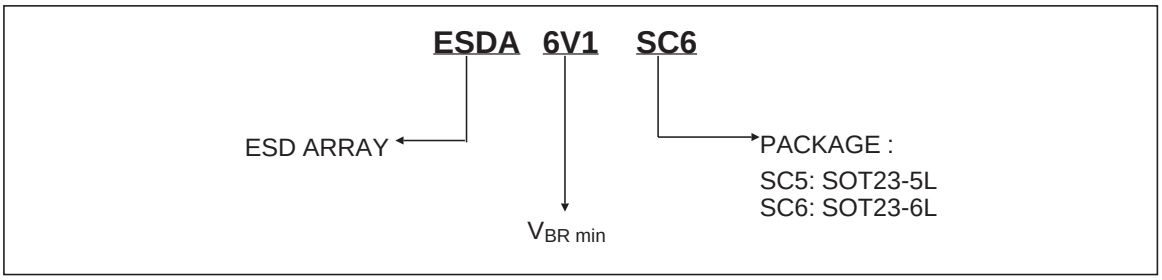
The tiny SOT23-5L and SOT23-6L packages allow design flexibility in the high density boards where the space saving is at a premium. This enables to shorten the routing and contributes to hardening against ESD.

ADVICE FOR OPTIMIZING CIRCUIT BOARD LAYOUT

Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended :

- The ESDAxxSC5/6 should be placed as close as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized
- All conductive loops, including power and ground loops should be minimized
- The ESD transient return path to ground should be kept as short as possible.
- Ground planes should be used whenever possible.

ORDER CODE



MARKING

Type	Marking
ESDA6V1SC5	EC61
ESDA6V1SC6	ES61
ESDA5V3SC5	EC53

Packaging: Standard packaging is tape and reel.

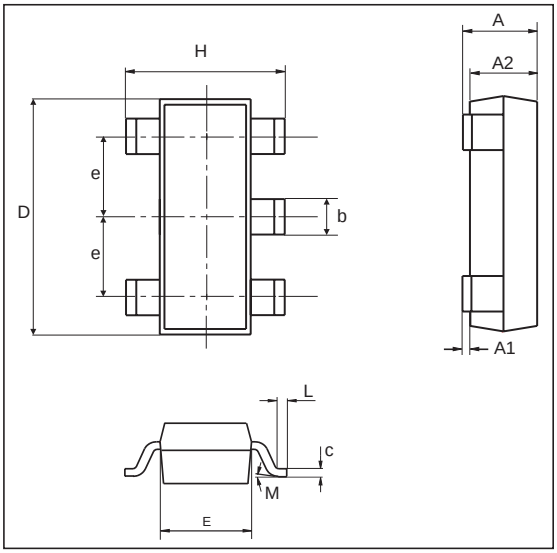
MARKING

Type	Marking
ESDA5V3SC6	ES53
ESDA14V2SC5	EC15
ESDA14V2SC6	ES15
ESDA25SC6	ES25

Packaging: Standard packaging is tape and reel.

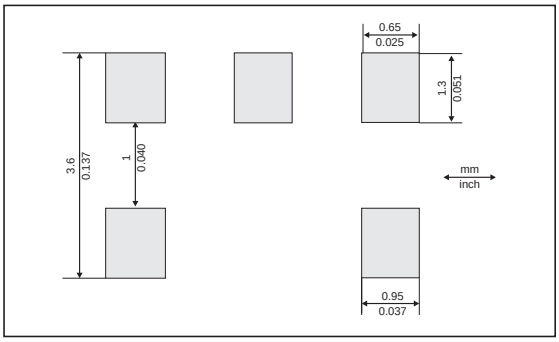
PACKAGE MECHANICAL DATA

SOT23-5L



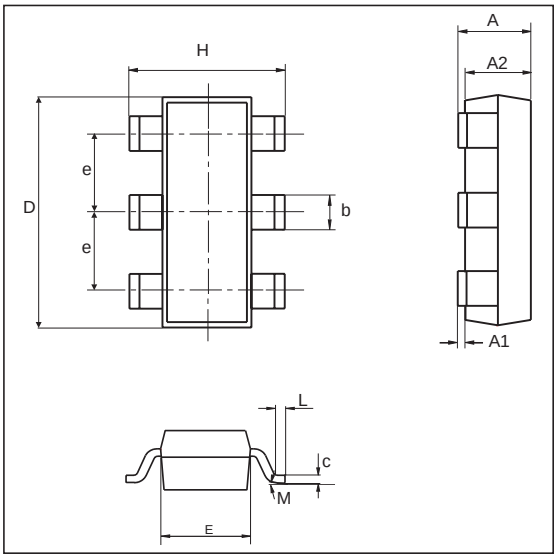
REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90		1.45	0.035		0.057
A1	0		0.15	0		0.006
A2	0.90		1.30	0.035		0.0512
b	0.35		0.50	0.0137		0.02
c	0.09		0.20	0.004		0.008
D	2.80		3.00	0.11		0.118
E	1.50		1.75	0.059		0.0689
e		0.95			0.0374	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
M			10°			10°

FOOT PRINT



PACKAGE MECHANICAL DATA

SOT23-6L



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A	0.90		1.45	0.035		0.057
A1	0		0.15	0		0.006
A2	0.90		1.30	0.035		0.0512
b	0.35		0.50	0.0137		0.02
C	0.09		0.20	0.004		0.008
D	2.80		3.00	0.11		0.118
E	1.50		1.75	0.059		0.0689
e		0.95			0.0374	
H	2.60		3.00	0.102		0.118
L	0.10		0.60	0.004		0.024
M			10°			10°

FOOT PRINT