Ordering number : EN *5651

Bi-CMOS LSI

LV2700V

Spread Spectrum Communications IC

Preliminary

Overview

The LV2700V provides the reception and transmission functions necessary for half-duplex communication in spread-spectrum communications systems.

Features

- Frequency conversion is not required. (direct signal processing at 236 MHz)
- Wide spread-spectrum bandwidth (20 MHz)
- Sanyo developed system for PN code synchronization
- Allows direct primary modulation (FSK and FM) by data and analog signals. (Maximum data rate: 150 kbps)
- Low-voltage operation (2.7 to 5.5 V)
- Low power dissipation (36 mW in RX mode)

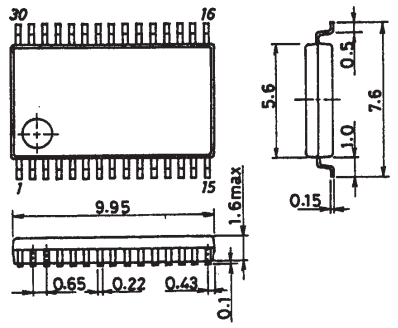
Functions

[TX Block]
- Spectrum spreader
- Crystal oscillator circuit
- PN code generator (M sequence)
- M sequence code length (31 or 63 chips) and tap switching
- 9.83 MHz PLL
- Band limiting filter (LPF) for data transmission

[RX Block]
- Spectrum despreader
- Synchronization supplementation and protection
- 236-MHz PLL
- PN code generator (M sequence)
- M sequence code length (31 or 63 chips) and tap switching
- FSK (FM) demodulator
- Lock detector

Package Dimensions

[LV2700V]



SANYO: SSOP30

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Allowable power dissipation	Pd max		150	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		3	V
Allowable voltage range	V_{CC}op		2.7 to 5.5	V

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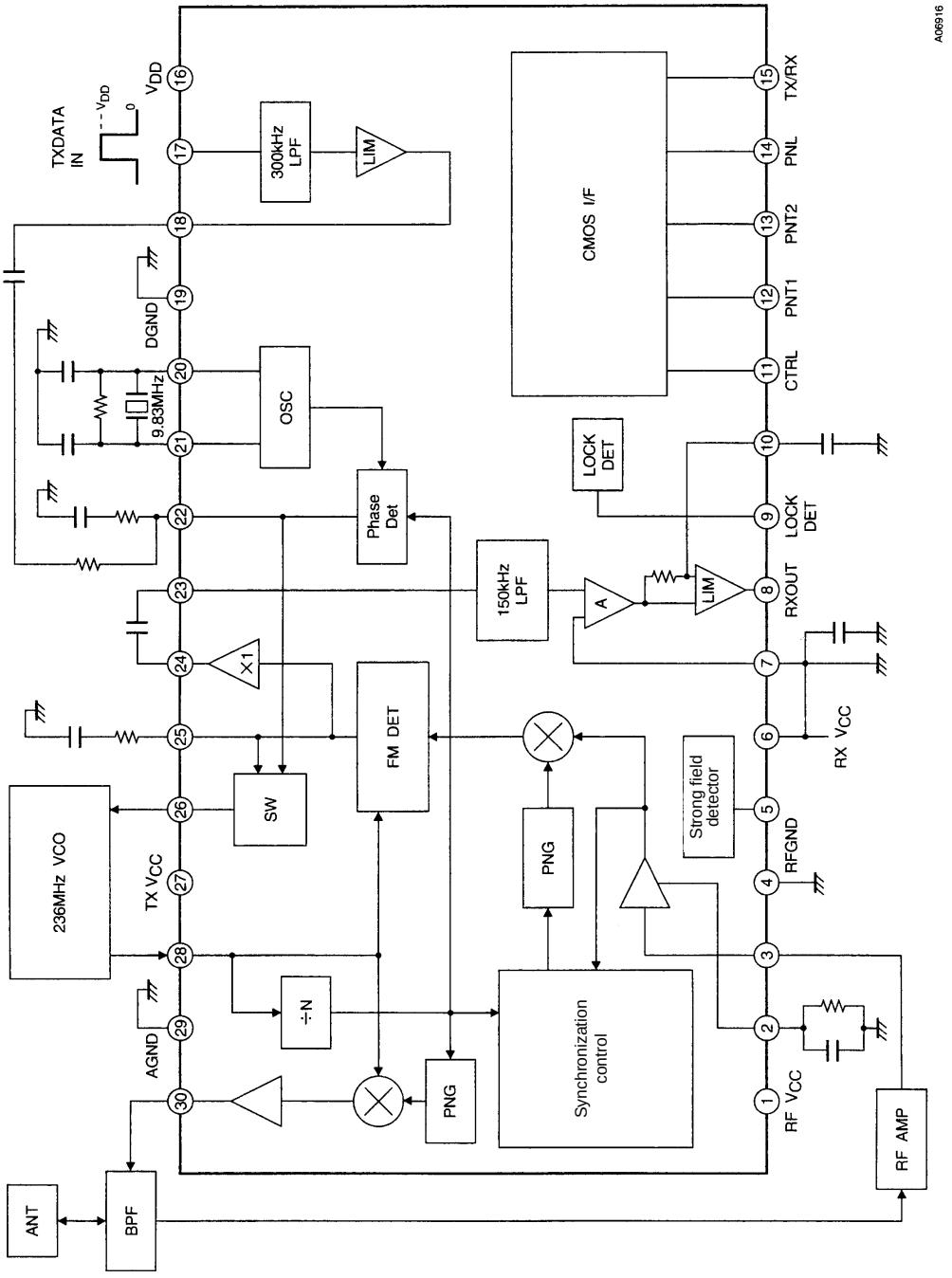
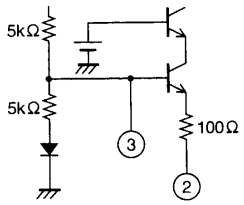
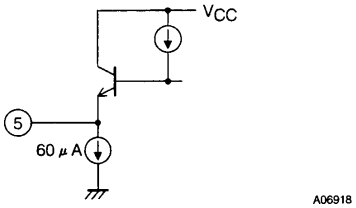
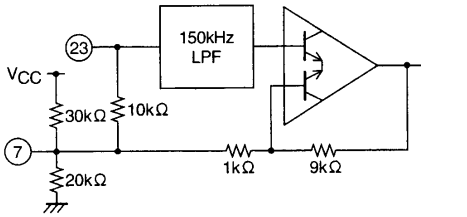
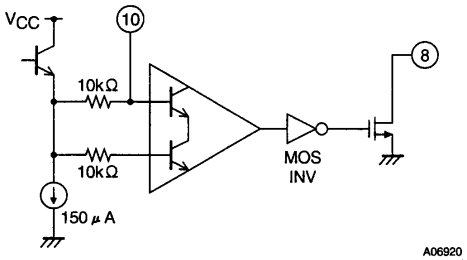
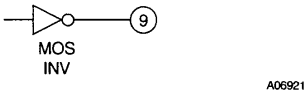
Electrical Characteristics at Ta = 25°C, V_{CC} = 3 V, fc = 236 MHz, fm = 10 kHz, Vm = 0.2 Vp-p

Parameter		Symbol	Conditions	Ratings			Unit
				min	typ	max	
Quiescent current		$I_{CCO}TX$	$TXV_{CC} + V_{DD}$		8	11	mA
		$I_{CCO}RX$	$RFV_{CC} + RXV_{CC} + V_{DD}$		12	16	mA
[TX Block]							
Modulated signal voltage		V_OTX	TXDATAOUT, f = 10 kHz		0.2		Vp-p
RF output voltage		V_OTX	TXREOUT		–35		dBm
Spread bandwidth		WS	TXRFOUT		19.7		MHz
[RX Block]							
Input sensitivity		V_SRX	RFIN			–75	dBm
Demodulated output 1	High level	V_ORX1H	RXOUT	2.5			V
	Low level	V_ORX1L	RXOUT			0.4	V
Demodulated output 1		V_ORX2	Pin 10 output w/o CEXT	240	300		mVrms
Total harmonic distortion		THD RX	Pin 10 output w/o CEXT		0.5	2	%
Signal-to-noise ratio		S/N	Pin 10 output w/o CEXT	45	55		dB
[CMOS-Level Interface]							
Input high-level voltage		V_IH	Pins 11 to 15, 17	2.1			V
Input low-level voltage		V_IL	Pins 11 to 15, 17			0.6	V
Output high-level voltage		V_OH	Pins 8, 9	2.5			V
Output low-level voltage		V_OL	Pins 8, 9			0.4	V
Input high-level current		I_IH	Pins 11 to 15, 17			5	µA
Input low-level current		IIL	Pins 11 to 15, 17			5	µA
Input amplitude		V_{IN}	VCOIN	–16			dBm
Crystal oscillator frequency conditions		X_{OSC}	XIN, XOUT	5		13	MHz
Input capacitance		C_{IN}	RFIN, XIN, VCOIN		2.5		pF

Block Diagram



Pin Functions

Pin No.	Pin	Pin voltage(V)	Pin function	Equivalent circuit
1	RFV_{CC}		RF block power supply	
2	REXT	0.2	Connection for the external capacitor and resistor used by the internal RF amplifier	
3	RFIN	1	RF input	
4	RFGND		RF block ground	
5	ANTDUMP	1.2	Output for the DC voltage used under strong reception conditions to prevent saturation of the RF amplifier. Voltage variability range: about 0.5 V	
6	RXV_{CC}		Reception block power supply	
7	BIASIN		DC bias voltage for the demodulation signal processing block (LPF, amplifier, limiter)	
8	RXOUT		Demodulated data output (This is an open drain output.)	
9	LOCK DET		Outputs a high level when PN code synchronization is established. (This is a CMOS-level output.)	
10	CEXT	Same as V7	Amplifier output for demodulated output. The pin 8 output data is made valid by connecting a capacitor between this pin and ground.	

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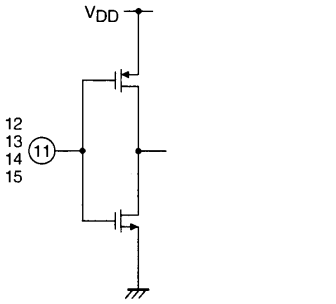
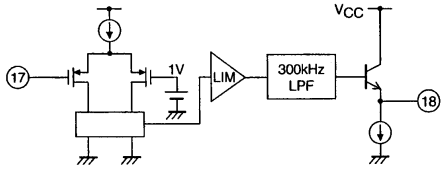
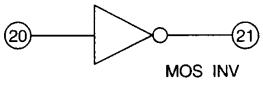
<table>
<tr><th>Pin No.</th><th>Pin</th><th>Pin voltage(V)</th><th>Pin function</th><th>Equivalent circuit</th></tr>
<tr><td>11</td><td>CTRL</td><td></td><td>Turns the optimal PN code synchronization control on or off. Control is turned on by a high level input.</td><td rowspan="5"> 

A06922</td></tr>
<tr><td>12</td><td>PNT1</td><td></td><td>Tap selection for the PN code (M sequence)</td></tr>
<tr><td>13</td><td>PNT2</td><td></td><td>Tap selection for the PN code (M sequence). These pins select one of three code types.
<table>
<tr><th>PNT1</th><th>PNT2</th><th>PN code</th></tr>
<tr><td>0</td><td>0</td><td>CODE1</td></tr>
<tr><td>0</td><td>1</td><td>CODE2</td></tr>
<tr><td>1</td><td>0</td><td>CODE3</td></tr>
<tr><td>1</td><td>1</td><td></td></tr>
</table>
0 = Low
1 = High</td></tr>
<tr><td>14</td><td>PNL</td><td></td><td>PN code length selection
High: 63 chips
Low: 31 chips</td></tr>
<tr><td>15</td><td>TX/RX</td><td></td><td>Send/receive mode selection.
High: Transmission
Low: Reception</td></tr>
<tr><td>16</td><td>V_{DD}</td><td></td><td>CMOS block power supply</td><td></td></tr>
<tr><td>17</td><td>TX DATAIN</td><td></td><td>Transmission data input (CMOS levels). Do not apply analog signals to this pin.</td><td rowspan="2"> 

A06923</td></tr>
<tr><td>18</td><td>TX DATAOUT</td><td>1.7
0.7
1Vp-p</td><td>Transmission data output. The output signal is band limited to 300 kHz and voltage limited to 1 Vp-p.</td></tr>
<tr><td>19</td><td>DGND</td><td></td><td>CMOS block ground</td><td></td></tr>
<tr><td>20</td><td>XIN</td><td>1/2V_{CC}</td><td>Input for the 9.8304 MHz reference oscillator inverter.</td><td></td></tr>
<tr><td>21</td><td>XOUT</td><td>1/2V_{CC}</td><td>Output for the 9.8304 MHz reference oscillator inverter.
Add a resistor of about 1 MΩ between XIN and XOUT.</td><td> 

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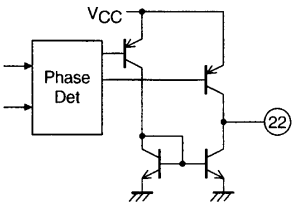
<tr><td>22</td><td>TXLPF</td><td>1.5</td><td>Connection for the 9.8-MHz PLL loop filter used in transmission.</td><td> 

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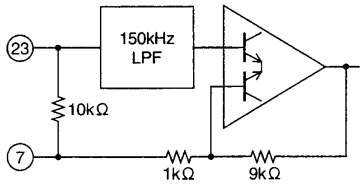
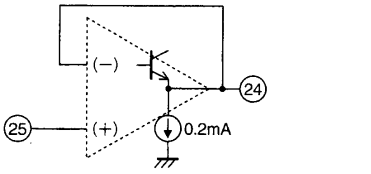
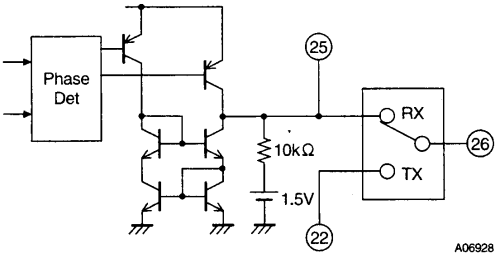
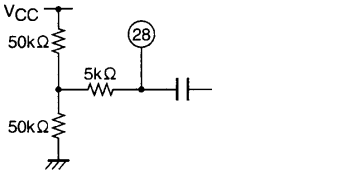
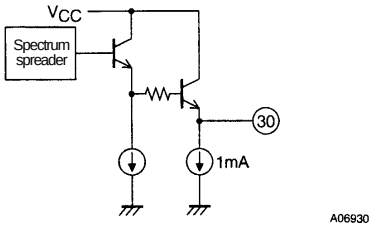
Pin No.	Pin	Pin voltage(V)	Pin function	Equivalent circuit
23	LPFIN	Same as V7	Demodulated signal input (loop filter output) used in reception.	
24	RXPDOUT	Same as V25	Pin 25 buffer output. Connect an external low-pass filter between pins 23 and 24 if required.	
25	RXLPF	1.5	Connection for the 236-MHz PLL loop filter used in reception.	
26	LPFOUT	1.5	Control input for the 236-MHz VCO. The LV2700V includes a switch for selecting the loop filter depending on the mode (transmission or reception).	
27	TX V_{CC}		Transmission power supply	
28	VCOIN	1/2 V_{CC}	Input for the output from the 236-MHz VCO. Minimum input level: about –20 dBm	
29	AGND		Analog system ground	
30	TX RFOUT	1.3	Spread-spectrum RF output (in transmission mode)	

Circuit Operation and Usage Notes

1. RF amplifier block

   The LV2700V includes an on-chip RF amplifier that provides a gain of about 15 dB. An input sensitivity of about –100 dBm can be acquired by adding an external 25-dB RF amplifier. Since IF frequency conversion is not used, a costly IF filter is not required. While the frequencies used are selected to be values relatively infrequently used in the weak field range (under 320 MHz), out of band components must be excluded using a bandpass filter after the antenna to improve both the interference rejection characteristics and the input sensitivity.

2. 236-MHz VCO

• The external 236-MHz VCO operates as follows in transmission and reception modes

[TX mode]

The VCO is adjusted to 236 MHz by a PLL circuit based on the 9.8304 reference.

That is, the phases of the VCO output that is input to pin 28 and the signal created by dividing the 9.8304 MHz reference oscillator output by 24 are compared and edge-type phase detector. The error signal is integrated by the pin 22 loop filter and fed back through pin 26 to the VCO control input.

[RX mode]

The spread spectrum RF signal input to pin 3 is amplified by 15 dB and a narrow band signal is recovered by a despreader circuit. The PLL circuit is then used for FM detection. That is, the phases of that signal and the VCO output from pin 28 are compared, and the error signal is integrated by the pin 25 loop filter and fed back through pin 26 to the VCO control input. An FM detected demodulated signal can be acquired from pin 25 at this time.

• Main characteristics

— For half-duplex communication, a VCO circuit using a SAW resonator is used for both transmission and reception.

Control sensitivity: 0.7 to 1.5 MHz/V

Frequency range: 236 MHz ±2 MHz

SAW resonator: We recommend the SAW resonators manufactured by Murata Mfg. Co., Ltd. (with a series resonance frequency error of ±500 ppm).

See the VCO circuit on page 8 for the recommended circuit, which is a Colpitts oscillator circuit.

— For unidirectional communication, an LC circuit based VCO may be used for the transmission side.

— The reception PLL circuit lock time is between 2 and 10 ms when power is first applied and between 0.5 and 1.0 ms after a transition from no input to the input present state.

3. FSK (FM) modulation technique

Modulation frequency range: 200 Hz to 150 kHz

When a modulated signal is applied to pin 22, there are limitations on low band FSK (FM) modulation, since this is equivalent to applying the modulation as a disturbance signal to the PLL circuit. If it is necessary to apply modulation to even lower bands, the 9.8 MHz reference oscillator circuit should be modified to be a VCXO circuit.

[For data input]

Apply the input data to pin 17. The signal is band limited to 300-kHz and then voltage limited to 1 Vp-p and output from pin 18. This signal is passed through a series RC circuit and connected to pin 22. The capacitor is a DC-cut capacitor of about 1 µF. The resistor should be about 20 kΩ, and is used for modulation adjustment.

[For analog signal input]

Do not use the internal 300-kHz low-pass filter and limiting amplifier, but rather apply the signal through the RC circuit to pin 22 directly.

When the resistor is 20 kΩ, the optimal signal input level will be about 0.3 Vp-p.

4. Notes on the FSK (FM) demodulated signal

[For data output]

Connect a capacitor of about 0.1 µF between pins 23 and 24, and another 1 µF capacitor between pin 10 and ground. This will allow a CMOS-level data output signal to be acquired from pin 8.

[For analog output]

An analog signal can be acquired from pin 10. In this case, do not insert a capacitor between pin 10 and ground. The cutoff frequency of the internal 150-kHz low-pass filter is set somewhat high for two reasons: to prevent PN code leakage and to limit attenuation of high-speed data as much as possible. As a result, this filter is inadequate for

reducing upper harmonic, high band, and other noise in audio signals. The LV2700V is designed so that good quality audio signals can be acquired by connecting an external filter between pins 23 and 24. The pin 24 output includes a buffer amplifier, thus making it a low-impedance output so that this output does not influence the pin 25 loop filter.

5. Pin 7
   The DC bias of the amplifier that is connected after the 150-kHz low-pass filter is set with an external resistor. Select a value for this resistor so that V7 will be 1.2 volts when V_{CC} is 3 volts.

6. Lock detection
   The LOCK DET pin (a CMOS-level output) goes high when PN code synchronization is detected. This output can be used as a simple technique for determining whether or not a carrier is present.

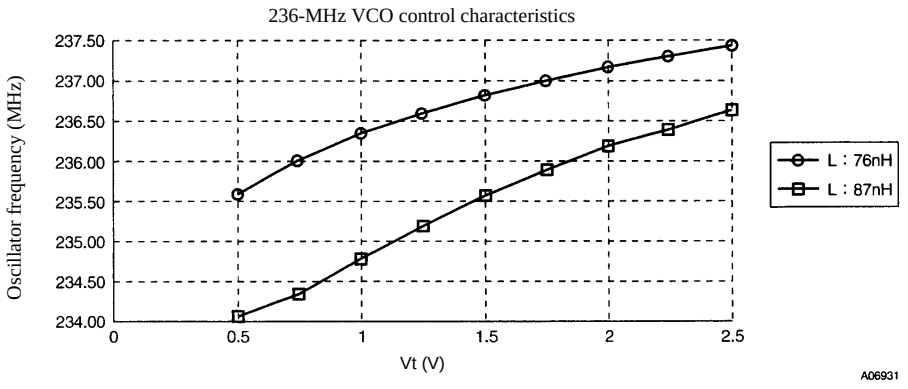
7. The ANTDUMP pin (pin 5)
   This pin outputs a DC level proportional to the RF input level. However, since this level is proportional to the input dBm value, it is not appropriate for use as an S-meter signal. It indicates voltage changes that are only meaningful in strong field reception conditions. It can be used to prevent saturation of the front end RF amplifier. However, the voltage change is +0.5 volt. (The pin 5 voltage for low input levels will be about 1.2 V.)

8. Power supply voltage application
   [TX mode]
   Provide the power-supply voltage to all the power-supply pins TXV_{CC}, RFV_{CC}, RXV_{CC}, and V_{DD}. Power saving is applied to the RF block bias internally.
   [RX mode]
   Provide the power-supply voltage to the RFV_{CC}, RXV_{CC}, and V_{DD} pin. TXV_{CC} must be left open.

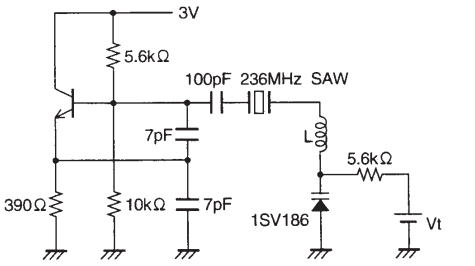
9. When changing the RF frequency from 236 MHz
   There are cases, for example due to considerations related to the SAW resonator characteristics, where it may be desirable to construct a system using a frequency other than 236 MHz. A 236-MHz AM synchronization detection output is used for PN code synchronization control. Since an RC circuit is used for the VCO output 90° phase shift circuit for this AM synchronization detection, it may not be possible to acquire the stipulated phase difference if the frequency is moved significantly far from 236 MHz. Assuming that a range of 45±5° is allowed, the corresponding frequency range will be 200 to 280 MHz.

Characteristics

236-MHz VCO Control Characteristics



VCO Circuit



Transistor: 2SC5245
Use an inductor with a value of 84 nH ±2% for the series inductor L.

An LC oscillator circuit may be used for the transmission side VCO for unidirectional communications systems.