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TFT COLOR LCD MODULE

NL10276AC30-09

38cm (15.0 Type)

XGA

Preliminary Data Sheet

(1st Edition)

All information is subject to change without notice.

Published by
1st Engineering Department
Color LCD Division
Display Device Operations Unit
NEC Electron Devices

INTRODUCTION

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Anti-radioactive design is not implemented in this product.

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

NL10276AC30-09 module is composed of the driver LSIs for driving the TFT (Thin Film Transistor) array with an amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into the narrow gap between a TFT array glass substrate and a color filter glass substrate.

RGB (Red, Green, Blue) data signals from a source system are modulated into a form suitable for active matrix addressing by the onboard signal processor and sent to the driver LSIs which in turn address the individual TFT cells.

Working as an electro-optical switch, each TFT cell regulates transmitted light from the backlight assembly when worked by the data source. Color images are created by regulating the amount of transmitted light through the array of red, green and blue dots.

1.2 APPLICATION

- PC monitor

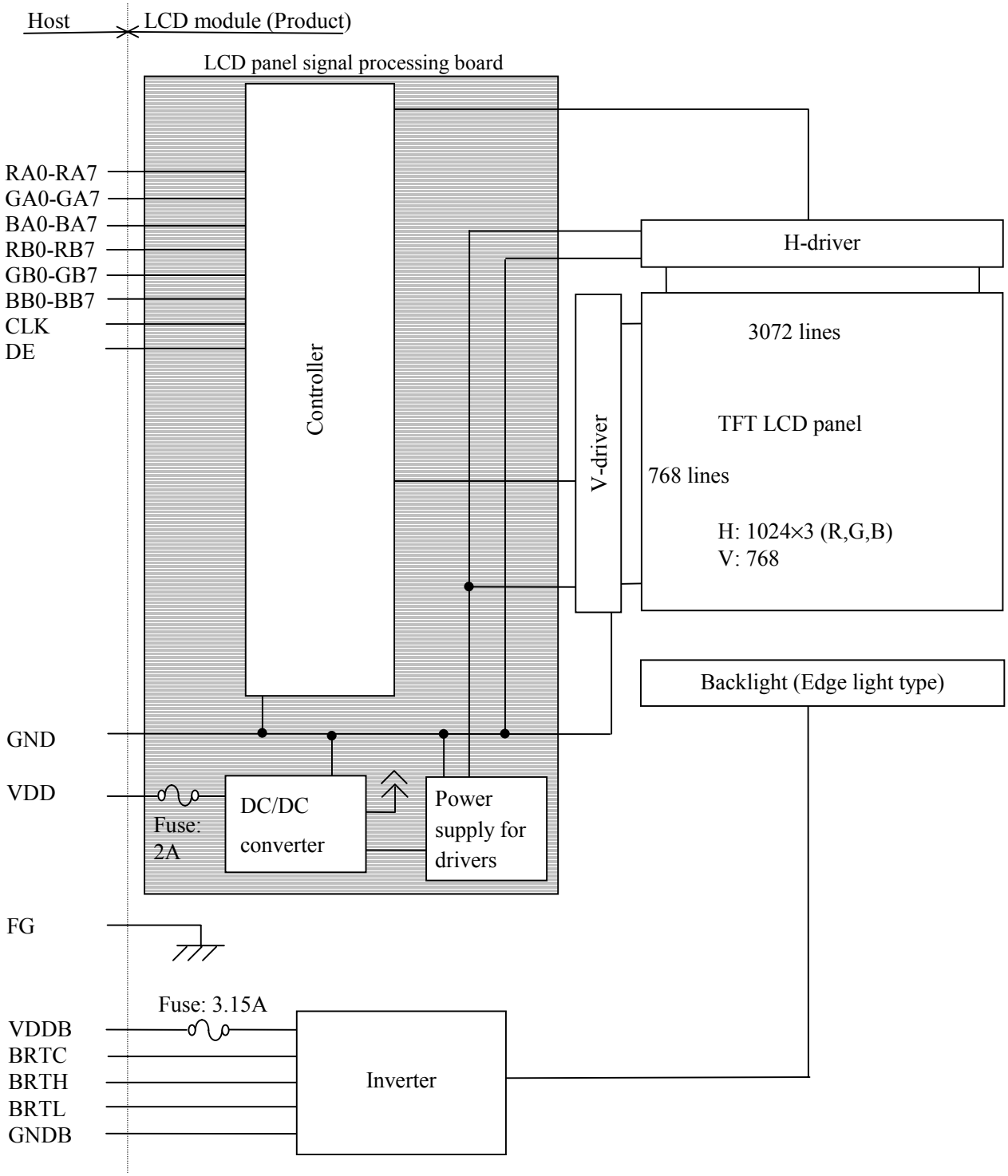
1.3 FEATURES

- Parallel 8bit interface
- Wide viewing angle
- High luminance
- High contrast
- Wide color gamut
- Luminance control
- Incorporated edge type backlight
- Replaceable lamp holder set and inverter

2. GENERAL SPECIFICATIONS

Display area	304.128 (H) × 228.096 (V) mm
Diagonal size of display	38 cm (15.0 inches)
Drive system	a-Si TFT active matrix
Display colors	16,777,216 colors (6bit + FRC)
Number of pixels	1024 (H) × 768 (V) pixel
Pixel arrangement	RGB (Red, Green, Blue) vertical stripe
Dot pitch	0.099 (H) × 0.297 (V) mm
Pixel pitch	0.297 (H) × 0.297 (V) mm
Module size	331.6 typ. (H) × 252.0 typ. (V) × 24.5 max.(D) mm
Weight	1500 g (typ.)
Contrast ratio	400:1 (typ.)
Viewing angle	*At the contrast ratio 10:1* • Horizontal: 60° (typ., left side, right side) • Vertical: 40° (typ., up side), 60° (typ., down side)
Designed viewing direction	• Viewing angle with optimum grayscale (γ=2.2): normal axis (perpendicular)
Polarizer pencil-hardness	3H (min.) [by JIS K5400]
Color gamut	*At LCD panel center* 72% (typ., design target) [against NTSC color space]
Response time	*Ton + Toff (10%→90%+90%→10%)* (30) ms (typ.)
Luminance	400cd/m^2 (typ., design target)
Signal system	Parallel 8bit interface (2port) [RGB 8bit data, CLK, DE]
Supply voltage	5V (for LCD panel signal processing board) 12V (for Backlight inverter)
Backlight	Edge light type: 4 cold cathode fluorescent lamps [Replaceable parts] • Lamp holder set: 150LHS17 • Inverter: 150PW161
Power consumption	*At maximum luminance and checkered flag pattern* 22 W (Typ.)

3. BLOCK DIAGRAM



Note1: GND is signal ground for logic and LCD driving. Connections of GND, FG (frame ground) and GNDB are not decided in the LCD module. These grounds should be connected to system ground in customer equipment.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	331.6 ± 1.0 (H) × 252.0 ± 1.0 (V) × 24.5 max. (D) Note1	mm
Display area	304.128 (H) × 228.096 (V) Note1	mm
Weight	1,500 (typ.), 1550 (max.)	g

Note1: See "**11.OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameters		Symbol	Rating	Unit	Remarks
Supply voltage	LCD panel signal board and driver	VDD	-0.3 to +6.0	V	Ta = 25°C
	Inverter	VDDB	-0.3 to +15.0	V	
Input voltage	Display signals Note3	Vi	-0.3 to +4.0	V	Ta = 25°C VDD=5.0V
	BRTC	ViB1	TBD	V	Ta = 25°C VDDB=12V
	BRTL	ViB2	TBD	V	
Storage temperature		Tst	-20 to +60	°C	-
Operating temperature		Top1	0 to +50		Front view surface Note2
		Top2	TBD		Rear view surface Note3
Relative humidity Note4		RH	≤ 95	%	Ta≤ 40°C
			≤ 85		40°C <Ta≤ 50°C
Absolute humidity Note4		-	≤ 78 Note5	g/m^3	Ta>50°C
Operating altitude		-	≤ 4,850	m	0°C≤ Ta ≤ 50°C
Storage altitude		-	≤ 13,600	m	-20°C≤ Ta ≤ 60°C

Note1: Display signals are DE, CLK, RA0 to RB7, GA0 to GB7and BA0 to BB7.
Note2: Measured at the LCD panel surface center (including self-heat)
Note3: Measured at the rear shield center (including self-heat)
Note4: No condensation
Note5: Ta = 50°C, RH = 85%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for LCD panel signal processing board

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage		VDD	4.5	5.0	5.5	V	-
Supply current		IDD	-	300 Note1	TBD Note2	mA	VDD=5.0V
Ripple voltage		VRP	-	-	100	mV	for VDD
Logic input voltage	Low	VIL	0	-	0.8	V	-
Logic input voltage	High	VIH	2.0	-	3.6	V	

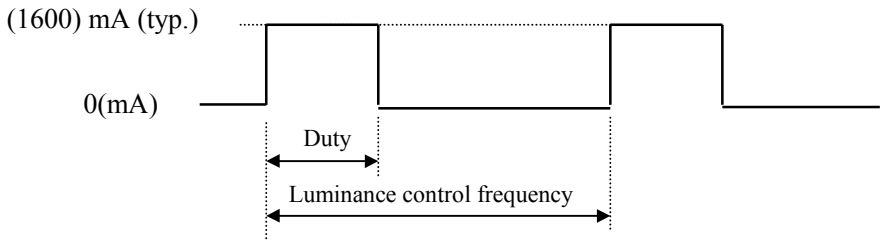
Note1: Checkered flag pattern (by EIAJ ED-2522)
Note2: Pattern for maximum current

4.3.2 Driving for backlight inverter

(Ta = 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Supply voltage		VDDB	10.8	12.0	13.2	V	Backlight power supply
Supply current	Note1	IDDB	-	(1600)	TBD	mA	VDDB=12.0V (at max. luminance)
Logic input voltage	BRTC	ViBL1	0	-	0.8	V	-
		ViBH1	2.0	-	5.0	V	
Logic input current	BRTC	IiBL1	-610	-	-	µA	-
		IiBH1	-	-	440	µA	
BRTL input current	BRTL	IiB2	-130	-	-	µA	-

Note1: Inverter current wave is as follows.



Maximum luminance control : 100% (Duty)
Minimum luminance control : 20% (Duty)
Luminance control frequency : 280±14 Hz (typ.)

4.3.3 Supply voltage ripple

This module works, even if the ripple levels are beyond the below values (See following the table.), but might have noise on the display image. Consider and evaluate enough before installing this module into customer's system.

Supply voltage (Acceptable level)	Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD (for LCD panel signal processing board; 5.0V)	≤ 100	mVp-p
VDDB (for backlight inverter; 12.0V)	≤ 200	mVp-p

Note1: The permissible ripple voltage includes spike noise.

4.3.4 Fuses

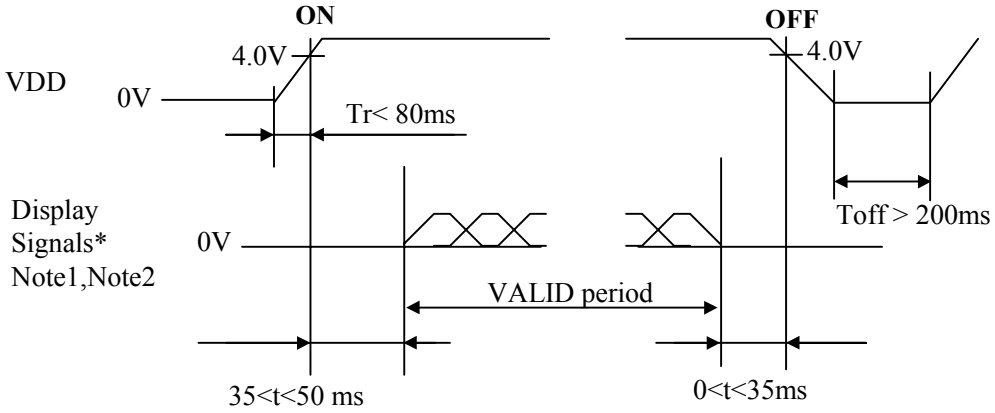
This module has fuses listed below. Check and evaluate power supplies of customer's system.

Fuse		Rating Note1	Unit	Remarks
Type	Supplier			
FCC16202AB	KAMAYA ELECTRIC Co., Ltd.	2	A	VDD (for LCD panel signal processing board)
		TBD	V	
MMCT3.15A	SOC Corporation	3.15	A	VDDB (for backlight inverter)
		TBD	V	

Note1: The power capacity should be more than twice of fuse current ratings. If the power capacity is less than the criteria value, the fuse may not blow, and then nasty smell, smoking and so on may occur.

4.4 SUPPLY VOLTAGE SEQUENCE

4.4.1 Sequence for LCD panel signal processing board

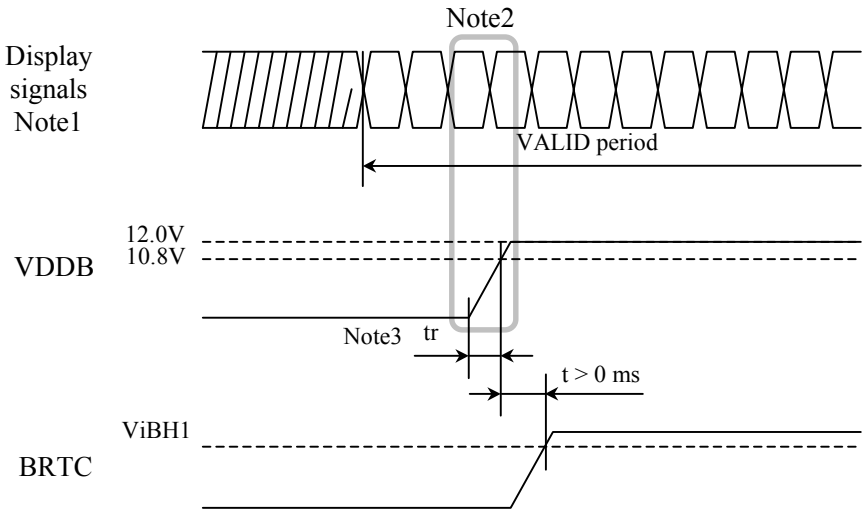


Note1: Display signals (DE, CLK, RA0 to RB7, GA0 to GB7, BA0 to BB7) must be "0" voltage (V), exclude the VALID period (See above sequence diagram). If input voltage to display signals is higher than 0.3V, the internal circuits might be damaged.

Note2: In terms of fall-off-potential while VDD leading edge is below 4.0V, protection circuits may work and then the module may not work.

Note3: If display signals to this module are cut while this module is working, even if the signal input to it once again, it may not work normally.

4.4.2 Sequence for backlight inverter



Note1: These are the display signals for LCD panel signal processing board.

Note2: The backlight power voltage (VDDB) should be inputted within the valid period of display signals, in order to avoid unstable data display.

Note3: The tr should be less than 800ms when BRTC terminal [Socket: CN201, Pin No.5] (See '4.5.2 Backlight inverter'.) is Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

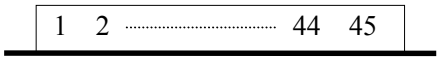
4.5.1 LCD panel signal processing board

CN1 socket (Module side): IL-FHR-B45S-HF (Japan Aviation Electronics Industry Limited)

Pin No.	Symbol	Function	Description
1	N.C.	Non-connection	Keep the terminal open.
2	VDD	Power Supply	+5V±10%
3	VDD		
4	VDD		
5	VDD		
6	RA0	Odd pixel data R	Odd pixel data R input (CMOS level) RA0: Least significant bit
7	RA1		
8	RA2		
9	RA3		
10	GND	Ground	Connect to system ground.
11	RA4	Odd pixel data R	Odd pixel data R input (CMOS level) RA7: Most significant bit
12	RA5		
13	RA6		
14	RA7		
15	GND	Ground	Connect to system ground.
16	GA0	Odd pixel data G	Odd pixel data G input (CMOS level) GA0: Least significant bit
17	GA1		
18	GA2		
19	GA3		
20	GND	Ground	Connect to system ground.
21	GA4	Odd pixel data G	Odd pixel data G input (CMOS level) GA7: Most significant bit
22	GA5		
23	GA6		
24	GA7		
25	GND	Ground	Connect to system ground.
26	BA0	Odd pixel data B	Odd pixel data B input (CMOS level) BA0: Least significant bit
27	BA1		
28	BA2		
29	BA3		
30	GND	Ground	Connect to system ground.
31	BA4	Odd pixel data B	Odd pixel data B input (CMOS level) BA7: Most significant bit
32	BA5		
33	BA6		
34	BA7		
35	GND	Ground	Connect to system ground.
36	N.C.	Non-connection	Keep the terminal open.
37	GND	Ground	Connect to system ground.
38	N.C.	Non-connection	Keep the terminal open.
39	GND	Ground	Connect to system ground.
40	N.C.	Non-connection	Keep the terminal open.
41	GND	Ground	Connect to system ground.
42	DE	Data enable	Data enable input(CMOS level)
43	GND	Ground	Connect to system ground.
44	CLK	Dot clock	Dot clock input(CMOS level)
45	GND	Ground	Connect to system ground.

Note1: Do not keep pins free (except 1,36,38 and 40) to avoid noise issue.

CN1 socket: Figure of socket

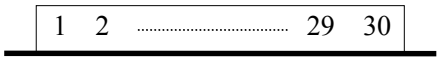


CN2 socket (Module side): IL-FHR-B30S-HF (Japan Aviation Electronics Industry Limited)

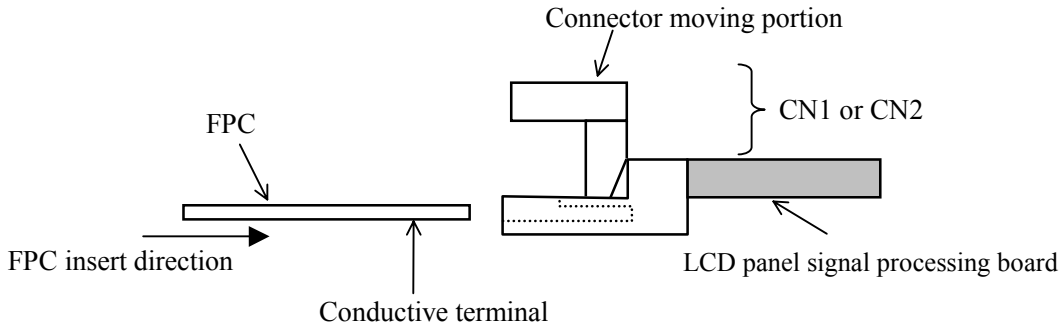
Pin No.	Symbol	Function	Description
1	RB0	Even pixel data R	Even pixel data R input (CMOS level) RB0: Least significant bit
2	RB1		
3	RB2		
4	RB3		
5	GND	Ground	Connect to system ground.
6	RB4	Even pixel data R	Even pixel data R input (CMOS level) RB7: Most significant bit
7	RB5		
8	RB6		
9	RB7		
10	GND	Ground	Connect to system ground.
11	GB0	Even pixel data G	Even pixel data G input (CMOS level) GB0: Least significant bit
12	GB1		
13	GB2		
14	GB3		
15	GND	Ground	Connect to system ground.
16	GB4	Even pixel data G	Even pixel data G input (CMOS level) GB7: Most significant bit
17	GB5		
18	GB6		
19	GB7		
20	GND	Ground	Connect to system ground.
21	BB0	Even pixel data B	Even pixel data B input (CMOS level) BB0: Least significant bit
22	BB1		
23	BB2		
24	BB3		
25	GND	Ground	Connect to system ground.
26	BB4	Even pixel data B	Even pixel data B input (CMOS level) BB7: Most significant bit
27	BB5		
28	BB6		
29	BB7		
30	GND	Ground	Connect to system ground.

Note1: Do not keep pins free to avoid noise issue.

CN2 socket: Figure of socket



Note2: Insert the FPC into the CN1 and CN2 with conductive terminal down.



Sectional drawing of CN1 and CN2

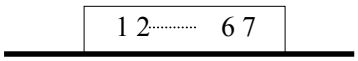
4.5.2 Backlight inverter

CN201 socket (Module side): S7B-PH-SM3-TB (J.S.T. Mfg Co., Ltd.)
Adaptable plug: TBD

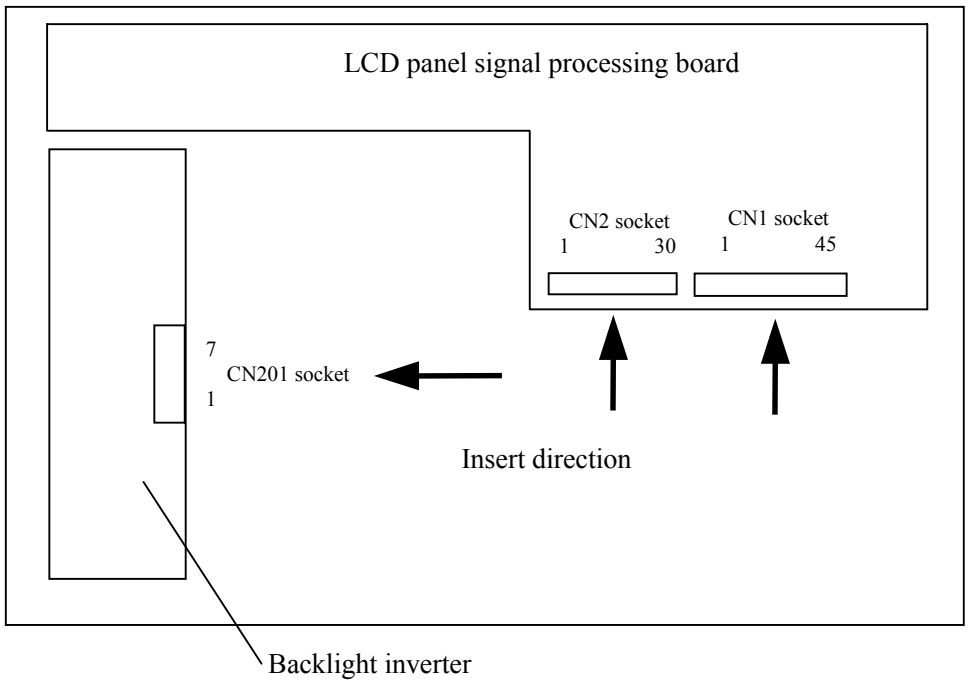
Pin No.	Symbol	Function	Description
1	VDDB	Power supply for backlight	+12V±10%
2	VDDB		
3	GNDB	Ground for backlight	Connect to system ground.
4	GNDB		
5	BRTC	Backlight ON/OFF control signal	"High" or "Open" : Backlight ON "Low" : Backlight OFF
6	BRTH	Luminance control signal	See "**4.6 LUMINANCE CONTROLS**".
7	BRTL		

Note1: Do not keep pins free to avoid noise issue.

CN201 socket: Figure of socket

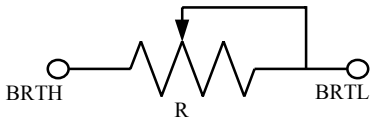


4.5.3 Position of sockets



4.6 LUMINANCE CONTROLS

4.6.1 Luminance control method

Control method	Function and adjustment	PWSEL	BRTP
Variable resistor Note1	The variable resistor for luminance control should be 10kΩ type, and zero point of the resistor corresponds to the minimum of luminance.  Max. luminance (TBD%): R=10kΩ Min. luminance (TBD%): R=0Ω Mating variable resistor: 10kΩ ±5%, B curve, 1/10W	High or Open	Open
Voltage Note1	BRTH should be fixed to 0V, and input to BRTL as follows. Max. Luminance (TBD%): 1V(typ.) Min. Luminance (TBD%): 0V		

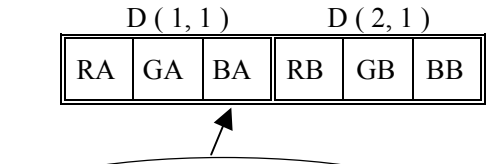
4.7 DISPLAY COLORS AND INPUT DATA SIGNALS

Display color		Data signal (0: Low level, 1: High level)																									
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:								:								:				
	↓				:								:								:				
	bright	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	↑				:								:								:				
	↓				:								:								:				
	bright	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue grayscale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑				:								:								:				
	↓				:								:								:				
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note: The combination of 8-bit signals (256-grayscale level) results in equivalent to 16,777,216 colors.

4.8 DISPLAY POSITIONS

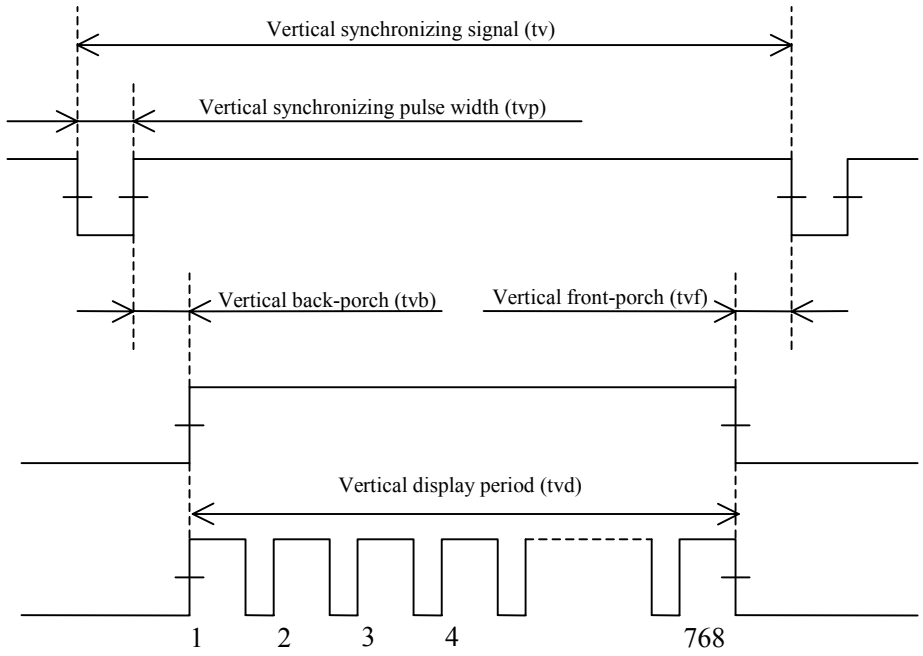
Odd Pixel: RA= R DATA Even Pixel : RB=R DATA
Odd Pixel: GA= G DATA Even Pixel : GB=G DATA
Odd Pixel: BA= B DATA Even Pixel : BB=B DATA

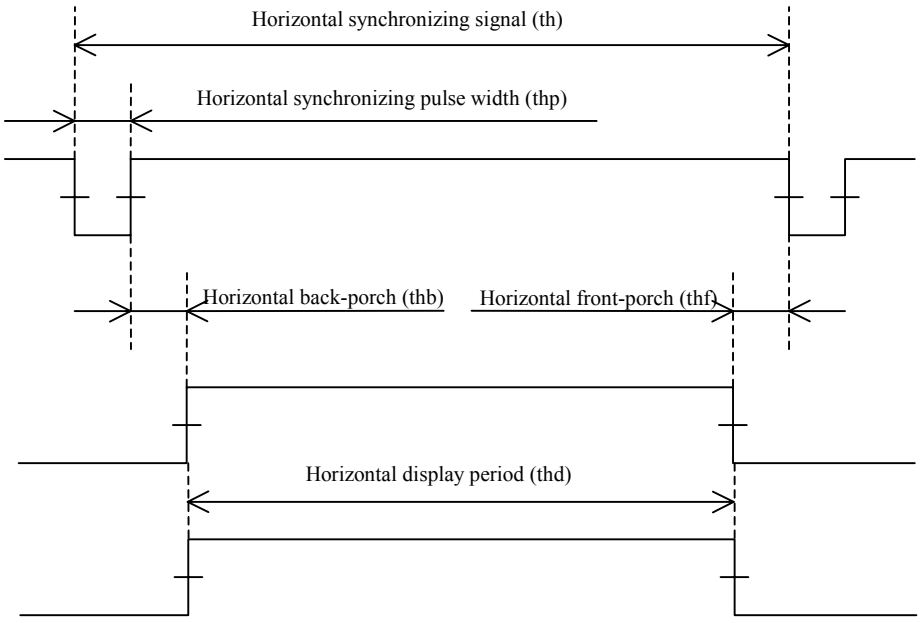


D(1, 1)	D(2,1)	•••	D(1024,1)
D(1,2)	D(2, 2)	•••	D(1024,2)
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
•	•	•	•
D(1,768)	D(2,768)	•••	D(1024,768)

4.9 INPUT SIGNAL TIMINGS

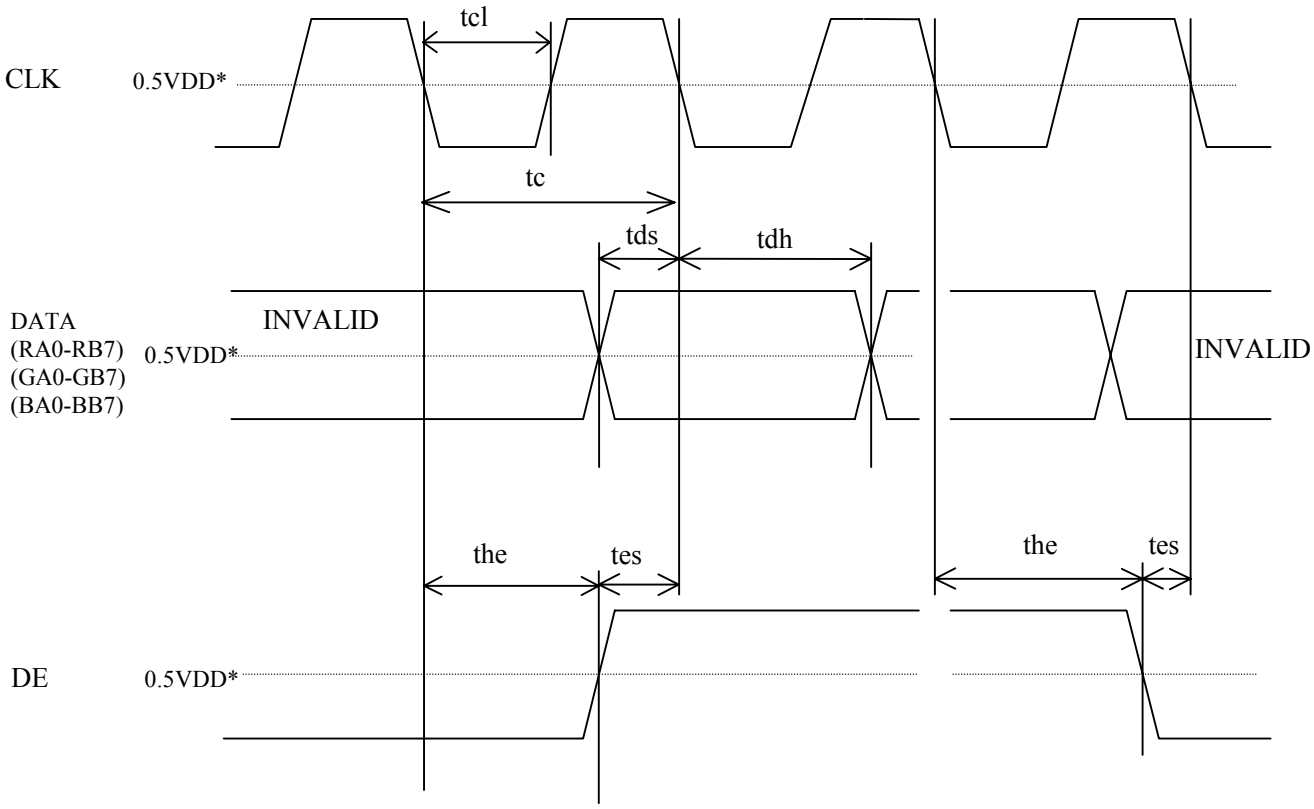
4.9.1 Definition of input signal timings



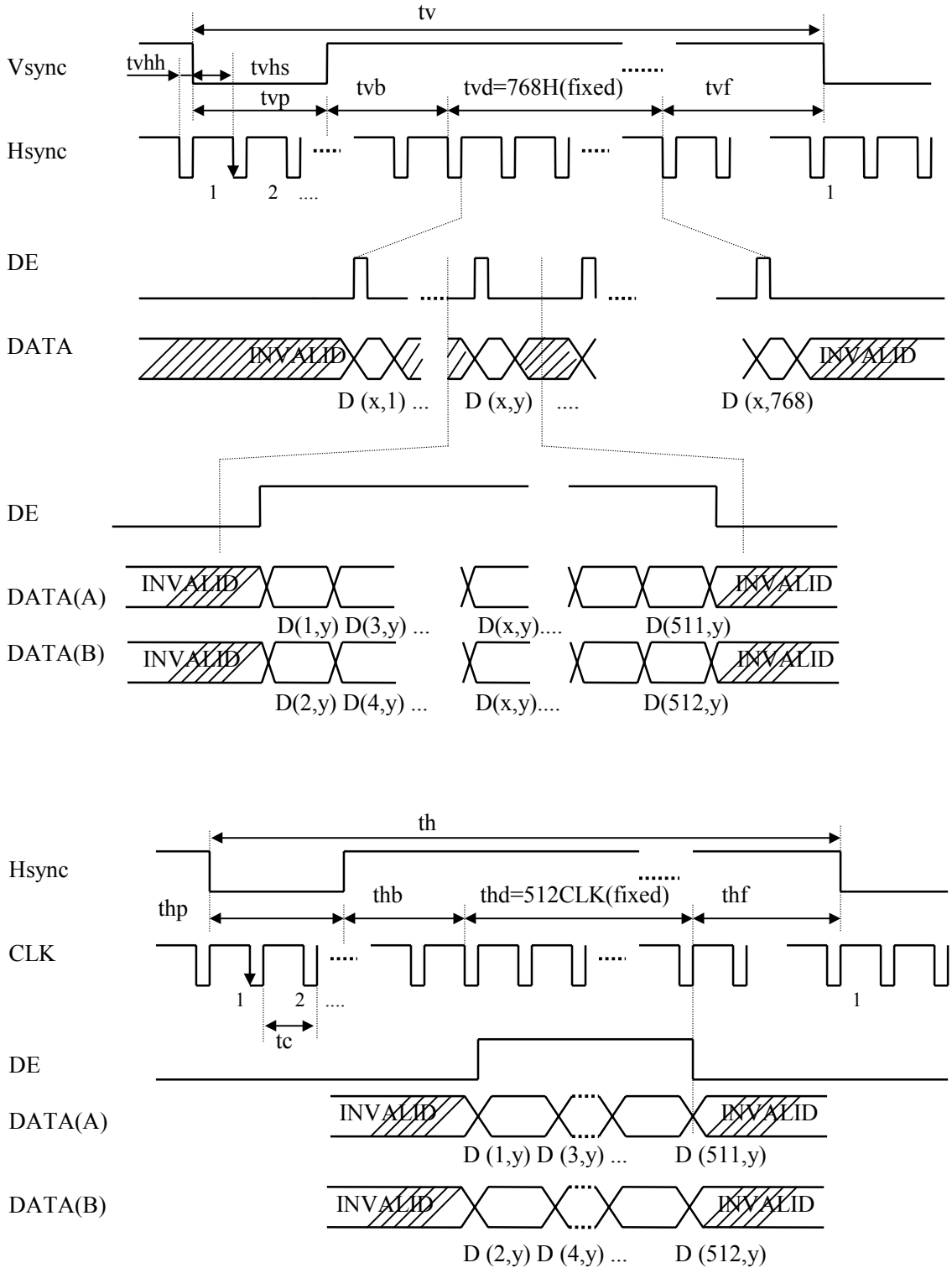


Note1: See "**4.9.4 Detailed input signal timing chart for numeration of pulse**".
Note2: These diagrams indicate virtual signal for set up to timing.

4.9.2 General input signal timing chart



4.9.3 Detailed input signal timing chart



DATA(A): RA0-RA7, GA0-GA7, BA0-BA7
DATA(B): RB0-RB7, GB0-GB7, BB0-BB7

4.9.4 Timing characteristics (2 port input)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency	Vf=75Hz	1/ tc	TBD -	39.375 25.397	TBD -	MHz ns	-
		Vf=60Hz		TBD -	32.500 30.769	TBD -	MHz ns	
	Duty		tcl / tc	0.4	0.5	0.6	-	-
Hsync	Period	Vf=75Hz	th	(12.3) (550)	16.660 656	- (1000)	μs CLK	typ.=60.023kHz
		Vf=60Hz		(12.3) (550)	20.677 672	- (1000)	μs CLK	typ.=48.363kHz
	Display period		thd	-	512	-	CLK	-
	Front-porch	Vf=75Hz	thf	-	8	-	CLK	-
		Vf=60Hz		-	12	-		
	Pulse width	Vf=75Hz	thp *	-	48	-	CLK	-
		Vf=60Hz		-	68	-		
	Back-porch	Vf=75Hz	thb *	-	88	-	CLK	-
		Vf=60Hz		-	80	-		
	* thp + thb			(38)	-	-	CLK	-
Vsync	Period	Vf=75Hz	tv	- (771)	13.328 800	TBD -	ms H	typ=75.029Hz
		Vf=60Hz		- (771)	16.666 806	TBD -	ms H	typ=60.0Hz
	Display period		tvd	-	768	-	H	-
	Front-porch	Vf=75Hz	tvf *	-	1	-	H	-
		Vf=60Hz		-	3	-		
	Pulse width		tvp *	-	3	-	H	-
				-	6	-		
	Back-porch		tvb *	-	28	-	H	-
				-	29	-		
	* tvp + tvb +tvf			(3)	-	-	H	-
	Vsync-Hsync timing		tvhs	1	-	-	CLK	-
	Hsync-Vsync timing		tvhh	1	-	-	CLK	-
DATA (RA0-RB7) (GA0-GB7) (BA0-BB7)	DATA-CLK (Set up)		tds	(2)	-	-	ns	-
	CLK-DATA (Hold)		tdh	(2)	-	-	ns	-
DE	DE-CLK timing		tes	(2)	-	-	ns	-
	CLK-DE timing		the	(2)	-	-	ns	-

Note1: All parameters should be kept within the specified range. Also Definition of unit is as follows.
1CLK = tc
1H = th

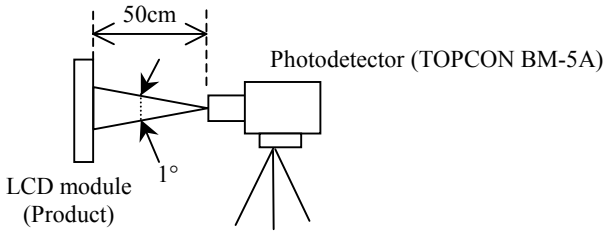
4.10 OPTICS

4.10.1 Optical characteristics

Parameter Note1			Symbol	Condition	min.	typ.	max.	Unit	Remarks
Contrast ratio			CR	White/Black, at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	(250)	350	-	-	Note2
Luminance			L	White, at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	(250)	400 (design target)	-	cd/m^2	-
Luminance uniformity			LU	-	-	-	1.1	1.3	Note3
Chromaticity			W	White (x, y)	-	(0.313),(0.329)	-	-	-
			R	Red (x, y)	-	TBD	-	-	
			G	Green (x, y)	-	TBD	-	-	
			B	Blue (x, y)	-	TBD	-	-	
Color gamut			C	θR = 0°, θL = 0°, θU = 0°, θD = 0° at center, against NTSC color space	60	72 (design target)	-	%	
Response time Note4			Ton	White to Black	-	TBD	TBD	ms	Note5
			Toff	Black to White	-	TBD	TBD	ms	
			Ton + Toff (10%→90%+90%→10%)		-	(30)	-	ms	-
Viewing angle	CR =10	Right	θR	θU = 0°, θD = 0°	TBD	60	-	°	Note6
		Left	θL	θU = 0°, θD = 0°	TBD	60	-	°	
		Up	θU	θR = 0°, θL = 0°	TBD	40	-	°	
		Down	θD	θR = 0°, θL = 0°	TBD	60	-	°	

Note1: Measurement conditions are as follows.
Ta = 25°C, VDD = 5.0V, VDDB = 12.0V
Display mode: 60Hz

Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note2: See "4.10.2 Definition of contrast ratio".
Note3: See "4.10.3 Definition of luminance uniformity".
Note4: Product surface temperature: TBD °C
Note5: See "4.10.4 Definition of response times".
Note6: See "4.10.5 Definition of viewing angles".

4.10.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

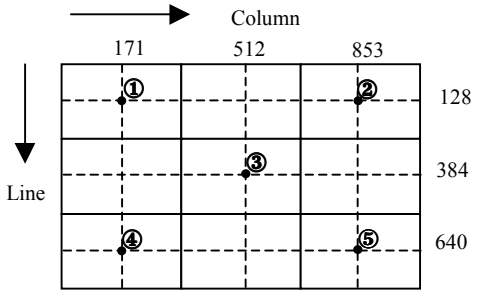
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.10.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

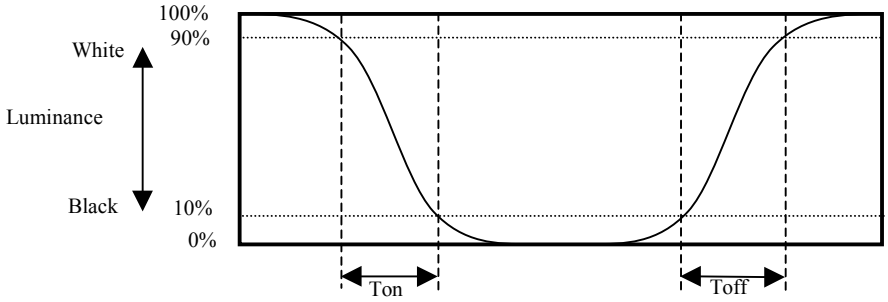
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

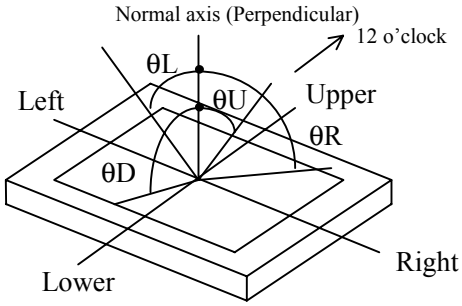


4.10.4 Definition of response times

Response time is measured, the luminance changes from "white" to "black", or "black" to "white" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 90% down to 10%. Also Toff is the time it takes the luminance change from 10% up to 90% (See the following diagram.).



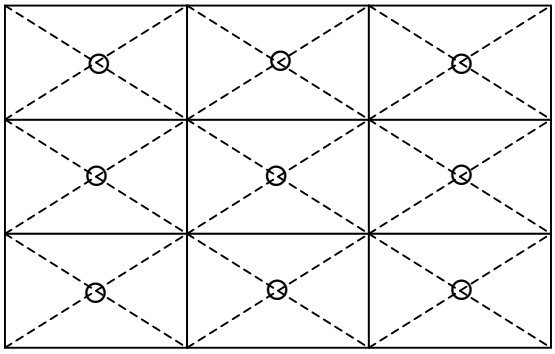
4.10.5 Definition of viewing angles



5. RELIABILITY TEST

Test item		Condition	Judgment
High temperature and humidity (Operation)		① 50 ± 2°C, RH = 85%, 240hours ② Display data is black.	No display malfunctions Note1
Heat cycle (Operation)		① 0 ± 3°C…1hour 55 ± 3°C…1hour ② 50cycles, 4hours/cycle ③ Display data is black.	No display malfunctions Note1
Thermal shock (Non operation)		① -20 ± 3°C…30minutes 60 ± 3°C…30minutes ② 100cycles, 30minutes/cycle ③ Temperature transition time is within 5 minutes.	No display malfunctions Note1
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z direction ④ 50 times each directions	No display malfunctions Note1 No physical damages
Mechanical shock (Non operation)		① 294m/ s^2, 11ms ② X, Y, Z direction ③ 3 times each directions	No display malfunctions Note1 No physical damages
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	No display malfunctions Note1
Dust (Operation)		① 15 kinds of dust (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	No display malfunctions Note1
Low pressure	operation	53.3 kPa 0°C±3°C --- 24 hours 50°C±3°C --- 24 hours	Note1
	non-operation	15 kPa -20°C±3°C --- 24 hours -60°C±3°C --- 24 hours	

Note1: Display functions are checked under the same conditions as product inspection.
Note2: See the following figure for discharge points.



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS", after understanding this contents!**

This sign has the meaning that customer will get an electrical shock, if customer has wrong operations.

This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS

Do not touch HIGH VOLTAGE PART of the inverter while turn on. Customer will be in danger of an electric shock.

∗ Pay attention to handling for the working backlight and IC! It may be over 35°C from ambient temperature.

∗ Do not shock and press the LCD panel and the backlight. There will be in danger of breaking, because they are made of glass. (Shock: To be not greater 294m/s^2 and to be not greater 11ms, Pressure: To be not greater 19.6N)

6.3 ATTENTIONS

6.3.1 Handling of the product

① Take hold of both ends without touch the circuit board when customer pulls out products (LCD modules) from packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.
② Do not hook cables nor pull connection cables such as flexible cable and so on, for fear of damage.
③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.
④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.
⑤ The torque for mounting screws must never exceed 0.39N·m. Higher torque values might result in distortion of the bezel.
⑥ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC Corporation recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.
⑦ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

6.3.2 Environment

① Dewdrop atmosphere must be avoided.

② Do not operate or store in high temperature or high humidity atmosphere. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.

③ Do not operate in high magnetic field. Circuit boards may be broken down by it.

④ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

① Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.

② The display color may be changed by viewing angle because of the use of condenser sheet in the backlight unit.

③ Optical characteristics may be changed by input signal timings.

④ This module uses cold cathode fluorescent lamps. The lifetime of lamps is shortened conspicuously at low and high temperatures.

6.3.4 Other

① All GND, GNDB, VDD and VDDB terminals should be used without a non-connected line.

② Do not disassemble a product or adjust volume without permission of NEC Corporation.

③ See 'REPLACEMENT MANUAL FOR LAMP HOLDER SET', if customer would like to replace backlight lamps.

④ Pay attention not to insert waste materials inside of products, if customer uses screwnails.

⑤ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC Corporation for repair and so on.

⑥ Not only the module but also the equipment that used the module should be packed and transported as the module becomes vertical. Otherwise, there is the fear that a display dignity decreases by an impact or vibrations."

General characteristics for the LCD

The following items are neither defects nor failures.

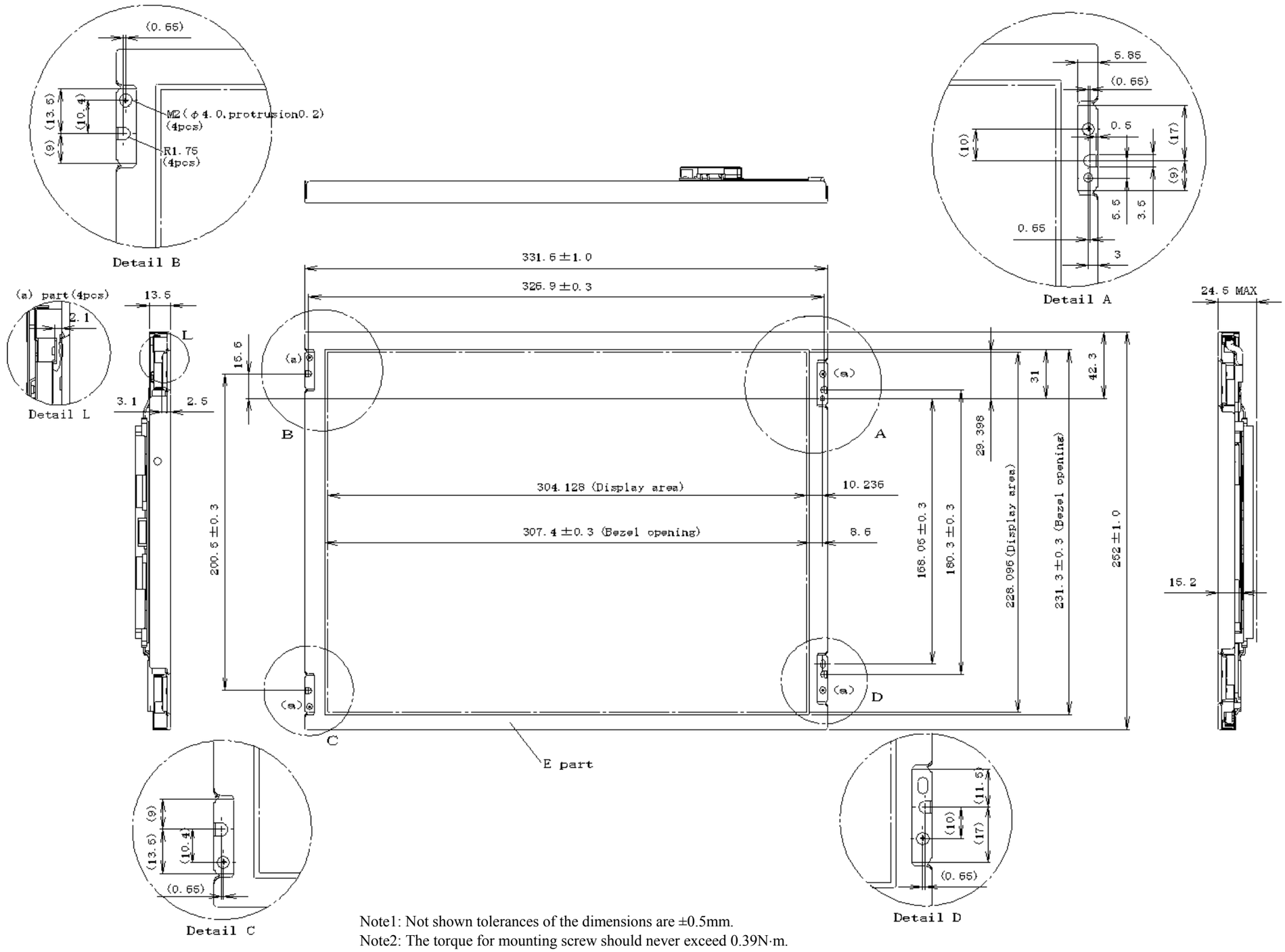
∗ Response time, luminance and color may be changed by ambient temperature.

∗ The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.

∗ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.

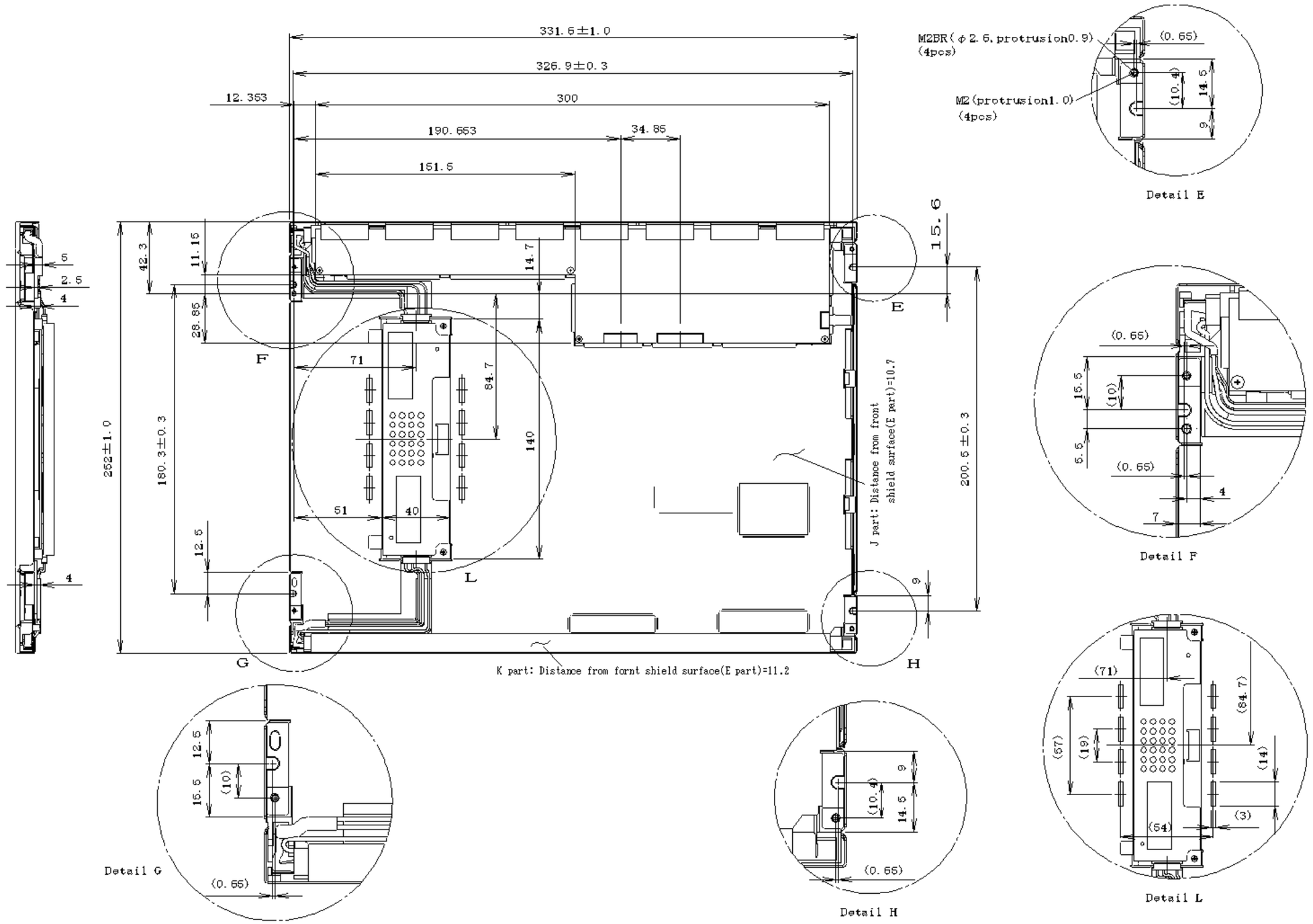
7. OUTLINE DRAWINGS(Unit: mm)

7.1 Front view



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for mounting screw should never exceed 0.39N·m.

7.2 Rear view



Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for mounting screw should never exceed 0.39N·m.

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and writer
1st edition	DOD - M - 0578	Aug. 28, 2001	**Revision contents** New issue **Signature of writer** *Approved by* Toshihide Ito TOSHIHIDE ITO *Checked by* *Prepared by* R. Kawashima R. KAWASHIMA