Surface Mount Capacitive Silicon Absolute Pressure Sensor

KP100

Data Sheet

Features

- Digital output
- Serial Peripheral Interface (SPI)
- Offset calibrated
- CMOS compatible surface micromachining
- Diagnostic modes
- SMD housing

P-DSOF-8-3

Type	Marking	Ordering Code	Pressure Range	Package
KP100	see below	Q62705-K348	60 kPa- 130 kPa	P-DSOF-8-3

Marking

Each device is marked with a human readable code on the side of Pins 5 to 8. This code contains the supplier logo, a date code, wafer lot number and an offset code.

Product Description

The KP100 is an absolute pressure sensor with SPI interface for side airbag applications. The basic accuracy including temperature drift is ±5%. The KP100 offers some diagnosis features in order to allow a sensor status analysis.

Pin Configuration

(top view)

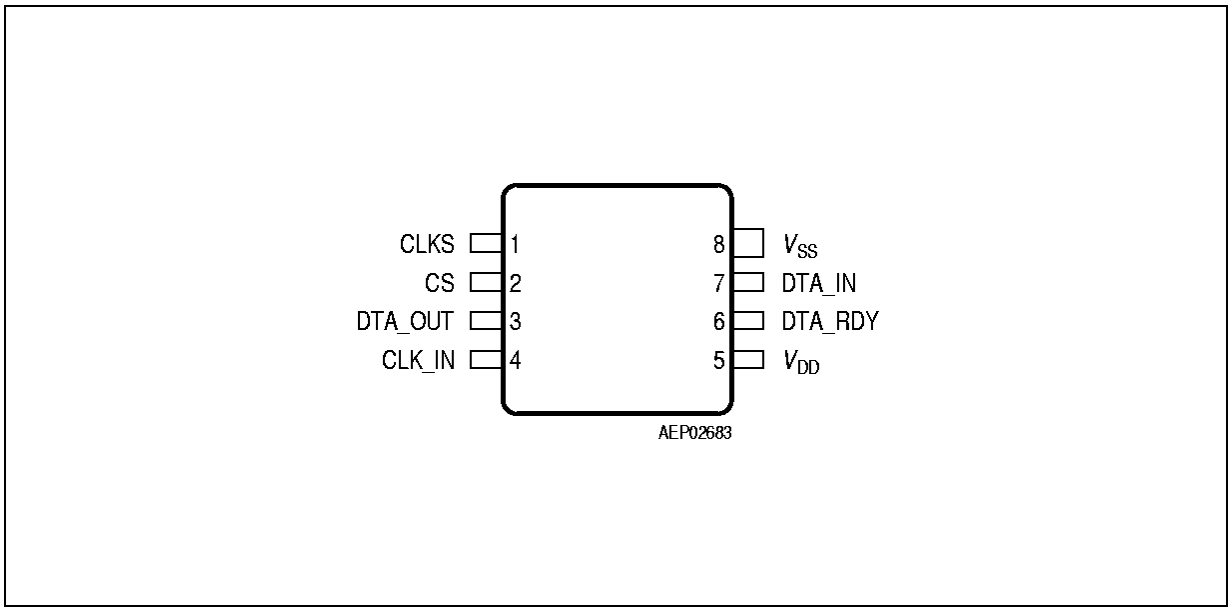


Figure 1

Pin Definitions and Functions

Pad No.	Symbol	Function
1	CLKS	Input; clock for serial interface
2	CS	Input; chip select, active low
3	DTA_OUT	Output of the serial interface
4	CLK_IN	Input; external clock = 4/8 MHz
5	V_{DD}	5 V power supply terminal
6	DTA_RDY	Data ready signal for serial interface
7	DTA_IN	Input for serial interface
8	V_{SS}	Ground potential

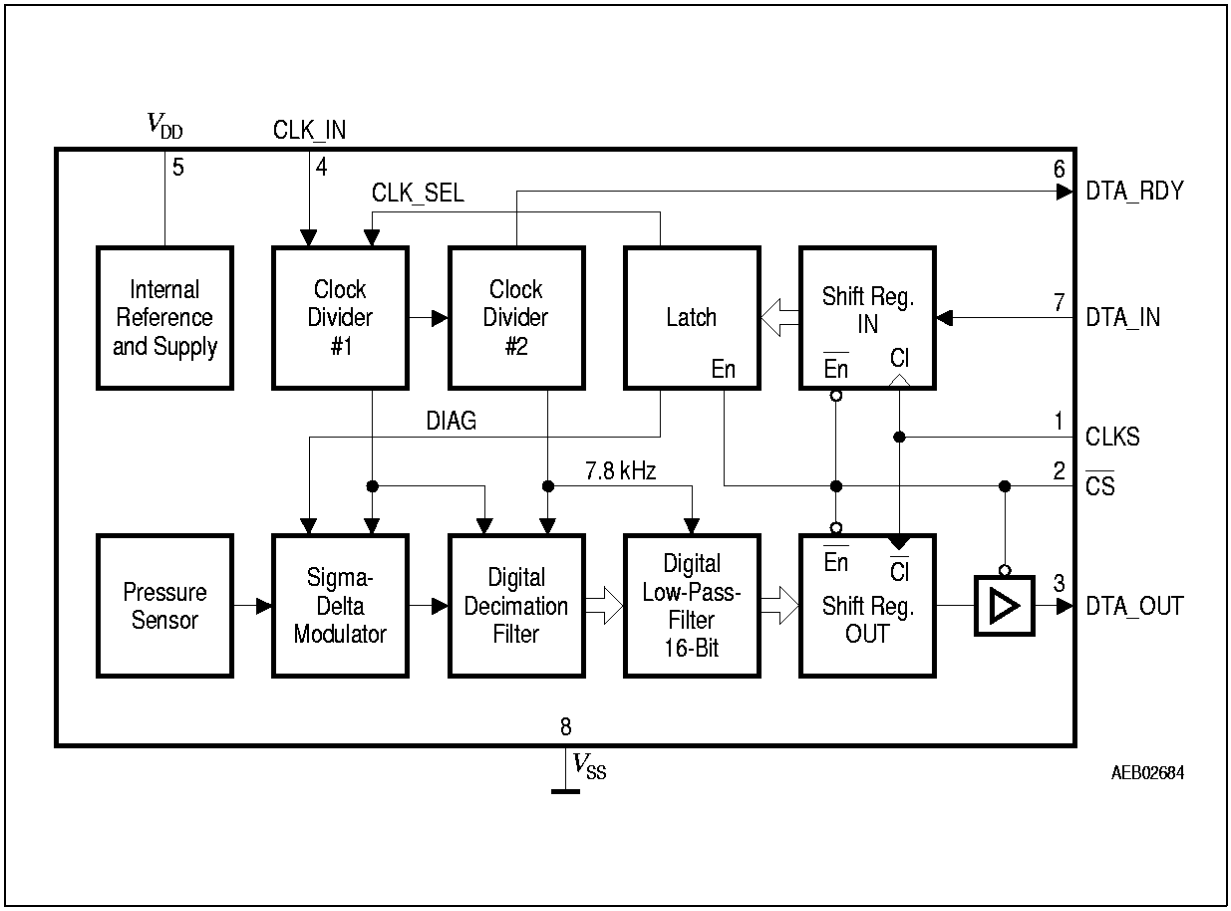


Figure 2 Block Diagram of the KP100

Functional Description

The IC consists of a surface micromachined pressure sensor, a sigma-delta A/D-converter, a digital filter and the SPI-interface. In normal operation, the applied pressure has to be in the range between 60 kPa and 130 kPa and delivers output codes between typ. 7680 and typ. 20190 digits.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Clock Oscillator					
Voltage on pin CLK_IN	V_{CLK_IN}	– 0.3	–	V_{DD}+0.3	V
Current on pin CLK_IN	I_{CKL_IN}	– 100	–	100	µA
Serial Peripheral Interface (SPI)					
Input voltage on pins CLKS, CS and DTA_IN	V_{CLKS} V_{CS} V_{DTA_IN}	– 0.3	–	V_{DD}+0.3	V
Current on pins CLKS, CS, DTA_IN	I_{CLKS} I_{CS} I_{DTA_IN}	– 1.0	–	1.0	mA
Temperature					
Storage temperature	T_S	– 40	–	90	°C
Junction temperature	T_j	– 40	–	100	°C
Pressure					
Pressure overload	p_{OL}	–	–	200	kPa

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Protection

Human Body Model (HBM) tests according to:
Standard EIA/JESD22-A114-B HBM (covers MIL STD 883D)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
ESD-Protection	V_{ESD}	–	± 2	kV	R = 1.5 kΩ, C = 100 pF

Operating Range

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Supply current	I_{DD}	1.0	1.8	2.5	mA
External clock frequency CLK_IN	f_{CLK_IN}	–	4/8	4.2/8.4	MHz
Operating temperature range	T_A	– 40	–	+ 90	°C
Pressure range	R_P	60	–	130	kPa

Electrical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Digital output range	R_Y	0	–	65534	digits
Resolution	–	–	2	–	digits
Output range for a typ. sensitivity (value see below) over specified pressure range (for zero offset, at 25 °C)	Y	7680	–	20190	digits
Offset The offset is written on the package in an encoded Form, called LC (calculation see below)	a LC	– 3000 00	–	6984 TT	digits
Sensitivity (see below: transfer function)	b	–	46	–	digits/ $(kPa)^{1.25}$
Exponent of transfer function (see below)	c	–	1.25	–	1
Repeatability		–	16	–	digits
Noise	σ	–	–	14.5	digits
Information rate	f_L	–	7.8	–	kHz
Filter cutoff frequency (– 3 dB)	$f_{-3\,dB}$	–	360	–	Hz
Accuracy over temperature range (-40 °C to 90 °C)	ε	–	± 5%	–	1

***Calculation of the offset a from the LC-code written on the package**

The offset of each pressure sensor is individually measured at the Infineon production line. It is written on the sensor package in encoded Form. The so called LC code consists of two signs X and Y. The offset a is calculated from the code using the table and the formula below:

$$a = (X \times 25 + Y) \times 16 - 3000$$

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
0	1	2	3	4	5	6	7	8	9	A	V	C	D	E	F	G	H	K	L	M	P	R	S	T

Electrical Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input pin CLK_IN					
Input capacitance	C_{CKL_IN}	–	–	5	pF
Input current	I_{CKL_IN}	– 5	–	5	µA
Input high voltage	V_{HCKL_IN}	3.5	–	–	V
Input low voltage	V_{LCKL_IN}	–	–	1.5	V
Input hysteresis	V_{INHYST}	150	–	–	mV
“H” output voltage on pins DTA_OUT, DTA_RDY I_{OH} = – 1 mA	V_{OH}	0.8 V_{DD}	–	–	V
“L” output voltage on pins DTA_OUT, DTA_RDY I_{OL} = + 1 mA	V_{LH}	–	–	0.1 V_{DD}	V
“H” input current on pin CLKS	I_{IH}	–	–	50	µA
“L” input current on pin CLKS	I_{IL}	– 200	–	–	µA
“H” input current on pin DTA_IN	I_{IH}	–	–	200	µA
“L” input current on pin DTA_IN	I_{IL}	– 50	–	–	µA
“H” input current on pin CS	I_{IH}	–	–	50	µA
“L” input current on pin CS	I_{IL}	– 200	–	–	µA

Electrical Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input voltage HIGH level CLKS, CS, DTA_IN	V_{IH}	4.0	–	–	V
Input voltage LOW level CLKS, CS, DTA_IN	V_{IL}	–	–	1.0	V
Input hysteresis on pins CLKS, CS, DTA_IN	$V_{OH} - V_{LH}$	–	0.5	–	V

SPI Timing Tolerances

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
CS lead time	t_{lead}	250	–	–	ns
CS lag time	t_{lag}	250	–	–	ns
CLKS "H" pulse width	t_{WH}	880	–	–	ns
CLKS "L" pulse width	t_{WL}	880	–	–	ns
DTA_IN setup time at pin DTA_IN	t_{SU}	200	–	–	ns
DTA_IN hold time at pin DTA_IN	t_{H}	200	–	–	ns
DTA_OUT output delay time at pin DTA_OUT	t_{D}	–	–	200	ns
Clock frequency CLKS	f_{CLKS}	–	–	500	kHz
Clock cycle time	t_{C}	2	–	–	µs
DTA_OUT TRI-STATE® delay time	t_{Z}	–	–	200	ns
DTA-RDY Timing					
DTA_RDY cycle time	t_{CDR}	–	128	–	µs
DTA_RDY pulse width	t_{WDR}	–	16	–	µs
DTA_OUT status valid setup time	t_{SUDO}	–	–	1	µs
DTA_OUT status valid delay time	t_{DO}	–	–	1	µs
DTA_RDY fall time	t_{FDR}	–	–	100	ns
DTA_RDY rise time	t_{RDR}	–	–	200	ns

Transfer Function

The general relation between output code and pressure is given by the formula

$$Y(p) = a + b \cdot \left[\frac{p}{kPa}\right]^c \qquad [digit]$$

Interface description

The KP100 digital interface consists of the pins DTA_IN, CLKS, DTA_OUT, CS and DTA_RDY. The interface is active when CS is low.

At the DTA_RDY pin a pulse of approx. 16 µs appears with a frequency of 7.8 kHz. The rising edge of this pulse indicates that the output register has been loaded with a new 16 bit wide data word, where the first bit is a parity bit. The data can then be clocked out by applying a clock signal at CLKS. With every falling edge of CLKS the DTA_OUT is updated, starting with the parity, followed by the LSB. After the 16th falling edge the MSB appears at DTA_OUT and the readout cycle is completed.

Simultaneously data can be loaded into the KP100 via DTA_IN. The data is clocked in with every rising edge at CLKS. Only the three last bits of the input data are relevant. They are used to select the diagnosis modes and to switch between 4 and 8 MHz operation. After completing a read-write cycle the three input bits can be activated by applying a positive pulse at CS of at least 50 µs.

If for example the diagnosis mode 1 has been choosen the corresponding diagnosis value will appear at DTA_OUT in the next read-write cycle.

For the simplest mode of operation the CS and DTA_IN pins are pulled to ground potential. Then only the pins CLKS, DTA_OUT and DTA_RDY are needed to read the pressure data, since the power-on condition of the KP100 is to deliver pressure data in 8 MHz mode.

Read Write Cycle

A complete read write cycle is shown in the diagram below. DTA_RDY and DTA_OUT are KP100 output signals, CLKS, DTA_IN and CS are KP100 input signals. The first 13 DTA_IN bits are don’t care bits.

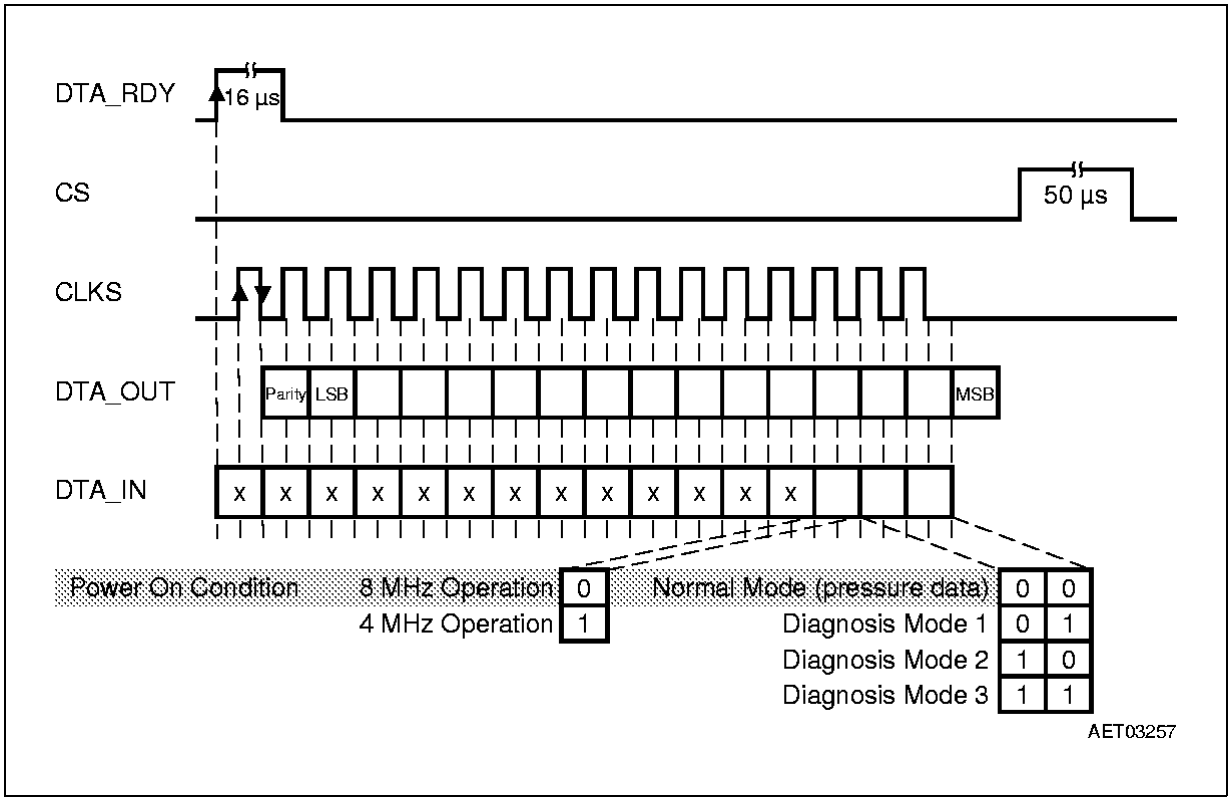


Figure 3

Diagnosis Features

For transmission reliability the first bit of the data word is a parity bit whereas the next 15 bits are data bits starting with the LSB. Parity is odd in normal mode and even in any diagnosis mode. It is calculated only for the 12 MSBs, the first 3 LSBs are ignored.

Besides of the parity bit in the output code there are several additional diagnosis features. In detail these are an automatic fuse-check and three diagnosis modes.

Automatic fuse-check:

Fuses are used for correcting the transfer function between pressure and output code. An additional parity-fuse guarantees that fuse-data is reliable. If a wrong parity is detected the output code will go to FFFFH, which is defined as an error code. The condition is latched, i.e. the error code will be transmitted until the next power on reset.

Diagnosis mode 1:

This mode puts the sigma-delta converter into an idle condition where it operates without input signal. This is a good method to check the basic analog performance of the chip. An output code of 8020H (± 3E8H) is expected.

Diagnosis mode 2:

The sensor array is subdivided into two independent areas. In diagnosis 2 mode the difference signal of the two areas is measured. A drift of the diagnosis 2 value indicates a mechanical damage of one or more cells. For an efficient use of this mode it is recommended to store the initial diagnosis 2 value on the application board (e.g. in the µC flash) already at the production line.

Diagnosis mode 3:

This mode applies a general reset to the chip and initiates a special self-test sequence, where the complete digital filter part is checked. After programming the diagnosis 3 mode and activating it by a high-pulse at CS, the following 10 read write cycles must deliver the output values listed below:

Number	1	2	3	4	5	6	7	8	9	10
Output value (hex)	0000	0000	0000	0000	0900	25E6	4E8D	741B	9135	A664

Note that between these 10 read-write cycles no further CS pulse must be applyed, in order not to end or to restart the diagnosis 3 mode. Also note that no DTA_RDY must be skipped in this mode, since each value will be overwritten by the subsequent value.

Any error in these codes indicates an error in the digital circuitry of the chip.

Additionally, this diagnosis mode also resets the fuse-check latch. However, a remaining error conditiotion in the fuses will immediately reestablish this latch, so that the output is set to FFFFH.

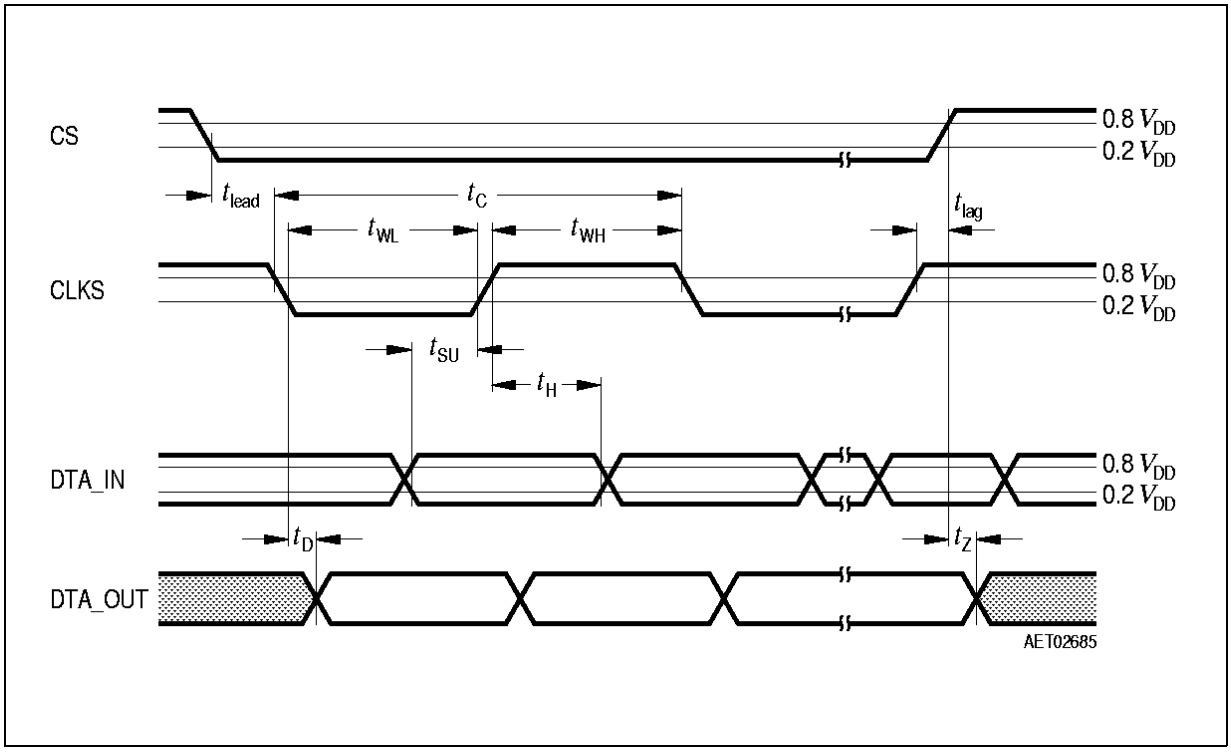


Figure 4 Serial Peripheral Interface: Timing Diagram

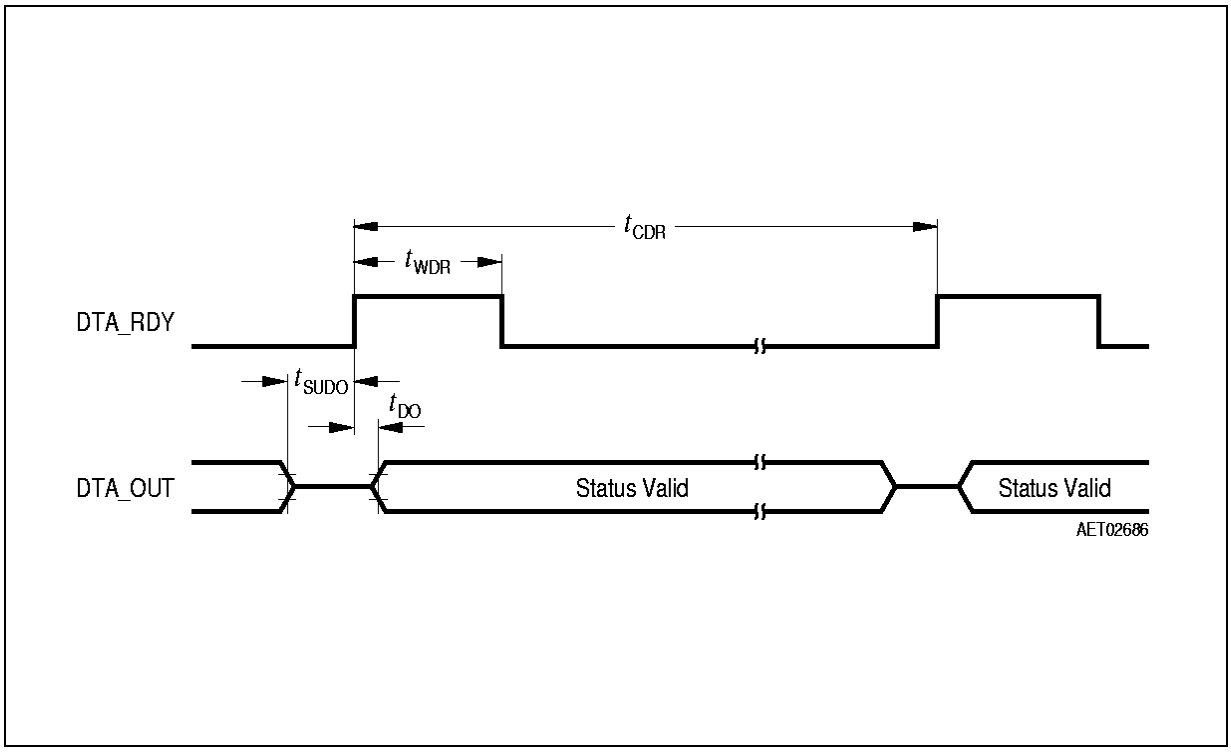


Figure 5 DTA_RDY Timing Diagram

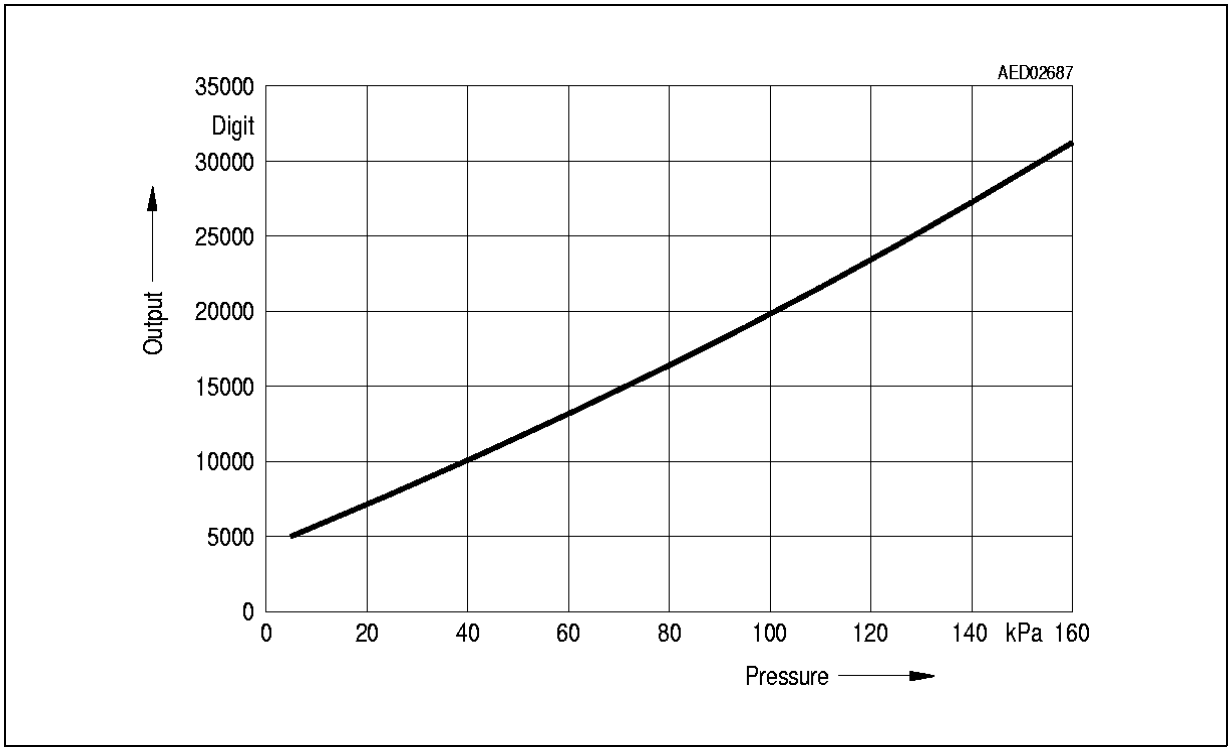
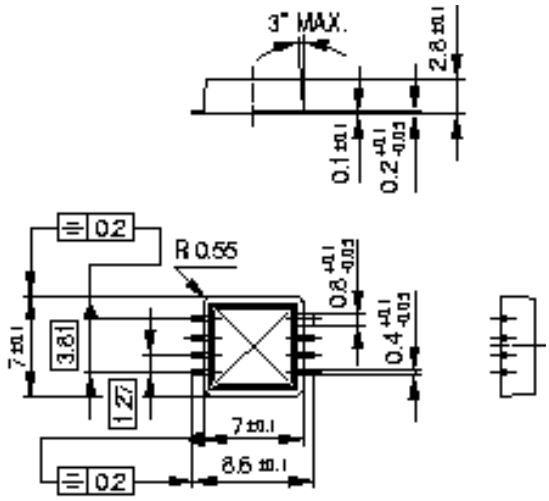


Figure 6 Transfer Function

Package Outlines

P-DSOF-8-3
(Plastic Dual Small Outline Flat Package)



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Dimensions in mm