T-51-09-12

Monolithic D/A Converter
12-Bit, 50Msps
12ns Settling Time to 0.1%, 70dB SFDR

The TDC1112 is an ECL compatible, 12-bit monolithic D/A converter capable of converting digital data into an analog current at data rates in excess of 50Msps (MegaSample Per Second).

The analog performance has been optimized for dynamic performance, with very low glitch energy. The output is able to drive a 50Ω load with 1V outputs while keeping a spurious-free-dynamic range greater than 70dB.

Data registers are incorporated on the chip. This eliminates the temporal data skew encountered with external registers and latches and minimizes the glitches that can adversely affect many applications.

Features

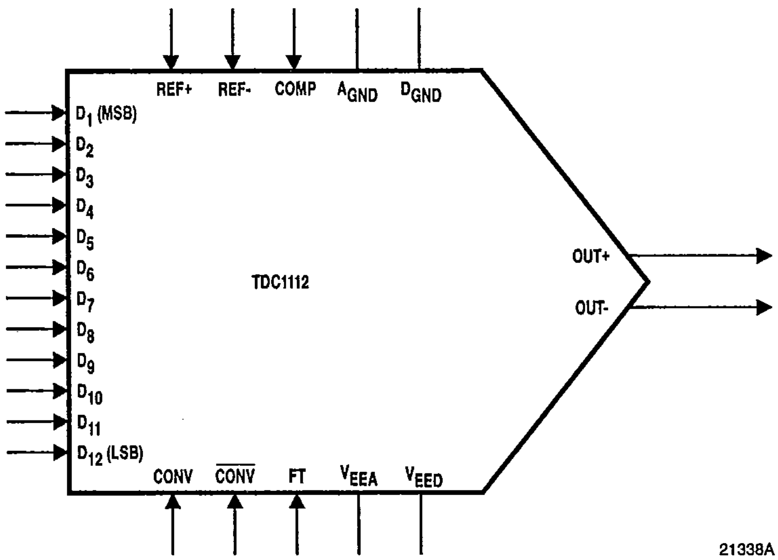
- 12-Bit Resolution
- 50Msps Data Rate
- ECL Inputs
- Very Low Glitch – No Track And Hold Circuit Needed
- Dual +4dBm (1V Into 50Ω) Outputs Make Output Amplifiers Unnecessary In Many Applications
- 70dB Typical Spurious-Free-Dynamic-Range
- Available Compliant To MIL-STD-883C

Applications

- Direct Digital RF Signal Generation
- Test Signal Generation
- Arbitrary Waveform Synthesis
- Broadcast And Studio Video
- High-Resolution A/D Converters

B

Interface Diagram



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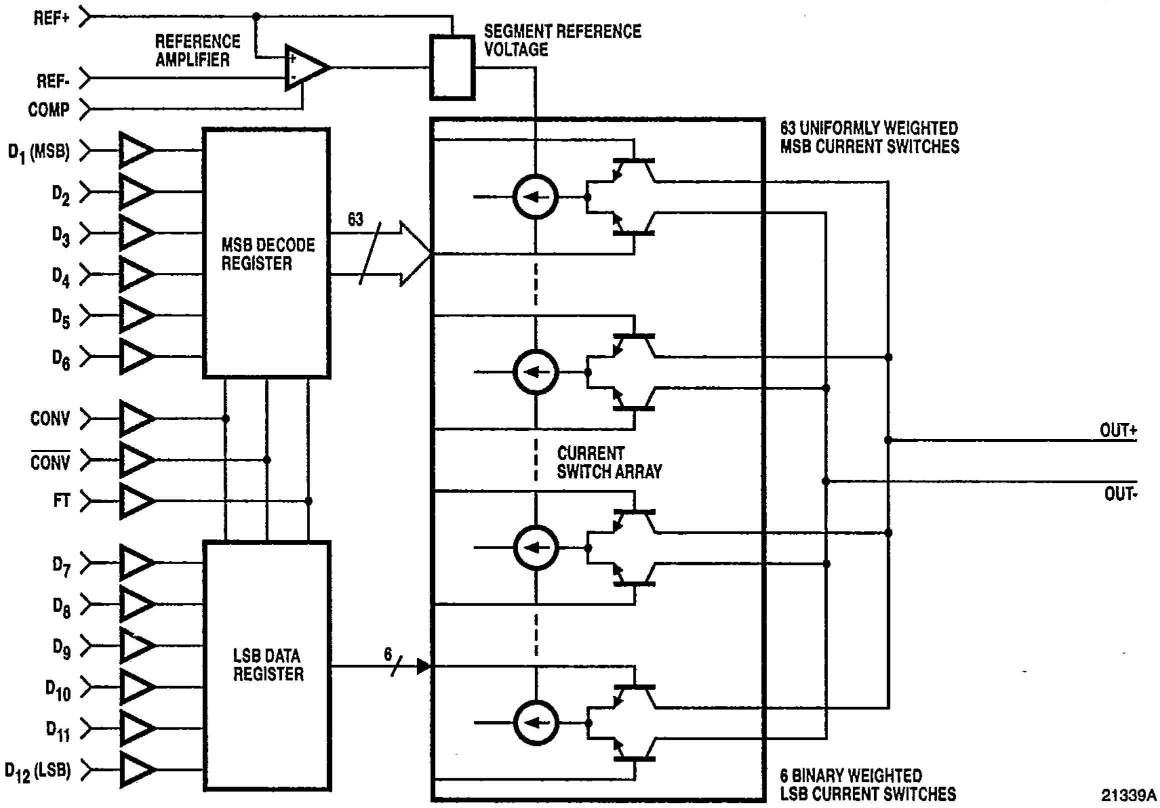
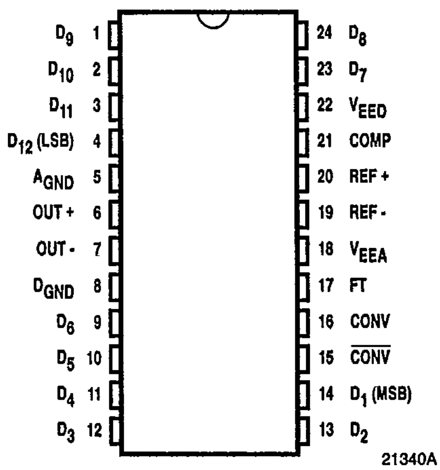
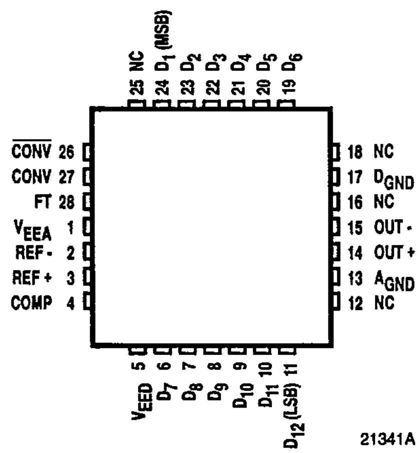
Functional Block Diagram



Pin Assignments



24 Pin Hermetic Ceramic DIP – J7 Package
24 Pin Plastic DIP – N7 Package



28 Contact Chip Carrier – C3 Package
28 Leaded Plastic Chip Carrier – R3 Package

Functional Description

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General Information

The TDC1112 consists of five major circuit sections: the LSB data register, the MSB decode block, the decoded MSB register, the current switch array, and the reference amplifier. All data bits are registered just before the current switches to minimize the temporal skew that would generate glitches.

There are three major D/A architectures: thermometer code segmentation, weighted current sources, and R−2R. In thermometer code segmentation there is one current source for each possible output level. The current sources are equally weighted and for an input code of N, N current sources are turned on. An N bit segmented D/A has 2^N current sources. A weighted current source D/A has one current source for each bit of input with a binary weighting for the current sources. In an R−2R D/A, there is one current source per bit, and a resistor network which scales the current sources to have a binary weighting.

When transitioning from a code of 011111111111 to 100000000000, both the R−2R D/A and binary weighted D/A are turning some current sources on while turning others off. If the timing is not perfect, there is a moment where all current sources are either on or off, resulting in a glitch. In a segmented architecture, 2047 of the current sources remain on, and one more is turned on to increment the output-no possibility of a glitch.

The TDC1112 uses a hybrid architecture with the 6 MSBs segmented, and the 6 LSBs from a R−2R network. The result is a converter which has very low glitch energy, and a moderate die size.

Power, Grounds, and Layout

The TDC1112 requires a single −5.2V power supply. The analog (V_{EEA}) and digital (V_{EED}) supply voltages should be decoupled from each other, as shown in the *Typical Interface Circuits*, to provide the highest noise immunity. The 0.1µF decoupling capacitors should be placed as close as possible to the power pins. The inductors are simple ferrite beads and are neither critical in value nor always required.

The high slew-rates of digital data make capacitive coupling with the D/A output a real problem. Since the digital signals contain high-frequency harmonics of the clock, as well as the signal that is being provided to the DAC, the result of data feedthrough often looks like harmonic distortion which degrades the Spurious-Free-Dynamic-Range (SFDR) performance of the D/A.

The layout of grounds in any system is an important design consideration. Separate analog and digital grounds are provided at the TDC1112. All ground pins should be connected to a common low-noise, low-impedance groundplane. This groundplane should be common for the TDC1112 and all of its immediate interface circuitry, which includes all of the reference circuitry, the output load circuitry, and all of the power supply decoupling components.

The digital driving logic should use a separate system ground, and this ground should be connected (typically through a ferrite bead inductor) to the analog groundplane in only one place. The analog and digital grounds may be connected in other ways if required by the user's system grounding plan, however, the voltage differential between the A_{GND} and D_{GND} pins must be held to within ±0.1V.

Reference

The TDC1112 has two reference inputs: REF+ and REF−. These are the inverting and noninverting inputs of the internal reference amplifier. An externally generated reference voltage is applied to the REF− pin. Current flows into the REF+ pin through an external current setting resistor (R_{REF}). This current is the reference current (I_{REF}) which serves as an internal reference for the current source array. The output current for an input code N from OUT+ is related to I_{REF} through the following relationship:

$$I_{OUT}\,(\text{Input Code N}) = N \times \frac{I_{REF}}{64}$$

This means that with an I_{REF} that is nominally 625µA, the full scale output is 40mA, which will drive a 50Ω load in parallel with a 50Ω transmission line (25Ω load total) with a 1V peak-to-peak signal. The impedance seen by the REF− and REF+ pins should be approximately equal so that the effect of amplifier input bias current is minimized.

Reference (cont.)

The TDC1112 has been optimized to operate with a reference current of 625µA. Significantly increasing or decreasing this current may degrade the performance of the device. The minimum and maximum values for V_{REF} and I_{REF} are listed in the *Operating Conditions Table*.

The internal reference amplifier is externally compensated to assure stability. To compensate this amplifier, a 0.1µF capacitor should be connected between the COMP pin and V_{EEA}. The amplifier has been optimized to minimize the TDC1112 settling time, and as a result should be considered a DC amplifier. Performance of the TDC1112 operating in a multiplying D/A mode is not guaranteed.

A typical interface circuit that includes a stable, adjustable reference circuit is shown in *Figures 9a-c*.

Digital Inputs

The data inputs are single-ended ECL compatible. The TDC1112 is specified with two sets of setup and hold times. One of these pairs of specifications guarantees the performance of the TDC1112 to specifications listed in the minimum and maximum columns of the *System Performance Characteristics Table*. The second more rigid specification is recommended for applications where lowest possible glitch and highest SFDR are desired. The more stringent t_S and t_H insure that the data will not be slewing during times critical to the TDC1112, and will hence minimize the effects of capacitively coupled data feedthrough and optimize SFDR performance. Another method reducing the effect of capacitive coupling is to slow down the slew rates of the digital inputs. This has been done in the circuit shown in *Figures 9a-c* by the addition of 50Ω series resistors to the data lines.

Clock and Feedthrough Control

The TDC1112 requires an ECL clock signal (CONVert and $\overline{\text{CONVert}}$). Even though complementary operation is preferred, a single-ended signal may be used if either unused CONV input is biased at a DC voltage midway between the active input's V_{IH} and V_{IL} levels.

Data is synchronously entered on the rising edge of CONV (the falling edge of $\overline{\text{CONV}}$). The CONV input is ignored in the Feedthrough (FT=HIGH) mode.

The Feedthrough (FT) pin is normally held LOW, in which case the TDC1112 operates in a clocked mode (the output changes only after a clock rising edge). An internal pull-down resistor is provided, and this pin may be left open for clocked operation. For certain applications, such as high-precision successive approximation A/D converters, speed may be more important then glitch performance. In these cases, the FT pin may be brought HIGH, which makes the input registers transparent. This allows the analog output to change immediately and asynchronous in response to the digital input, without the need for a clock.

Since skew in the bits of the input word will result in glitches, and may affect settling time, it is recommended that the TDC1112 be operated in clocked mode for most applications.

Analog Outputs

Two simultaneous and complementary analog outputs are provided. Both of these outputs are full-power current sources. By loading the current source outputs with a resistive load, they may be used as voltage outputs. OUT+ provides a 0 to −40mA output current (0 to −1V when terminated in 25Ω) as the input code varies from 0000 0000 0000 to 1111 1111 1111. OUT− varies in a complementary manner from −40 to 0mA (−1 to 0V when terminated with 25Ω) over the same code range. (See the *Output Coding Table*.) The output current is proportional to the reference current and the input code.

The recommended output termination is 25Ω. This can be provided by placing a 50Ω source resistor between the output pin and ground, then driving a 50Ω transmission line. With this load, the output voltage range of the converter is 0 to −1.0V. If a load is capacitively coupled to the TDC1112, it is recommended that a 25Ω load at DC, as seen by the TDC1112, continue to be maintained. The output voltage should be kept within the output compliance voltage range, V_{OC}, as specified in the *Electrical Characteristics Table*, or the accuracy may be impaired.

See *Figure 9b* for a suggested circuit for achieving a bipolar output voltage range. Optimum DC linearity is obtained by using a differential output either with a balun, or an operational amplifier in the differential mode. If it is desired that the TDC1112 be operated in a single ended fashion, the unused output should be connected directly to ground as is shown in *Figure 9c*.

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Package Interconnections

Signal Type	Signal Name	Function	Value	J7, N7 Package Pins	C3, R3 Package Pins
Power	V_{EEA}	Analog Supply Voltage	–5.2V	18	1
	V_{EED}	Digital Supply Voltage	–5.2V	22	5
	A_{GND}	Analog Ground	0.0V	5	13
	D_{GND}	Digital Ground	0.0V	8	17
Reference	REF–	Reference Voltage Input	–1.0V	19	2
	REF+	Reference Current Output	–0.625mA	20	3
	COMP	Compensation Capacitor	0.1μF, See Text	21	4
Data Input	D_1 (MSB)	Most Significant Bit Input	ECL	14	24
	D_2		ECL	13	23
	D_3		ECL	12	22
	D_4		ECL	11	21
	D_5		ECL	10	20
	D_6		ECL	9	19
	D_7		ECL	23	6
	D_8		ECL	24	7
	D_9		ECL	1	8
	D_{10}		ECL	2	9
	D_{11}		ECL	3	10
	D_{12} (LSB)	Least Significant Bit Input	ECL	4	11
Feedthrough	FT	Feedthrough Mode Control	ECL	17	28
Convert (Clock)	CONV	Convert (Clock) Input	ECL	16	27
	$\overline{CONV}$	Convert (Clock) Input	ECL	15	26
Analog Output	OUT+	Analog Output	0 to –40mA	6	14
	OUT–	Analog Output	–40 to 0mA	7	15

Output Coding Table [1]

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Input Data MSB	D1-12	LSB	OUT+ (mA)	V_{OUT+} (mV)	OUT− (mA)	V_{OUT-} (mV)
0000	0000	0000	0.000	0.00	40.000	−1000.00
0000	0000	0001	0.009	−0.24	39.990	−999.75
0000	0000	0010	0.019	−0.49	39.980	−999.52
⋮			⋮	⋮	⋮	⋮
0111	1111	1111	19.995	−499.88	20.005	−500.12
1000	0000	0000	20.005	−500.12	19.995	−499.88
⋮			⋮	⋮	⋮	⋮
1111	1111	1101	39.980	−999.52	0.019	−0.49
1111	1111	1110	39.990	−999.75	0.009	−0.24
1111	1111	1111	40.000	−1000.00	0.000	0.00

Note: 1. $I_{REF} = 625\mu A$, $R_{LOAD} = 25\Omega$.

Figure 1. Timing Diagram

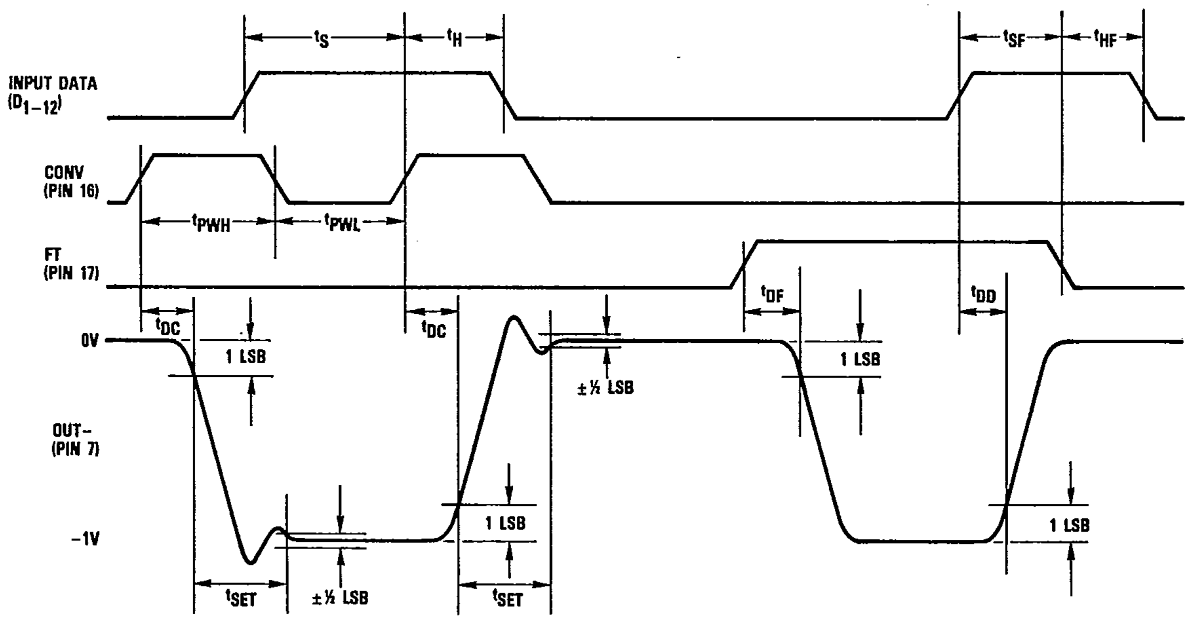

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Figure 2a. Equivalent Input Circuit (Data and FT)

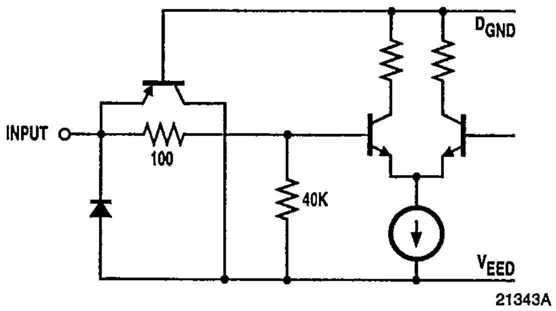


Figure 2b. Equivalent Input Circuit (CONV and $\overline{CONV}$)

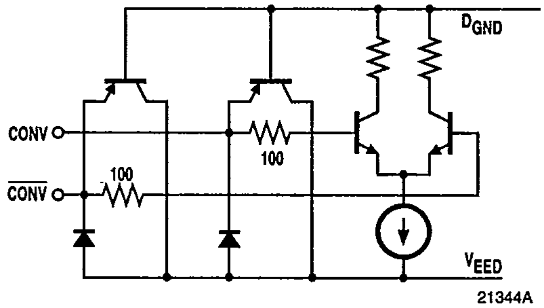


Figure 3. Equivalent Reference and Output Circuits

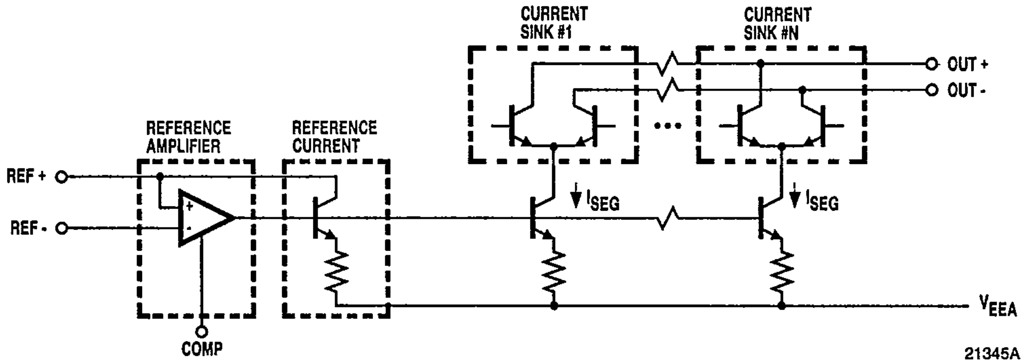


Figure 4. Standard Test Load

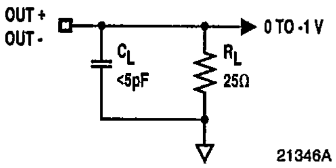
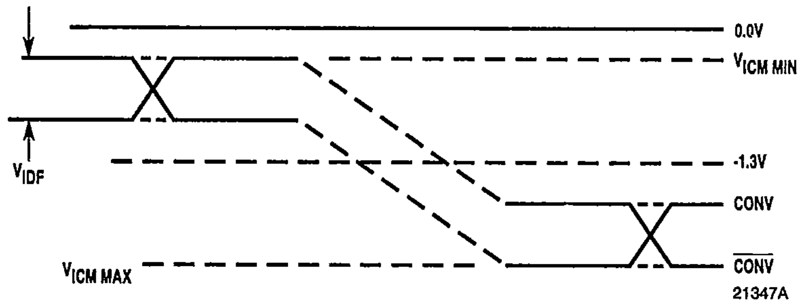


Figure 5. CONV and $\overline{CONV}$ Switching Levels



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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltages		
	V_{EEA} (measured to A_{GND})	−7.0 to +0.5V
	V_{EEA} (measured to V_{EED})	−50 to +50mV
	V_{EED} (measured to D_{GND})	−7.0 to +0.5V
	A_{GND} (measured to D_{GND})	−0.5 to +0.5V
Inputs		
	Applied voltage	
	CONV, $\overline{CONV}$, FT, D_{1-12} (measured to D_{GND}) [2]	V_{EED} to +0.0V
	REF+, REF− (measured to A_{GND}) [2]	V_{EEA} to +0.0V
	Applied current	
	REF+, REF−, externally forced (measured to A_{GND}) [3,4]	±3mA
	Digital inputs	±3mA
Outputs		
	Applied voltage	
	OUT+, OUT− (measured to A_{GND}) [2]	−2.0 to +2.0V
	Applied current	
	OUT+, OUT−, externally forced (measured to A_{GND}) [3,4]	+50mA
	Short-circuit duration (single output to GND)	Unlimited
Temperature		
	Operating, ambient (plastic package)	−20 to +90°C
	(ceramic package)	−60 to +150°C
	junction (plastic package)	+140°C
	(ceramic package)	+200°C
	Lead, soldering (10 seconds)	+300°C
	Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

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Operating conditions

Parameter		Temperature Range						Units
		Commercial			Military			
		Min	Nom	Max	Min	Nom	Max	
F_S	Clock Frequency	0		50	0		50	MHz
V_{EEA}	Analog Supply Voltage (measured to A_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{EEA}	Analog Supply Voltage (measured to V_{EED}) [1]	−20	0.0	+20	−20	0.0	+20	mV
V_{EED}	Digital Supply Voltage (measured to D_{GND})	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	−0.1	0.0	0.1	−0.1	0.0	0.1	V
V_{REF}	Reference Voltage, REF−	−0.7	−1.0	−1.3	−0.7	−1.0	−1.3	V
I_{REF}	Reference Current, REF+	0.550	0.625	0.700	0.575	0.625	0.675	mA
C_C	Compensation Capacitor	0.01	0.1		0.01	0.1		μF
V_{IL}	Digital Input Voltage, Logic LOW			−1.55			−1.60	V
V_{IH}	Digital Input Voltage, Logic HIGH	−1.05			−1.00			V
t_S	Input Data Setup Time	17			18			ns
t_S	Input Data Setup Time [2]	24			24			ns
t_H	Input Data Hold Time	0			0			ns
t_H	Input Data Hold Time [2]	4			4			ns
t_{SF}	Setup Time, Data to FT			7			7	ns
t_{HF}	Hold Time, Data to FT			24			24	ns
V_{ICM}	CONV Input Voltage, Common Mode Range [3]	−0.5		−2.0	−0.5		−2.0	V
V_{IDF}	CONV Input Voltage, Differential [3]	0.4		1.2	0.4		1.2	V
t_{PWL}	CONV Pulse Width LOW							
	≥40Msps	10.5			10.5			ns
	<40Msps	11			11			ns
t_{PWL}	CONV Pulse Width LOW [2]	18			18			ns
t_{PWH}	CONV Pulse Width HIGH							
	≥40Msps	8.0			8.5			ns
	<40Msps	9.0			9.0			ns
t_{PWH}	CONV Pulse Width HIGH [2]	11			11			ns
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Notes:
1. A common power supply, isolated simply with ferrite bead inductors, is recommended for V_{EEA} and V_{EED}. See the Typical Interface Circuits, Figures 9a-c.
2. SFDR sensitive applications.
3. See Figure 5., CONV, CONV Switching Levels.

Electrical characteristics within specified operating conditions [1]

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	Parameter	Test Conditions	Commercial Min	Commercial Max	Military Min	Military Max	Units
I_{EE}	Supply Current ($I_{EEA}+I_{EED}$) [2]	V_{EEA}=Max [3]		−180		−195	mA
		T_A=70 °C		−150			mA
		T_C=125°C				−145	mA
C_{REF}	Reference Input Capacitance	REF+, REF−		15		15	pF
C_I	Digital Input Capacitance	D_{1-12}, FT, CONV, CONV		15		15	pF
I_{IL}	Digital Input Current, Logic LOW	V_{EED}=Max, V_I=−1.85V	−10	200	−10	250	μA
I_{IH}	Digital Input Current, Logic HIGH	V_{EED}=Max, V_I=−0.8V	−10	200	−10	250	μA
I_{IC}	CONV Input Current	V_{EED}=Max, $-1.85V < V_I < -0.8V$		50		50	μA
R_O	Output Resistance	OUT+, OUT−	12		12		kOhms
C_O	Output Capacitance	OUT+, OUT−		45		45	pF
V_{OC}	Output Compliance Voltage	OUT+, OUT−	−1.2	+1.2	−1.2	+1.2	V
I_O	Full-Scale Output Current	OUT+, OUT−	40		40		mA

Notes:
1. Worst case over all data and control states.
2. See the Typical Supply Current vs. Temperature graph (Figure 6) for typical values.
3. Standard test load, Figure 4.

Switching characteristics within specified operating conditions

	Parameter	Test Conditions	Commercial Min	Commercial Typ	Commercial Max	Military Min	Military Typ	Military Max	Units
F_S	Maximum Clock Rate [1,2,3]	V_{EEA}, V_{EED}=Min, FT=LOW	50			50			Msps
t_{DC}	Clock to Output Delay [2,3]	V_{EEA}, V_{EED}=Min, FT=LOW			20			20	ns
t_{DD}	Data to Output Delay [2,4]	V_{EEA}, V_{EED}=Min, FT=HIGH			25			25	ns
t_{DF}	FT to Output Delay [2]	V_{EEA}, V_{EED}=Min			30			30	ns
t_R	Output Risetime [3]	90% to 10% of FSR, FT=LOW		2	4		2	4	ns
t_F	Output Falltime [3]	10% to 90% of FSR, FT=LOW		2	4		2	4	ns
t_{SET}	Output Voltage Settling Time [2,5,6]	FT=LOW, Worst Case Full-Scale Voltage Transition on OUT− to 0.1% FS (4 LSB or 10 Bits)		12	20		13		ns
		to 0.05% FS (2 LSB)		17			14		ns
		to 0.0188% FS (3/4 LSB)		20	30		18	35	ns
		to 0.0125% FS (1/2 LSB)		25	35		25		ns

Notes:
1. F_S is limited only by t_{PWL}, t_{PWH}, t_S and t_H requirements.
2. See Figure 1., Timing Diagram.
3. Clock Mode.
4. Feedthrough Mode.
5. Standard test load, Figure 4.
6. See the Typical Output Voltage Settling Time vs. Settling Accuracy curve.

System performance characteristics within specified operating conditions

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Parameter		Test Conditions	Commercial Min	Commercial Typ	Commercial Max	Military Min	Military Typ	Military Max	Units
E_{LI}	Linearity Error, Integral (Terminal Based)	Note 1,							
		TDC1112			±0.096			±0.096	%
		TDC1112-1			±0.048			±0.048	%
		TDC1112-2			±0.048			±0.048	%
		TDC1112-3			±0.024			±0.024	%
E_{LD}	Linearity Error, Differential	Note 1,							
		TDC1112			±0.096			±0.096	%
		TDC1112-1			±0.048			±0.048	%
		TDC1112-2			±0.024			±0.024	%
		TDC1112-3			±0.012			±0.012	%
SFDR	Spurious-Free Dynamic Range [2]	32Msps,							
		F_{OUT}=12MHz	55	67			67		dB
		F_{OUT}=10MHz		68		54	68		dB
		40Msps,							
		F_{OUT}=16MHz		63			63		dB
		F_{OUT}=5MHz		70			70		dB
		F_{OUT}=1MHz		72			72		dB
E_G	Absolute Gain Error	Note 3		±1	±5		±1	±5	%
TC_{EG}	Gain Error Temperature Coefficient	Note 3		±30			±30		ppm/°C
I_{OF}	Output Offset Current	Note 4		±0.1	±5		±0.1	±5	μA
TC_{OF}	Offset Temperature Coefficient	Note 5		±2			±2		μV/°C
V_{OS}	REF+ to REF- Offset Voltage			±1.5	±10		±1.5	±10	mV
I_B	REF- Input Bias Current				5			10	μA
PSRR	Power Supply Rejection Ratio	Note 6			-50			-48	dB
PSS	Power Supply Sensitivity	Note 7			-140			-140	μA/V
DP	Differential Phase	Note 8		0.2					Degree
DG	Differential Gain	Note 8		0.3					%
G_A	Peak Glitch Area [9]	FT=LOW		20	35		20	45	pV-sec

Notes:
1. OUT- connected to A_{GND}. OUT- driving virtual ground. V_{EEA}, V_{EED}, I_{REF}=Nom.
2. Circuit as shown in Figure 9a., I_{REF}=Nom.
3. V_{EED}, V_{EEA}, V_{REF}=Nom.
4. V_{EEA}, V_{EED}=Min, D_{1-12}=LOW.
5. V_{EEA}, V_{EED}=Max, D_{1-12}=LOW.
6. 120Hz, 0.6Vp-p ripple on V_{EEA} and V_{EED}. dB relative to 0.6Vp-p ripple input. V_{EEA}, V_{EED}, I_{REF}=Nom.
7. V_{EEA}, V_{EED}=±4%, I_{REF}=Nom.
8. F_S=4 x NTSC Subcarrier.
9. Worst case 1 LSB transition.

Typical Performance Curves (Typical Settling Time Characteristics)

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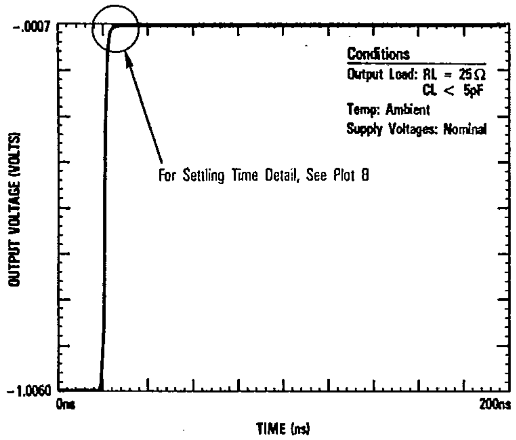
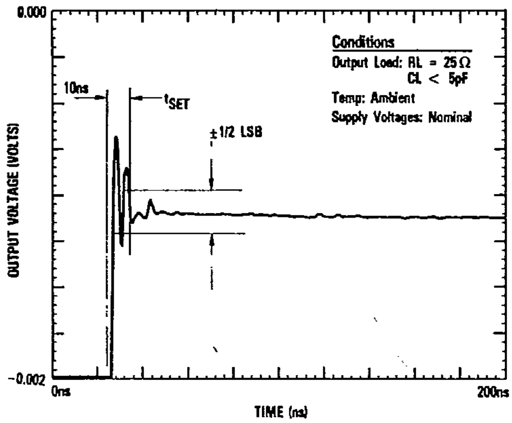
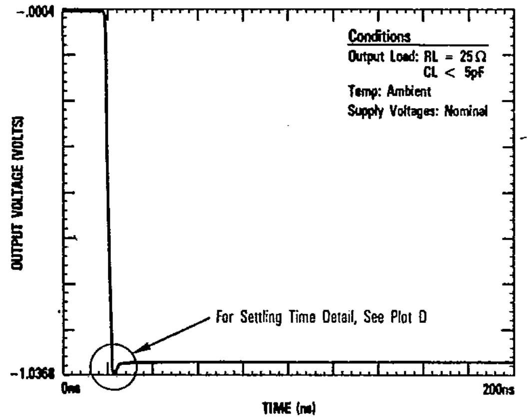
A. Full-Scale Output Transition, Rising Edge



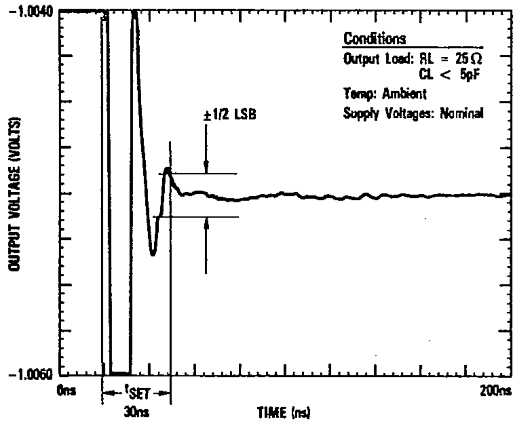
B. Settling Time, Full-Scale Output, Rising Edge



C. Full-Scale Output Transition, Falling Edge



D. Settling Time, Full-Scale Output, Falling Edge



E. Typical Settling Time vs. Settling Accuracy

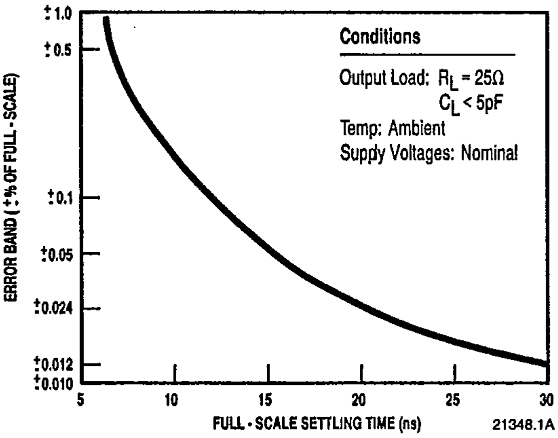


Figure 6. Typical Supply Current vs. Temperature

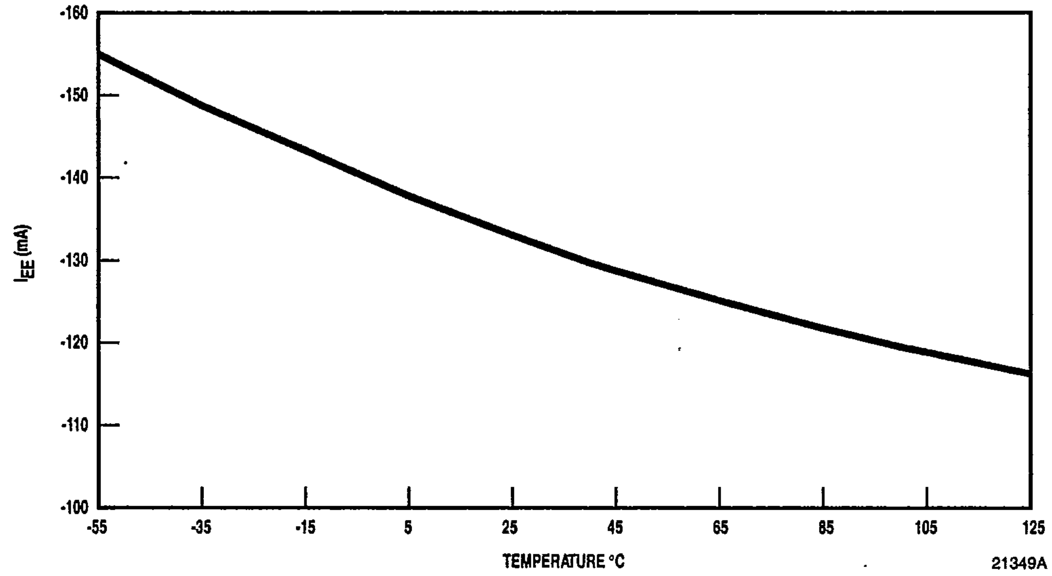


Figure 7. Typical Output Spectrum, 40MSPS, 13.336MHz F_{OUT}

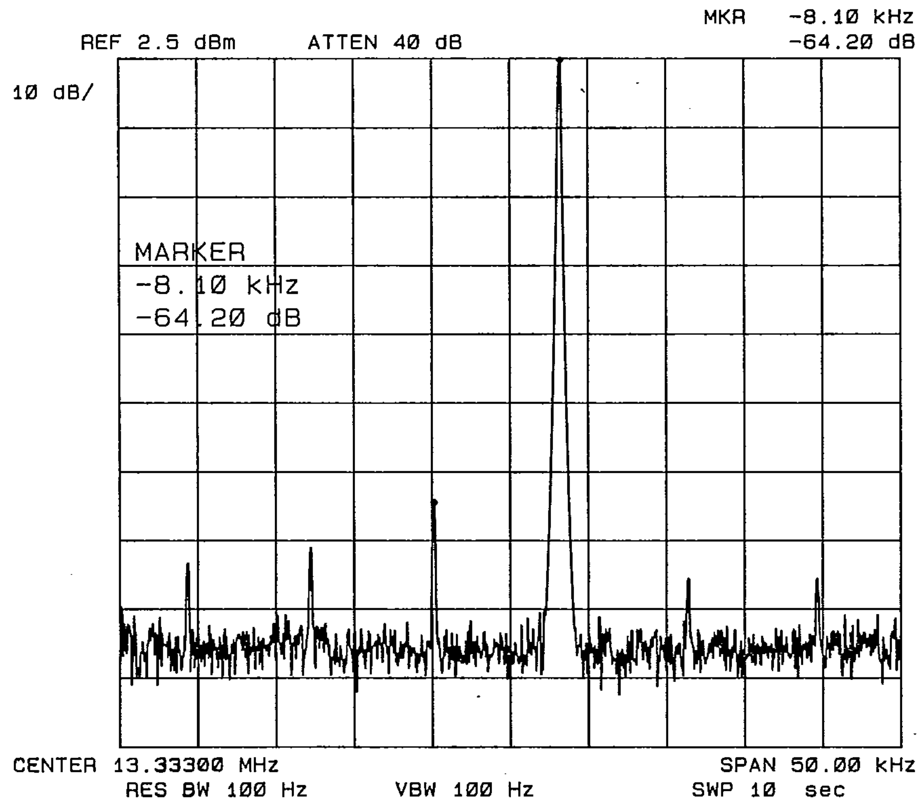
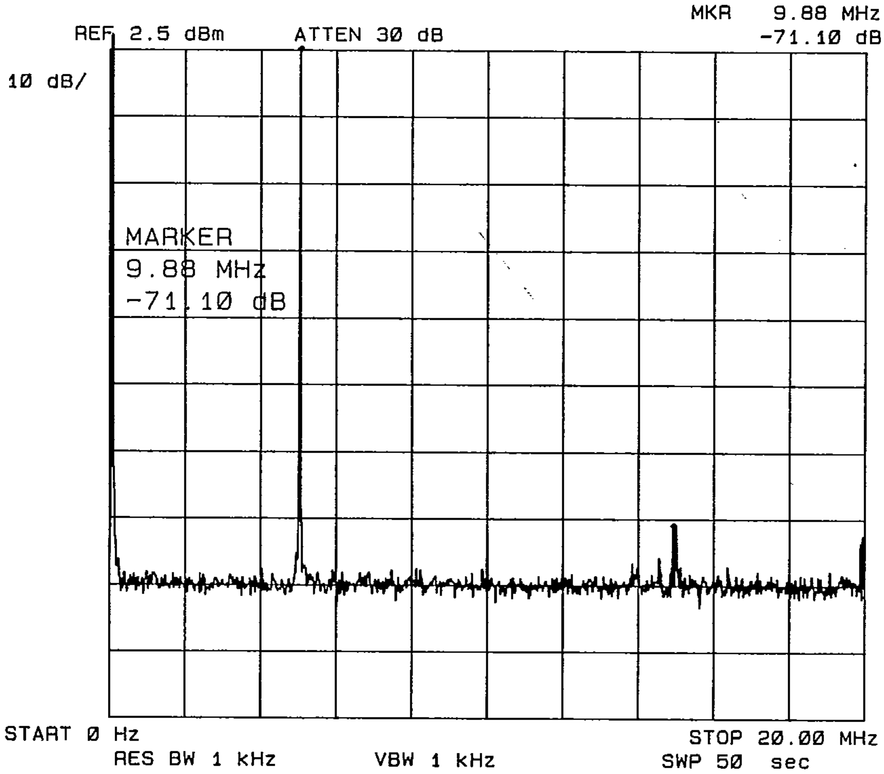


Figure 8. Typical Output Spectrum, 40Msps, 5MHz F_{OUT}



Application Discussion

Direct Digital Synthesis Applications

For most synthesis applications, optimum signal purity is obtained with the use of a balun (a simple RF transformer made by wrapping a few turns of wire around a ferrite core) as shown in *Figure 9a*. This configuration has the benefit of cancelling common mode distortion.

An output amplifier is not recommended because any amplifier will add extra distortion of its own, which is likely to be much greater than that present from the direct outputs of the TDC1112.

The strict adherence to at least the minimum input data setup and hold times is important for the realization of the optimal performance. Spur levels may decrease as setup and hold times are increased. It is possible to achieve even higher performance in some instances by carefully "tuning" the input data setup and hold times (slightly delaying or advancing the CONV signal in relation to the data) fed to the TDC1112. The *Operating Conditions Table* has two sets of data for t_S and t_H, one which guarantees performance of the device in most applications, and one, more conservative specification which has been found to be optimal for DDS applications.

The actual digital-data waveform which represents a sine wave contains strong harmonics of that sinewave. This can be seen by connecting a digital data line to the input of an analog spectrum analyzer. Therefore, data feedthrough to the analog output of a system due to improper board layout or system shielding and grounding will appear as additional harmonic distortion, adversely affecting SFDR.

Harmonic distortion may improve even further with reduced AC termination impedance values, at the expense of lowered output voltage.

The purity of the output of the TDC1112 is greater than that which can be measured by many spectrum analyzers.

Direct Digital Synthesis Applications (cont.)

The spectral plots shown in *Figures 7 and 8* were generated with an HP8568B, which has a noise floor barely below that of the TDC1112, once the TDC1112 performance has been optimized. When making spectral measurements it is important to remember that the TDC1112 output power is +4dBm, which is greater power than many analyzers are equipped to handle without adding distortion of their own. Accordingly, it may be necessary to introduce an attenuator to the input of the spectrum analyzer to see the true DAC performance.

The CONV signal provided to the TDC1112 must be as free from clock jitter as possible. Clock jitter is the random cycle-to-cycle variation in clock period. CONV clock jitter will effectively appear at the output as phase noise. A value of 10ps or less for clock jitter is recommended for the highest performance applications. Ordinary crystal oscillators are satisfactory. High-performance synthesizers, such as the HP8662, used to trigger a precision pulse generator, are also satisfactory, although not as jitter free as a crystal oscillator.

Figure 9a. Typical Interface Circuit with Balun Output

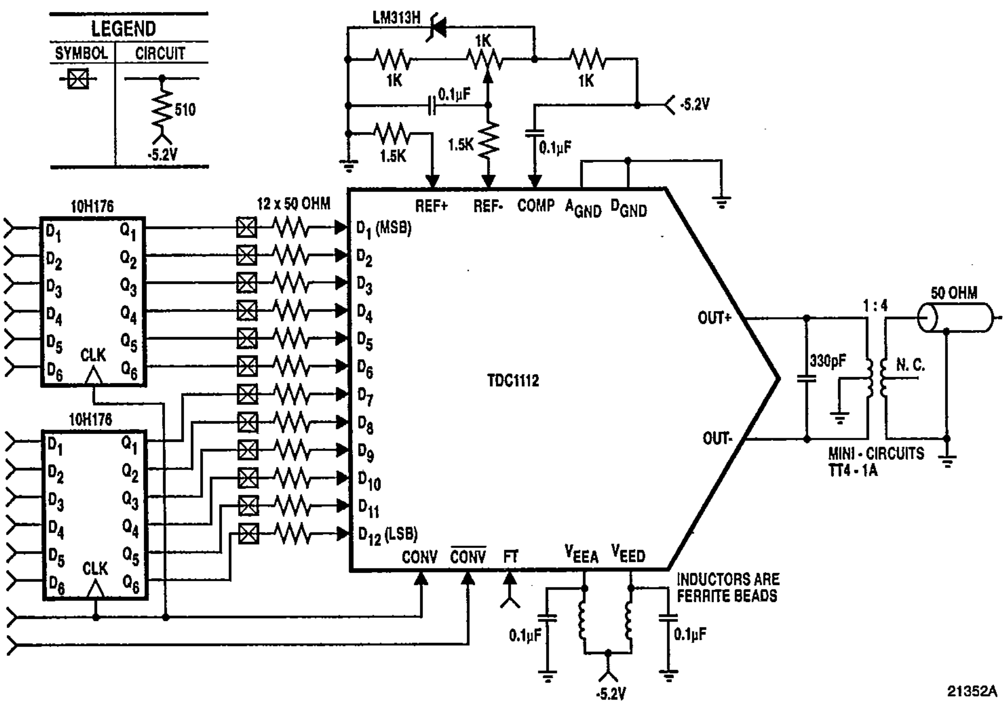


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Figure 9b. Typical Interface Circuit with Bipolar, Differential Mode Operational Amplifier Output

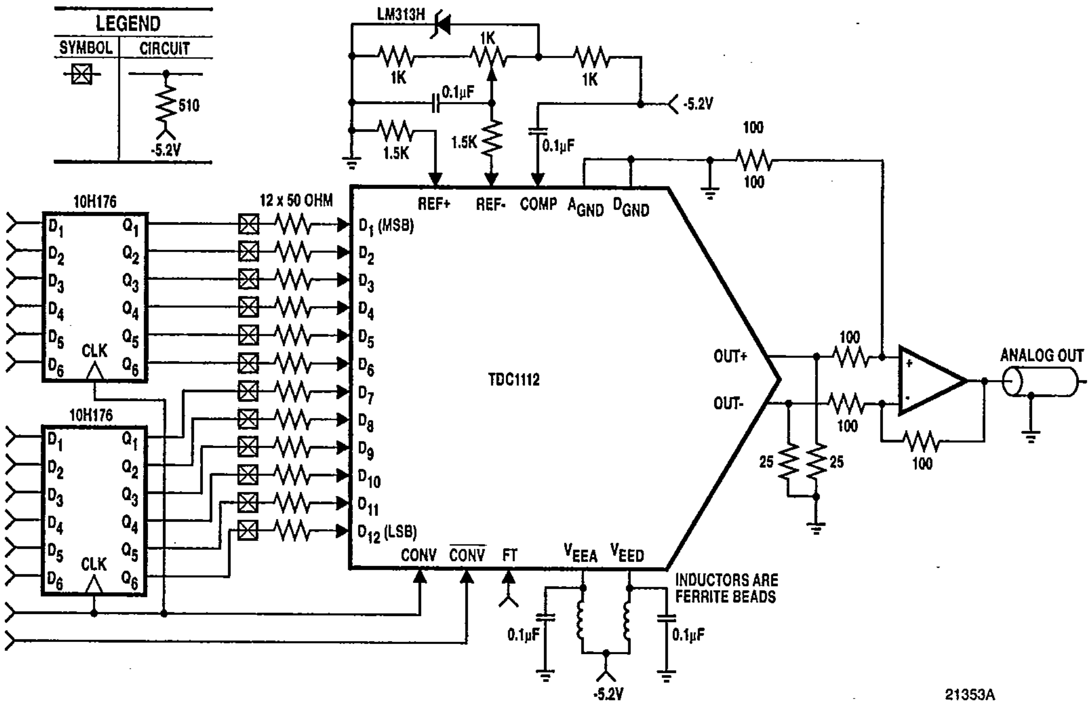
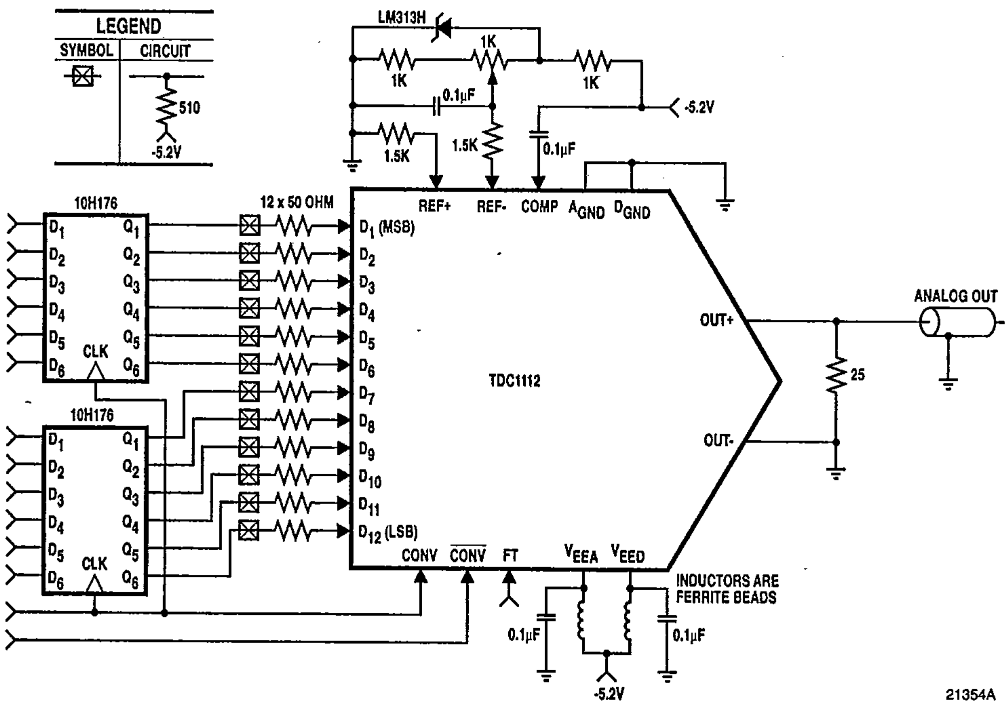


Figure 9c. Typical Interface Circuit with Resistive Load Output



Ordering Information

T-51-09-12

Product [1] Number	Temperature Range	Screening	Package	Package [1] Marking
TDC1112J7CX	STD – T_A = 0°C to 70°C	Commercial	24 Pin Hermetic Ceramic DIP	1112J7C-X
TDC1112J7VX	EXT – T_C = –55°C to 125°C	MIL-STD-883	24 Pin Hermetic Ceramic DIP	1112J7V-X
TDC1112N7CX	STD – T_A = 0°C to 70°C	Commercial	24 Pin Plastic DIP	1112N7C-X
TDC1112C3VX	EXT – T_C = –55°C to 125°C	MIL-STD-883	28 Contact Chip Carrier	1112C3V-X
TDC1112R3CX	STD – T_A = 0°C to 70°C	Commercial	28 Leaded Plastic Chip Carrier	1112R3C-X

Note: 1. The "X" in the product designation denotes the linearity grade, guaranteed over the operating temperature range, per the following table:

Linearity Grade (X)	None	1	2	3
E_{LD} Linearity Error, Differential	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)	±0.012% (1/2 LSB)
E_{LI} Linearity Error, Integral	±0.096% (4 LSB)	±0.048% (2 LSB)	±0.048% (2 LSB)	±0.024% (1 LSB)

Not every grade is available in every package/screening/temperature range combination. Consult factory for availability.

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