# TDC1009

## Use TMC2009 for New Designs

## VLSI Multiplier–Accumulator

12 X 12 Bit, 135ns

The TDC1009 is a high-speed 12 x 12 bit parallel multiplier-accumulator which operates at a 135 nanosecond cycle time (7.4MHz multiply-accumulate rate). The input data may be specified as two's complement or unsigned magnitude, yielding a full-precision 24-bit product. Products may be accumulated to a 27-bit result.

Individually clocked input and output registers are provided to maximize system throughput and simplify bus interfacing. These registers are positive-edge-triggered D-type flip-flops. The result is divided into a 3-bit eXTended Product (XTP), a 12-bit Most Significant Product (MSP), and a 12-bit Least Significant Product (LSP). Individual three-state output ports are provided for the XTP, the MSP, and the LSP. The output register can be preloaded directly via the output ports.

Built with TRW's 2-micron bipolar process, the TDC1009 is a uniquely powerful LSI signal processing device.

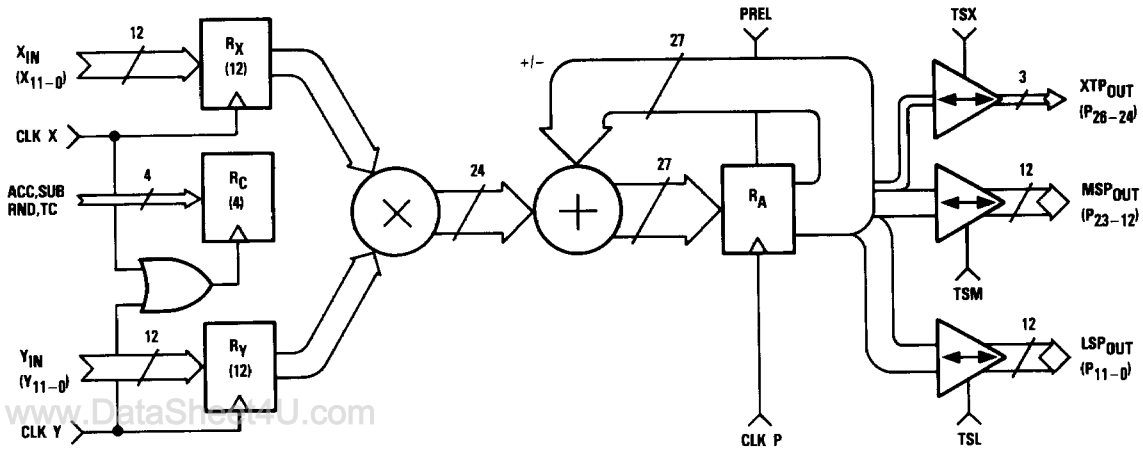
### Features

- 135ns Multiply-Accumulate Time (Worst Case)
- 12 x 12 Bit Parallel Multiplication With Accumulation To 27-Bit Result
- Selectable Accumulation, Subtraction, Rounding, And Preloading
- All Inputs And Outputs Are Registered TTL Compatible
- Three-State Output
- Two's Complement Or Unsigned Magnitude Operation
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In 64 Lead Ceramic DIP, 68 Contact Chip Carrier, Or 68 Leaded Chip Carrier

### Applications

- Array Processors
- Video Processors
- Radar Signal Processors
- FFT Processors
- General Purpose Digital Signal Processors
- Microcomputer/Minicomputer Accelerators

### Functional Block Diagram



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