TDC1006

Serial Shift Register
256-Bit

The TRW TDC1006 is a positive-edge-triggered serial shift register which operates at 25MHz. This device is cascadable in the number of words and the word size.

Complementary TTL outputs Q and $\overline{Q}$ are provided. Two data inputs, D0 and D1, are controlled by a data select input, DS. This provides on-chip recirculate gating when the true output is hard-wired to one of the inputs.

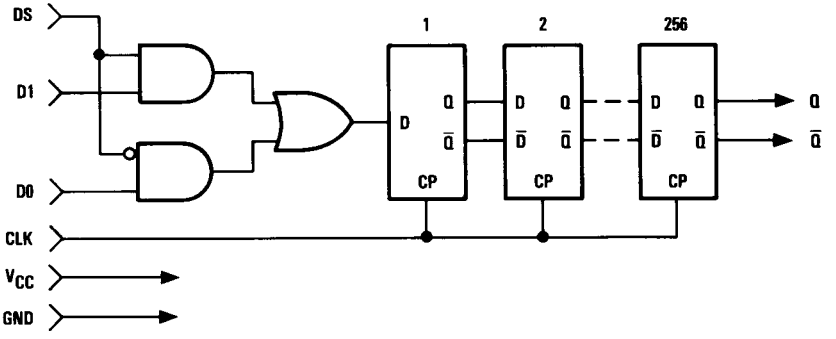
Features

- 25MHz Guaranteed Clock Frequency
- Fully TTL Compatible
- True and Complementary Outputs
- Proven High-Reliability Radiation Hard Bipolar Process
- Single +5V Power Supply
- Available In A 16 Pin CERDIP
- Horizontal And Vertical Cascadability

Applications

- High-Speed Data Acquisition
- First-In First-Out Data Buffers
- Coefficient Storage For FIR Filters
- Digital Delay Lines
- Local Storage Registers

Functional Block Diagram



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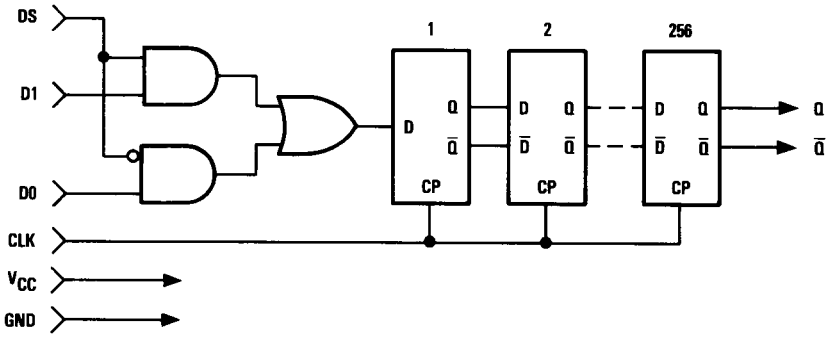
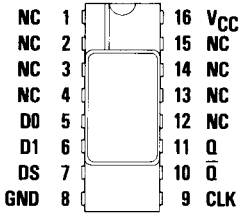
Functional Block Diagram



Pin Assignments



16 Pin CERDIP – B9 Package

Functional Description

General Information

The TDC1006 is a 256-bit positive-edge-triggered serial shift register. One of two data inputs (D0 and D1) is selected by the Data Select control DS. Complementary outputs Q and $\bar{Q}$ are available.

Power

The TDC1006 operates from a single +5 Volt power supply.

Name	Function	Value	J9 Package
V_{CC}	Positive Supply Voltage	+5.0V	Pin 16
GND	Ground	0.0V	Pin 8

Data Inputs

The TDC1006 is a single 256-bit shift register with two data inputs D0 and D1.

Name	Function	Value	J9 Package
D0	Data Input 0	TTL	Pin 5
D1	Data Input 1	TTL	Pin 6

Data Select

The TDC1006 has one data select control (DS) to select between inputs D0 and D1. Input D1 is selected when DS is HIGH, D0 is selected when DS is LOW.

Name	Function	Value	J9 Package
DS	Data Select	TTL	Pin 7

Data Outputs

Complementary outputs Q and $\overline{Q}$ are provided for the TDC1006.

Name	Function	Value	J9 Package
Q	Data Output	TTL	Pin 11
$\overline{Q}$	Data Output Inverted	TTL	Pin 10

Clocks

The TDC1006 has one clock signal, CLK.

Name	Function	Value	J9 Package
CLK	Clock	TTL	Pin 9

K

No Connects

There are several pins on the TDC1006 which are not connected internally. These pins may be left unconnected.

Name	Function	Value	J9 Package
NC	No Connect	Open	Pins 1-4, 12-15

Figure 1. Timing Diagram

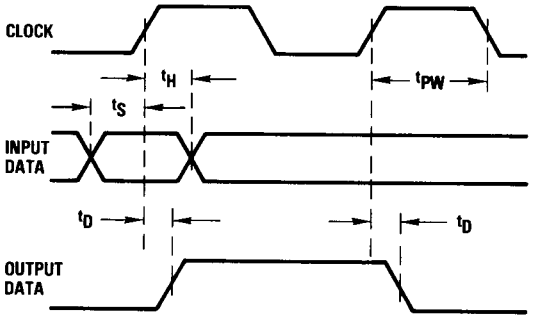


Figure 2. Equivalent Input/Output Schematics

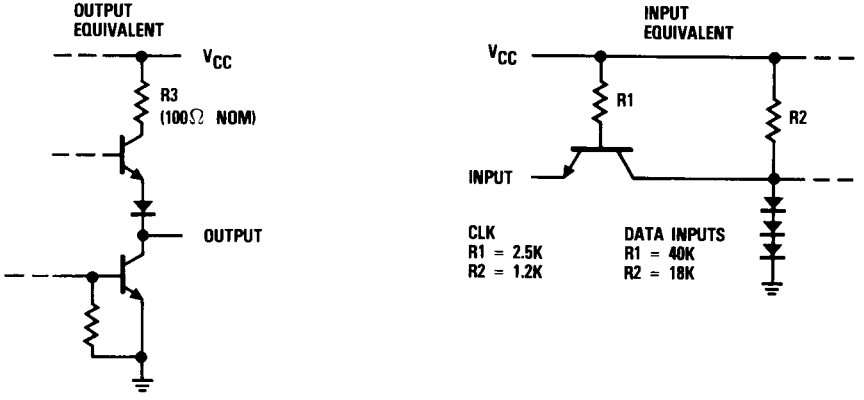
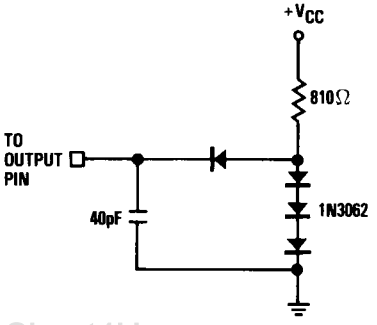


Figure 3. Test Load



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0 V
Input Voltage	0 to +5.5V
Output	
Applied voltage (measured to GND)	0 to +5.5V [2]
Applied current, externally forced	−1.0 to +6.0mA [3,4]
Short circuit duration (single output in high state to ground)	1 sec
Temperature	
Operating, ambient	−55 to +150°C
junction	+175°C
Lead, soldering (10 sec.)	+300°C
Storage	−65 to +160°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
t_{PW}	Clock Pulse Width	15			15			ns
t_S	Input Register Setup Time	7			7			ns
t_H	Input Register Hold Time	10			10			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−400			−400	μA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{CC}	Supply Current	V_{CC} = Max		135		155	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max		0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max	2.4		2.4		V
I_{IL}	Input Current, Logic LOW [1]	V_{CC} = Max, V_{IL} = 0.4V		−0.5		−0.8	mA/Load
I_{IH}	Input Current, Logic HIGH [1]	V_{CC} = Max, V_{IH} = 2.4V		20		50	μA/Load

Note: 1. CLK. Sixteen equivalent loads.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
F_C	Clock Frequency	See Figure 1	25		24		MHz
t_D	Output Delay	See Figure 1		32		35	ns

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1006B9C	STD − T_A = 0°C to 70°C	Commercial	16 Pin CERDIP	1006B9C
TDC1006B9A	EXT − T_C = −55°C to 125°C	High Reliability	16 Pin CERDIP	1006B9A