LTC2401/LTC2402

1-/2-Channel 24-Bit µPower No Latency ΔΣ™ ADC in MSOP-10

January 2000

FEATURES

- 24-Bit ADC in Tiny MSOP-10 Package
- 1- or 2-Channel Inputs
- Automatic Channel Selection (Ping-Pong) (LTC2402)
- Zero Scale and Full Scale Set for Reference and Ground Sensing
- **4ppm INL, No Missing Codes**
- **4ppm Full-Scale Error**
- **0.5ppm Offset**
- **0.6ppm Noise**
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter
- **Single Conversion Settling Time for Multiplexed Applications**
- Reference Input Voltage: 0.1V to V_{CC}
- Live Zero—Extended Input Range Accommodates 12.5% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown

APPLICATIONS

- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain-Gage Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control

DESCRIPTION

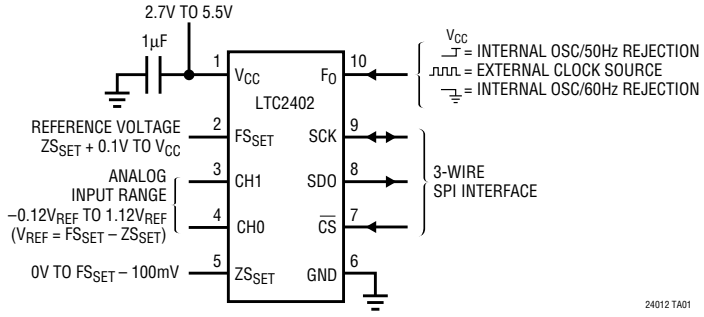
The LTC®2401/LTC2402 are 1- and 2-channel 2.7V to 5.5V micropower 24-bit analog-to-digital converters with an integrated oscillator, 4ppm INL and 0.6ppm RMS noise. These ultrasmall devices use delta-sigma technology and a new digital filter architecture that settles in a single cycle. This eliminates the latency found in conventional ΔΣ converters and simplifies multiplexed applications.

Through a single pin, the LTC2401/LTC2402 can be configured for better than 110dB rejection at 50Hz or 60Hz ±2%, or can be driven by an external oscillator for a user defined rejection frequency in the range 1Hz to 120Hz. The internal oscillator requires no external frequency setting components.

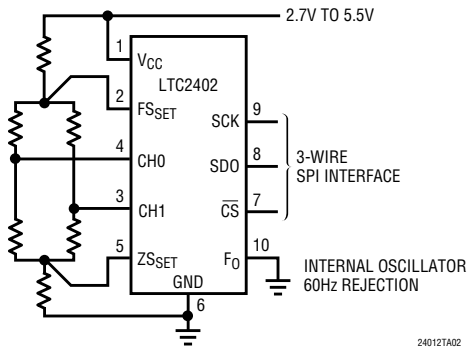
These converters accept an external reference voltage from 0.1V to V_{CC}. With an extended input conversion range of –12.5% V_{REF} to 112.5% V_{REF} (V_{REF} = FS_{SET} – ZS_{SET}), the LTC2401/LTC2402 smoothly resolve the offset and overrange problems of preceding sensors or signal conditioning circuits.

The LTC2401/LTC2402 communicate through a 2- or 3-wire digital interface that is compatible with SPI and MICROWIRE™ protocols.

TYPICAL APPLICATION



Pseudo Differential Bridge Digitizer

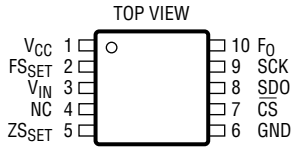


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) to GND .....–0.3V to 7V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)

Operating Temperature Range
LTC2401/LTC2402C ..... 0°C to 70°C
LTC2401/LTC2402I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

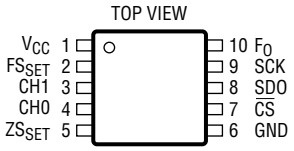
PACKAGE/ORDER INFORMATION



MS10 PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC2401CMS LTC2401IMS
MS10 PART MARKING
LTMB LTMC



MS10 PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC2402CMS LTC2402IMS
MS10 PART MARKING
LTMD LTME

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{REF} = FS_{SET} – ZS_{SET}. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution		●	24			Bits
No Missing Codes Resolution	0.1V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V (Note 5)	●	24			Bits
Integral Nonlinearity	FS_{SET} = 2.5V, ZS_{SET} = 0V (Note 6) FS_{SET} = 5V, ZS_{SET} = 0V (Note 6)	● ●		2 4	10 15	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V	●		0.5	2	ppm of V_{REF}
Offset Error Drift	2.5V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V			0.01		ppm of V_{REF}/°C
Full-Scale Error	2.5V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V	●		4	10	ppm of V_{REF}
Full-Scale Error Drift	2.5V ≤ FS_{SET} ≤ V_{CC}, ZS_{SET} = 0V			0.04		ppm of V_{REF}/°C
Total Unadjusted Error	FS_{SET} = 2.5V, ZS_{SET} = 0V FS_{SET} = 5V, ZS_{SET} = 0V			5 10		ppm of V_{REF} ppm of V_{REF}
Output Noise	V_{IN} = 0V (Note 13)			3		μV_{RMS}
Normal Mode Rejection 60Hz ±2%	(Note 7)	●	110	130		dB
Normal Mode Rejection 50Hz ±2%	(Note 8)	●	110	130		dB
Power Supply Rejection, DC	FS_{SET} = 2.5V, ZS_{SET} = 0V, V_{IN} = 0V			100		dB
Power Supply Rejection, 60Hz ±2%	FS_{SET} = 2.5V, ZS_{SET} = 0V, V_{IN} = 0V, (Note 7)			110		dB
Power Supply Rejection, 50Hz ±2%	FS_{SET} = 2.5V, ZS_{SET} = 0V, V_{IN} = 0V, (Note 8)			110		dB

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{REF} = FS_{SET} – ZS_{SET}. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 14)	●	–0.125 • V_{REF}		1.125 • V_{REF}	V
FS_{SET}	Full-Scale Set Range		●	0.1 + ZS_{SET}		V_{CC}	V
ZS_{SET}	Zero-Scale Set Range		●	0		FS_{SET} – 0.1	V
$C_{S(IN)}$	Input Sampling Capacitance				10		pF
$C_{S(REF)}$	Reference Sampling Capacitance				15		pF
$I_{IN(LEAK)}$	Input Leakage Current	$\overline{CS}$ = V_{CC}	●	–10	1	10	nA
$I_{REF(LEAK)}$	Reference Leakage Current	V_{REF} = 2.5V, $\overline{CS}$ = V_{CC}	●	–12	1	12	nA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	2.7V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 3.3V	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V	●			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 3.3V (Note 9)	●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 5.5V (Note 9)	●			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)			10		pF
V_{OH}	High Level Output Voltage SDO	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 10)	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 10)	●			0.4	V
I_{OZ}	High-Z Output Leakage SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 12) $\overline{CS}$ = V_{CC} (Note 12)	 ● ●		 200 20	 300 30	 µA µA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	2.56		307.2	kHz
t_{HEO}	External Oscillator High Period		●	0.5		390	µs
t_{LEO}	External Oscillator Low Period		●	0.5		390	µs
t_{CONV}	Conversion Time	F_O = 0V	●	130.66	133.33	136	ms
		$F_O = V_{CC}$	●	156.80	160	163.20	ms
		External Oscillator (Note 11)	●		20480/f_{EOSC} (in kHz)		ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10)			19.2		kHz
		External Oscillator (Notes 10, 11)			f_{EOSC}/8		kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)		45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12)	●	1.64	1.67	1.70	ms
		External Oscillator (Notes 10, 11)	●		256/f_{EOSC} (in kHz)		ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 9)	●		32/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		150	ns
t2	$\overline{CS}$ ↑ to SDO High Z		●	0		150	ns
t3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		150	ns
t4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7 to 5.5V unless otherwise specified. Input source resistance = 0Ω.

Note 4: Internal Conversion Clock source with the F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: $F_O = V_{CC}$ (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator. F_O = 0V or $F_O = V_{CC}$.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: For reference voltage values V_{REF} > 2.5V, the extended input of –0.125 • V_{REF} to 1.125 • V_{REF} is limited by the absolute maximum rating of the Analog Input Voltage pin (Pin 3). For 2.5V < $V_{REF} \leq$ 0.267V + 0.89 • V_{CC}, the input voltage range is –0.3V to 1.125 • V_{REF}. For 0.267V + 0.89 • V_{CC} < $V_{REF} \leq V_{CC}$, the input voltage range is –0.3V to V_{CC} + 0.3V.

PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply Voltage. Bypass to GND (Pin 4) with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

FS_{SET} (Pin 2): Full-Scale Set Input. This pin defines the full-scale input value. When $V_{IN} = FS_{SET}$, the ADC outputs full scale ($FFFFF_H$). The total reference voltage is $FS_{SET} – ZS_{SET}$.

CH0, CH1 (Pins 4, 3): Analog Input Channels. The input voltage range is $–0.125 • V_{REF}$ to $1.125 • V_{REF}$. For $V_{REF} > 2.5V$, the input voltage range may be limited by the absolute maximum rating of –0.3V to V_{CC} + 0.3V. Conversions are performed alternately between CH0 and CH1 for the LTC2402. Pin 4 is a No Connect (NC) on the LTC2401.

ZS_{SET} (Pin 5): Zero-Scale Set Input. This pin defines the zero-scale input value. When $V_{IN} = ZS_{SET}$, the ADC outputs zero scale (00000_H).

GND (Pin 6): Ground. Shared pin for analog ground, digital ground, reference ground and signal ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single-point grounding system.

$\overline{CS}$ (Pin 7): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion, the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW on $\overline{CS}$ wakes up the ADC. A LOW-to-HIGH transition on this pin disables the SDO digital output. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 8): Three-State Digital Output. During the data output period, this pin is used for serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS} = V_{CC}$), the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin can be used as a conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW.

SCK (Pin 9): Bidirectional Digital Clock Pin. In the Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the data output period. In the External Serial Clock Operation mode, SCK is used as digital input for the external serial interface. An internal pull-up current source is automatically activated in Internal Serial Clock Operation mode. The Serial Clock mode is determined by the level applied to SCK at power up and the falling edge of $\overline{CS}$.

F_O (Pin 10): Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$), the converter uses its internal oscillator and the digital filter's first null is located at 50Hz. When the F_O pin is connected to GND ($F_O = 0V$), the converter uses its internal oscillator and the digital filter's first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC}, the converter uses this signal as its clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

APPLICATIONS INFORMATION

Output Data Format

The LTC2401/LTC2402 serial output data stream is 32 bits long. The first 4 bits represent status information indicating the sign, selected channel, input range and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 4 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.

Bit 31 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is LOW if the last conversion was performed on CH0 and HIGH for CH1.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW. The sign bit changes state during the zero code.

Bit 28 (forth output bit) is the extended input range (EXR) indicator. If the input is within the normal input range $0 \le V_{IN} \le V_{REF}$, this bit is LOW. If the input is outside the normal input range, $V_{IN} > V_{REF}$ or $V_{IN} < 0$, this bit is HIGH.

The function of these bits is summarized in Table 1.

Table 1. LTC2401/LTC2402 Status Bits

Input Range	Bit 31 $\overline{EOC}$	Bit 30 CH0/CH1	Bit 29 SIG	Bit 28 EXR
$V_{IN} > V_{REF}$	0	0/1	1	1
$0 < V_{IN} \le V_{REF}$	0	0/1	1	0
$V_{IN} = 0^+/0^-$	0	0/1	1/0	0
$V_{IN} < 0$	0	0/1	0	1

Bit 27 (fifth output bit) is the most significant bit (MSB).

Bits 27-4 are the 24-bit conversion result MSB first.

Bit 4 is the least significant bit (LSB).

Bits 3-0 are sub LSBs below the 24-bit level. Bits 3-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 1. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and any SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first

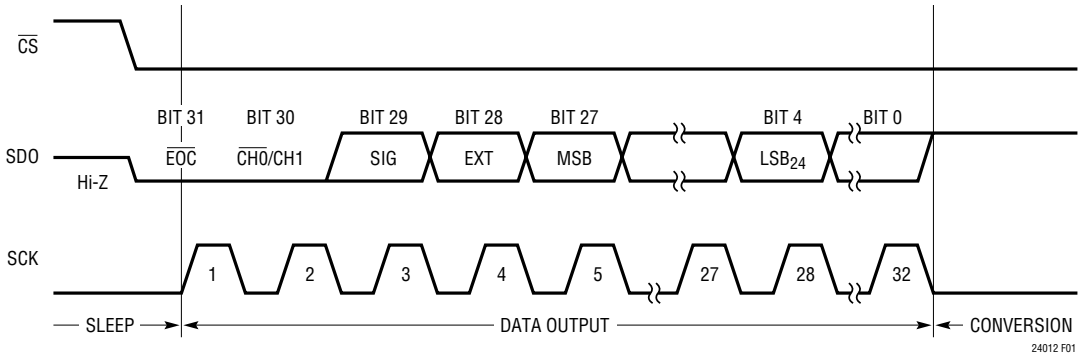


Figure 1. Output Data Timing

APPLICATIONS INFORMATION

falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating a new conversion cycle has been initiated. This bit serves as $\overline{EOC}$ (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the V_{IN} pin is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any input value from –0.125 • V_{REF} to 1.125 • V_{REF}. For input voltages greater than 1.125 • V_{REF}, the conversion result is clamped to the value corresponding to 1.125 • V_{REF}. For input voltages below –0.125 • V_{REF}, the conversion result is clamped to the value corresponding to –0.125 • V_{REF}.

Single Ended Half-Bridge Digitizer with Reference and Ground Sensing

Sensors convert real world phenomena (temperature, pressure, gas levels, etc.) into a voltage. Typically, this voltage is generated by passing an excitation current through the sensor. The wires connecting the sensor to the ADC form parasitic resistors R_{P1} and R_{P2}. The excitation current also flows through parasitic resistors R_{P1} and R_{P2}, as shown in Figure 2. The voltage drop across these parasitic resistors leads to systematic offset and full-scale errors.

In order to eliminate the errors associated with these parasitic resistors, the LTC2401/LTC2402 include a full-scale set input (FS_{SET}) and a zero-scale set input (ZS_{SET}). As shown in Figure 3, the FS_{SET} pin acts as a zero input full-scale sense input. Errors due to parasitic resistance R_{P1} in series with the half-bridge sensor are

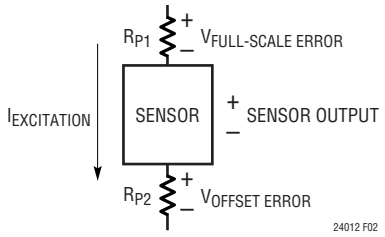


Figure 2. Errors Due to Excitation Currents

Table 2. LTC2401/LTC2402 Output Data Format

Input Voltage	Bit 31 $\overline{EOC}$	Bit 30 CH SELECT	Bit 29 SIG	Bit 28 EXR	Bit 27 MSB	Bit 26	Bit 25	Bit 24	Bit 23	…	Bit 4 LSB	Bit 3-0 SUB LSBs*
V_{IN} > 9/8 • V_{REF}	0	$\overline{CH0}$/CH1	1	1	0	0	0	1	1	...	1	X
9/8 • V_{REF}	0	$\overline{CH0}$/CH1	1	1	0	0	0	1	1	...	1	X
V_{REF} + 1LSB	0	$\overline{CH0}$/CH1	1	1	0	0	0	0	0	...	0	X
V_{REF}	0	$\overline{CH0}$/CH1	1	0	1	1	1	1	1	...	1	X
3/4V_{REF} + 1LSB	0	$\overline{CH0}$/CH1	1	0	1	1	0	0	0	...	0	X
3/4V_{REF}	0	$\overline{CH0}$/CH1	1	0	1	0	1	1	1	...	1	X
1/2V_{REF} + 1LSB	0	$\overline{CH0}$/CH1	1	0	1	0	0	0	0	...	0	X
1/2V_{REF}	0	$\overline{CH0}$/CH1	1	0	0	1	1	1	1	...	1	X
1/4V_{REF} + 1LSB	0	$\overline{CH0}$/CH1	1	0	0	1	0	0	0	...	0	X
1/4V_{REF}	0	$\overline{CH0}$/CH1	1	0	0	0	1	1	1	...	1	X
$0^+/0^-$	0	$\overline{CH0}$/CH1	1/0**	0	0	0	0	0	0	...	0	X
–1LSB	0	$\overline{CH0}$/CH1	0	1	1	1	1	1	1	...	1	X
–1/8 • V_{REF}	0	$\overline{CH0}$/CH1	0	1	1	1	1	0	0	...	0	X
V_{IN} < –1/8 • V_{REF}	0	$\overline{CH0}$/CH1	0	1	1	1	1	0	0	...	0	X

*The sub LSBs are valid conversion results beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.
**The sign bit changes state during the 0 code.

APPLICATIONS INFORMATION

removed by the FS_{SET} input to the ADC. The absolute full-scale output of the ADC (data out = $FFFFFF_{HEX}$) will occur at $V_{IN} = V_B = FS_{SET}$, see Figure 4. Similarly, the offset errors due to R_{P2} are removed by the ground sense input ZS_{SET}. The absolute zero output of the ADC (data out = 000000_{HEX}) occurs at $V_{IN} = V_A = ZS_{SET}$. Parasitic resistors R_{P3} to R_{P5} have negligible errors due to the 1nA (typ) leakage current at pins FS_{SET}, ZS_{SET} and V_{IN}. The wide dynamic input range (–300mV to 5.3V) and low noise (0.6ppm RMS) enable the LTC2401 or the LTC2402 to directly digitize the output of the bridge sensor.

The LTC2402 is ideal for applications requiring continuous monitoring of two input sensors. As shown in Figure 5, the LTC2402 can monitor both a thermocouple temperature probe and a cold junction temperature sensor. Absolute temperature measurements can be performed with a variety of thermocouples using digital cold junction compensation.

The selection between CH0 and CH1 is automatic. Initially, after power-up, a conversion is performed on CH0. For each subsequent conversion, the input channel selection

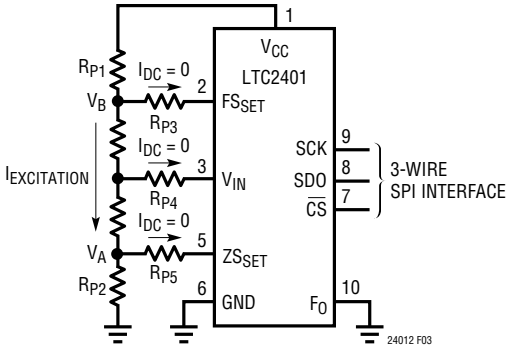


Figure 3. Half-Bridge Digitizer with Zero-Scale and Full-Scale Sense

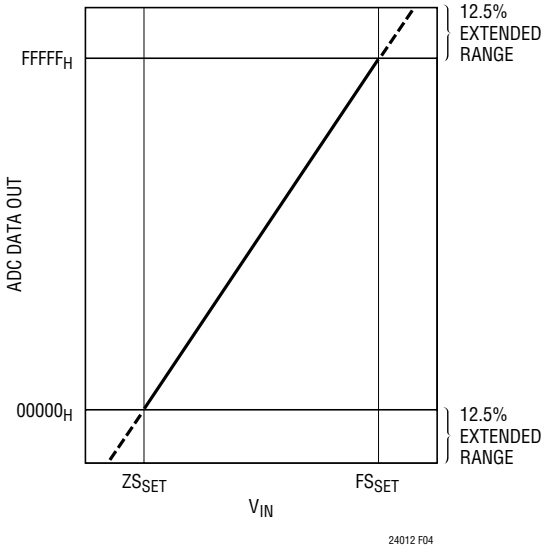


Figure 4. Transfer Curve with Zero-Scale and Full-Scale Set

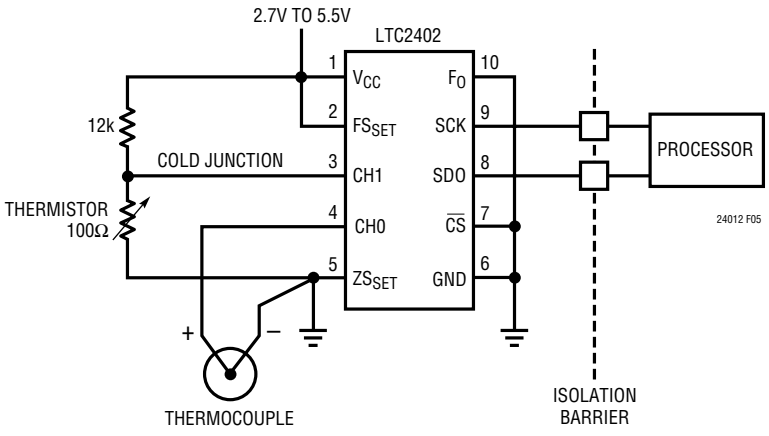


Figure 5. Isolated Temperature Measurement

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is alternated. Embedded within the serial data output is a status bit indicating which channel corresponds to the conversion result. If the conversion was performed on CH0, this bit (Bit 30) is LOW and is HIGH if the conversion was performed on CH1 (see Figure 6).

There are no extra control or status pins required to perform the alternating 2-channel measurements. The LTC2402 only requires two digital signals (SCK and SDO). This simplification is ideal for isolated temperature measurements or systems where minimal control signals are available.

Pseudo Differential Applications

Generally, designers choose fully differential topologies for several reasons. First, the interface to a 4- or 6-wire bridge is simple (it is a differential output). Second, they require good rejection of line frequency noise. Third, they typically look at a small differential signal sitting on a large common mode voltage; they need accurate measurements of the differential signal independent of the common mode input voltage. Many applications currently using fully differential analog-to-digital converters for any of the above reasons may migrate to a pseudo differential conversion using the LTC2402.

Direct Connection to a Full Bridge

The LTC2402 interfaces directly to a 4- or 6-wire bridge, as shown in Figure 7. Like the LTC2401, the LTC2402 includes a FS_{SET} and a ZS_{SET} for sensing the excitation voltage directly across the bridge. This eliminates errors due to excitation currents flowing through parasitic resistors. The LTC2402 also includes two single ended input channels which can tie directly to the differential output of the bridge. The two conversion results may be digitally subtracted yielding the differential result.

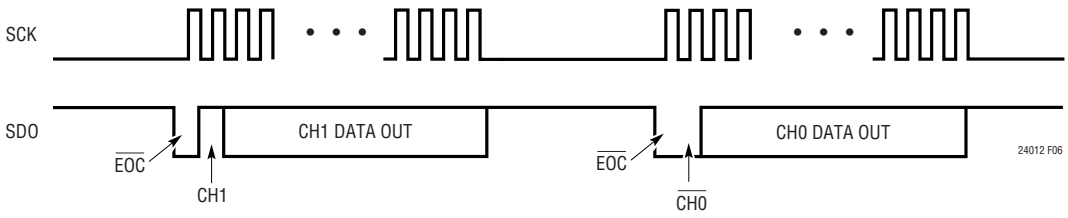

Figure 6. Embedded Selected Channel Indicator

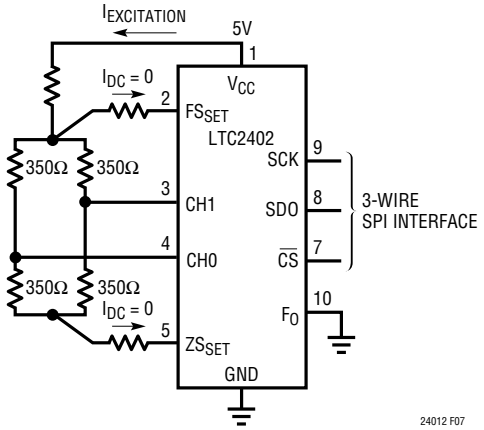

Figure 7. Pseudo Differential Strain Guage Application

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The LTC2402's single ended rejection of line frequencies (±2%) and harmonics is better than 110dB. Since the device performs two independent single ended conversions each with >110dB rejection, the overall common mode and differential rejection is much better than the 80dB rejection typically found in other differential input delta-sigma converters.

In addition to excellent rejection of line frequency noise, the LTC2402 also exhibits excellent single ended noise rejection over a wide range of frequencies due to its 4th order sinc filter. Each single ended conversion independently rejects high frequency noise (>60Hz). Care must be taken to insure noise at frequencies below 15Hz and at multiples of the ADC sample rate (15,600Hz) are not present. For this application, it is recommended the LTC2402 is placed in close proximity to the bridge sensor in order to reduce the noise injected into the ADC input. By performing three successive conversions (CH0-CH1-CH0), the drift and low frequency noise can be measured and compensated for digitally.

The absolute accuracy (less than 10 ppm total error) of the LTC2402 enables extremely accurate measurement of small signals sitting on large voltages. Each of the two pseudo differential measurements performed by the LTC2402 is absolutely accurate independent of the common mode voltage output from the bridge. The pseudo differential result obtained from digitally subtracting the two single ended conversion results is accurate to within the noise level of the device ($3\mu V_{RMS}$) divided by square root of 2, independent of the common mode input voltage.

Typically, a bridge sensor outputs 2mV/V full scale. With a 5V excitation, this translates to a full-scale output of 10mV. Divided by the RMS noise of 4.2μV(=3μV • 1.414), this circuit yields 2,300 counts with no averaging or amplification. If more counts are required, several conversions may be averaged (the number of effective counts is increased by a factor of square root of 2 for each doubling of averages).

An RTD Temperature Digitizer

RTDs used in remote temperature measurements often have long lead lengths between the ADC and RTD sensor. These long lead lengths lead to voltage drops due to excitation current in the interconnect to the RTD. This voltage drop can be measured and digitally removed using the LTC2402 (see Figure 8).

The excitation current (typically 200μA) flows from the ADC through a long lead length to the remote temperature sensor (RTD). This current is applied to the RTD, whose resistance changes as a function of temperature (100Ω to 400Ω for 0°C to 800°C). The same excitation current flows back to the ADC ground and generates another voltage drop across the return leads. In order to get an accurate measurement of the temperature, these voltage drops must be measured and removed from the conversion result. Assuming the resistance is approximately the same

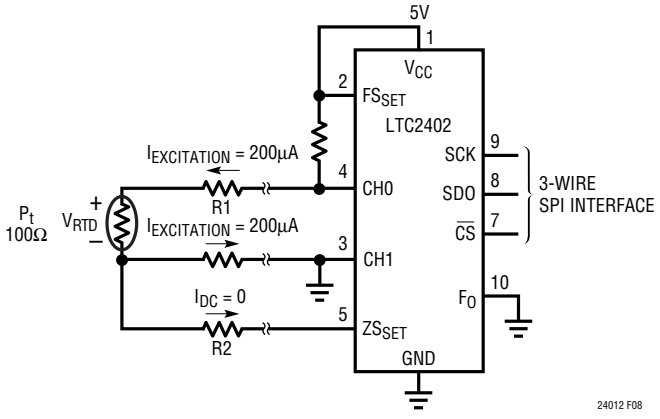

Figure 8. RTD Remote Temperature Measurement

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for the forward and return paths (R1 = R2), the auxiliary channel on the LTC2402 can measure this drop. These errors are then removed with simple digital correction.

The result of the first conversion on CH0 corresponds to an input voltage of $V_{RTD} + R1 \bullet I_{EXCITATION}$. The result of the second conversion (CH1) is $-R1 \bullet I_{EXCITATION}$. Note, the LTC2402's input range is not limited to the supply rails, it has underrange capabilities. The device's input range is –300mV to V_{REF} + 300mV. Adding the two conversion results together, the voltage drop across the RTD's leads are cancelled and the final result is V_{RTD}.

An Isolated, 24-Bit Data Acquisition System

The LTC1535 is useful for signal isolation. Figure 9 shows a fully isolated, 24-bit differential input A/D converter implemented with the LTC1535 and LTC2402. Power on the isolated side is regulated by an LT1761-5.0 low noise, low dropout micropower regulator. Its output is suitable for driving bridge circuits and for ratiometric applications.

During power-up, the LTC2402 becomes active at V_{CC} = 2.3V, while the isolated side of the LTC1535 must wait for V_{CC2} to reach its undervoltage lockout threshold of 4.2V. Below 4.2V, the LTC1535's driver outputs Y and Z are in a high impedance state, allowing the 1kΩ pull-down to define the logic state at SCK. When the LTC2402 first becomes active, it samples SCK; a logic "0" provided by the 1kΩ pull-down invokes the external serial clock mode. In this mode, the LTC2402 is controlled by a single clock line from the nonisolated side of the barrier, through the LTC1535's driver output Y. The entire power-up sequence, from the time power is applied to V_{CC1} until the LT1761's output has reached 5V, is approximately 1ms.

Data returns to the nonisolated side through the LTC1535's receiver at RO. An internal divider on receiver input B sets a logic threshold of approximately 3.4V at input A, facilitating communications with the LTC2402's SDO output without the need for any external components.

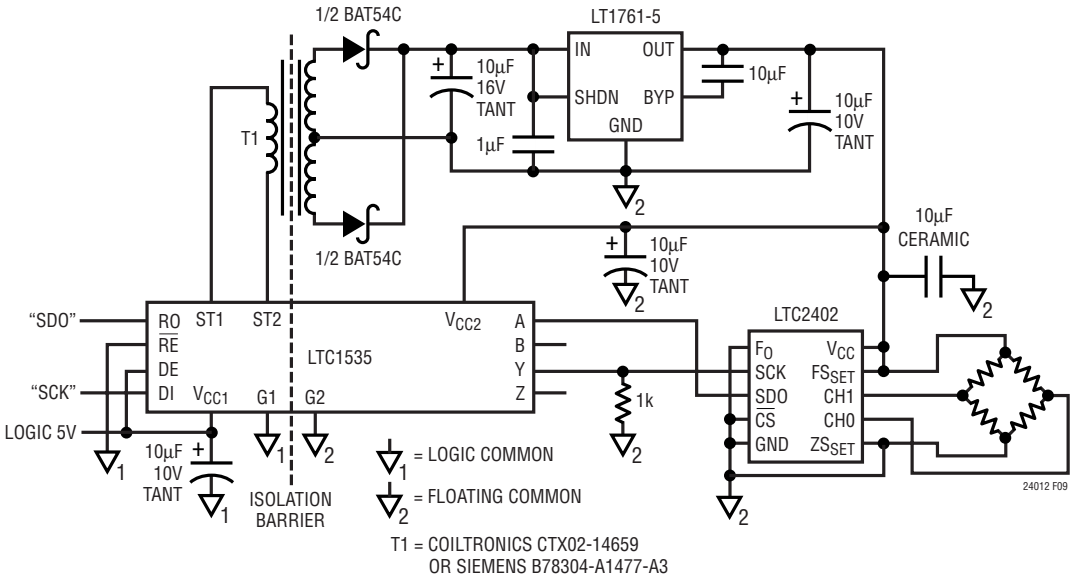
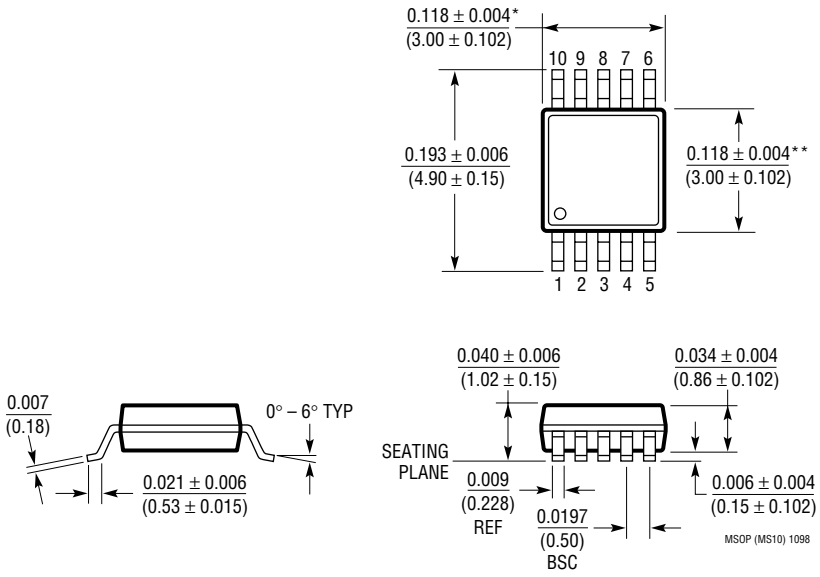


Figure 9. Complete, Isolated 24-Bit Data Acquisition System

PACKAGE INFORMATION

Dimensions in inches (millimeters) unless otherwise noted.

MS10 Package
10-Lead Plastic MSOP
(LTC DWG # 05-08-1661)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1019	Precision Bandgap Reference, 2.5V, 5V	3ppm/°C Drift, 0.05% Max
LT1025	Micropower Thermocouple Cold Junction Compensator	80µA Supply Current, 0.5°C Initial Accuracy
LTC1043	Dual Precision Instrumentation Switched Capacitor Building Block	Precise Charge, Balanced Switching, Low Power
LTC1050	Precision Chopper Stabilized Op Amp	No External Components 5µV Offset, 1.6µV_{P-P} Noise
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LTC1391	8-Channel Multiplexer	Low R_{ON}: 45Ω, Low Charge Injection Serial Interface
LT1460	Micropower Series Reference	0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions, MSOP, PDIP, SO-8, SOT-23 and TO-92 Packages
LT1461-2.5	Precision Micropower Voltage Reference	50µA Supply Current, 3ppm/°C Drift
LTC2400	24-Bit, No Latency ΔΣ ADC in SO-8	4ppm INL, 10ppm Total Unadjusted Error, 200µA
LTC2404/LTC2408	4-/8-Channel, 24-Bit, No Latency ΔΣ ADC	4ppm INL, 10ppm Total Unadjusted Error, 200µA

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