DC Accurate, Clock-Tunable Linear Phase 5th Order Bessel Lowpass Filter

FEATURES

- Clock-Tunable Cutoff Frequency
- 1mV DC Offset (Typical)
- 80dB CMR (Typical)
- Internal or External Clock
- 50μV_{RMS} Clock Feedthrough
- 100:1 Clock-to-Cutoff Frequency Ratio
- 80μV_{RMS} Total Wideband Noise
- 0.004% Noise + THD at 2V_{RMS} Output Level
- 50kHz Maximum Cutoff Frequency
- Cascadable for Faster Roll-Off
- Operates from ±2.375 to ±8V Power Supplies
- Self-Clocking with 1 RC

APPLICATIONS

- Audio
- Strain Gauge Amplifiers
- Anti-Aliasing Filters
- Low Level Filtering
- Digital Voltmeters
- Smoothing Filters
- Reconstruction Filters

DESCRIPTION

The LTC1065 is the first monolithic filter providing both clock-tunability with low DC output offset and over 12-bit DC accuracy. The frequency response of the LTC1065 closely approximates a 5th order Bessel polynomial. With appropriate PCB layout techniques the output DC offset is typically 1mV and is constant over a wide range of clock frequencies. With ±5V supplies and ±4V input voltage range, the CMR of the device is typically 80dB.

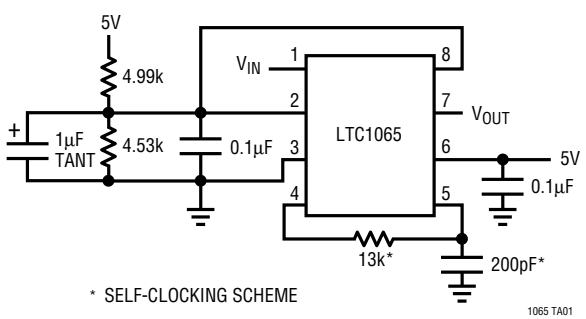
The filter cutoff frequency is controlled either by an internal or external clock. The clock-to-cutoff frequency ratio is 100 : 1. The on-board clock is nearly power supply independent and it is programmed via an external RC. The 50μV_{RMS} clock feedthrough of the device is considerably lower than other existing monolithic filters.

The LTC1065 wideband noise is 80μV_{RMS} and it can process large AC input signals with low distortion. With ±7.5V supplies, for instance, the filter handles up to 4V_{RMS} (94dB S/N ratio) while the standard 1kHz THD is below 0.005%; 87dB dynamic range (S/N + THD) is obtained with input levels between 2V_{RMS} and 2.5V_{RMS}.

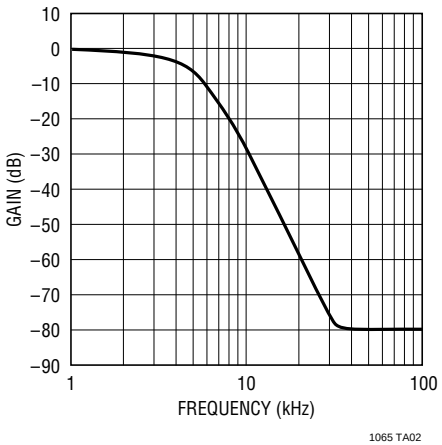
The LTC1065 is available in 8-pin miniDIP and 16-pin SOL. For a Butterworth response, see LTC1063 data sheet. The LTC1065 is pin compatible with the LTC1063.

TYPICAL APPLICATION

3.4kHz Single 5V Supply Bessel Lowpass Filter



Frequency Response

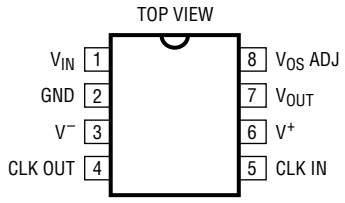


ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 400mW
Voltage at Any Input .... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Burn-In Voltage 16V
Storage Temperature Range ..... –65°C to 150°C

Operating Temperature Range
LTC1065C ..... –40°C to 85°C
LTC1065M ..... –55°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

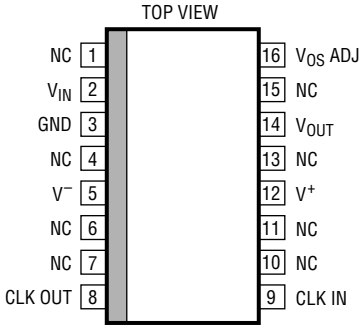


J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J)
T_{JMAX} = 100°C, θ_{JA} = 110°C/W (N)

ORDER PART NUMBER

LTC1065CN8
LTC1065MJ8



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 100°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1065CS

ELECTRICAL CHARACTERISTICS

V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz, R_L = 10k, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock-to-Cutoff Frequency Ratio (f_{CLK}/f_C)	$\pm2.375V \leq V_S \leq \pm7.5V$			100±0.5		
Maximum Clock Frequency (Note 1)	V_S = ±7.5V			5		MHz
	V_S = ±5V			4		MHz
	V_S = ±2.5V			3		MHz
Minimum Clock Frequency (Note 2)	$\pm2.5V \leq V_S \leq \pm7.5V$, T_A < 85°C			30		Hz
Input Frequency Range			0		$0.9f_{CLK}$	
Filter Gain	V_S = ±5V, f_{CLK} = 25kHz, f_C = 250Hz					
	f_{IN} = 250Hz	●	–3.5	–3.1	–2.7	dB
	f_{IN} = 1kHz	●	–43.0	–41.0	–39.0	dB
	V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz					
	f_{IN} = 100Hz			0		dB
	$f_{IN} = 1kHz = 0.2f_C$	●	–0.215	–0.175	–0.135	dB
	$f_{IN} = 2.5kHz = 0.5f_C$	●	–1.1	–0.972	–0.84	dB
	$f_{IN} = 4kHz = 0.8f_C$	●	–2.35	–2.13	–1.9	dB
	$f_{IN} = 5kHz = f_C$	●	–3.35	–3.1	–2.83	dB
	$f_{IN} = 10kHz = 2f_C$	●	–14.63	–14.15	–13.7	dB
	$f_{IN} = 20kHz = 4f_C$	●	–43.0	–41.15	–39.0	dB

ELECTRICAL CHARACTERISTICS

V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz, R_L = 10k, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Filter Gain	V_S = ±2.375V, f_{CLK} = 500kHz, f_C = 5kHz					
	f_{IN} = 1kHz	●	–0.225	–0.185	–0.145	dB
	f_{IN} = 2.5kHz	●	–1.1	–1.0	–0.83	dB
	f_{IN} = 4kHz	●	–2.35	–2.15	–1.9	dB
	f_{IN} = 5kHz	●	–3.35	–3.1	–2.83	dB
	f_{IN} = 10kHz	●	–14.63	–14.1	–13.7	dB
Clock Feedthrough	±2.375V ≤ V_S ≤ ±7.5V			50		μV_{RMS}
Wideband Noise (Note 3)	±2.375V ≤ V_S ≤ ±7.5V, 1Hz < f < f_{CLK}			80		μV_{RMS}
THD + Wideband Noise (Note 4)	V_S = ±7.5V, f_C = 20kHz, f_{IN} = 1kHz, $2V_{RMS} \le V_{IN} \le 2.5V_{RMS}$			–87		dB
Filter Output ± DC Swing	V_S = ±2.375V		1.5/–2.0	1.7/–2.2		V
		●	1.3/–1.8			V
	V_S = ±5V		4.0/–4.5	4.3/–4.8		V
		●	3.8/–4.3			V
	V_S = ±7.5V		6.5/–7.0	6.8/–7.3		V
		●	6.3/–6.8			V
Input Bias Current				10		nA
Dynamic Input Impedance				800		MΩ
Output DC Offset (Note 5)	V_S = ±2.375V			2		mV
	V_S = ±5V			0	±5	mV
	V_S = ±7.5V			–4		mV
Output DC Offset Drift	V_S = ±2.375V			10		µV/°C
	V_S = ±5V			20		µV/°C
	V_S = ±7.5V			25		µV/°C
Self-Clocking Frequency (f_{OSC})	R (Pin 4 to 5) = 20k, C (Pin 5 to GND) = 470pF					
	V_S = ±2.375V		99	103	112	kHz
	LTC1065C	●	95	103	112	kHz
	LTC1065M	●	92	100	112	kHz
	V_S = ±5V		100	106	112	kHz
	LTC1065C	●	98	106	114	kHz
	LTC1065M	●	97	105	114	khz
	V_S = ±7.5V		102	106	114	kHz
	LTC1065C	●	101	109	116	kHz
	LTC1065M	●	100	108	116	kHz
External CLK Pin Logic Thresholds	V_S = ±2.375V Min Logical "1"			1.43		V
	Max Logical "0"			0.47		V
	V_S = ±5V Min Logical "1"			3		V
	Max Logical "0"			1		V
	V_S = ±7.5V Min Logical "1"			4.5		V
	Max Logical "0"			1.5		V
Power Supply Current	V_S = ±2.375V, f_{CLK} = 500kHz			2.5	4.0	mA
	LTC1065C	●			5.5	mA
	LTC1065M	●			6.0	mA
	V_S = ±5V, f_{CLK} = 500kHz			5.5	9	mA
	LTC1065C	●			11	mA
	LTC1065M	●			12	mA
	V_S = ±7.5V, f_{CLK} = 500kHz			7.0	12.0	mA
	LTC1065C	●			14.5	mA
	LTC1065M	●			16.0	mA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The maximum clock frequency is arbitrarily defined as: the frequency at which the filter AC response exhibits ≥ 1dB of gain peaking.

Note 2: At limited temperature ranges (i.e., $T_A \leq 50°C$) the minimum clock frequency can be as low as 10Hz. The typical minimum clock frequency is arbitrarily defined as: the clock frequency at which the output DC offset changes by more than 1mV.

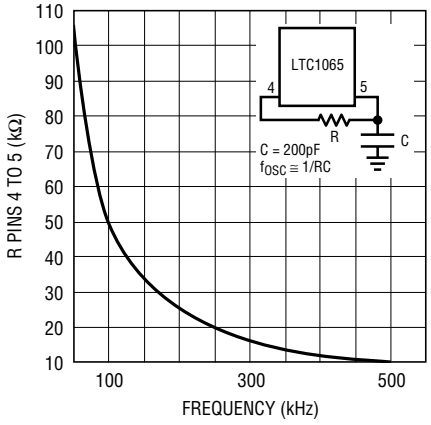
Note 3: The wideband noise specification does not include the clock feedthrough.

Note 4: To properly evaluate the filter's harmonic distortion an inverting output buffer is recommended. An output buffer (although recommended) is not necessarily needed when measuring output DC offset or wideband noise (see Figure 3).

Note 5: The output DC offset is optimized for ±5V supply. The output DC offset shifts when the power supplies change; however this phenomenon is repeatable and predictable.

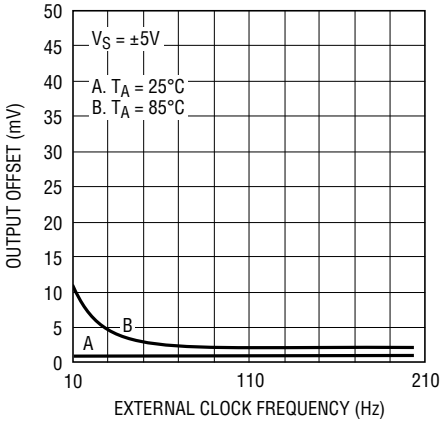
TYPICAL PERFORMANCE CHARACTERISTICS

Self-Clocking Frequency vs R



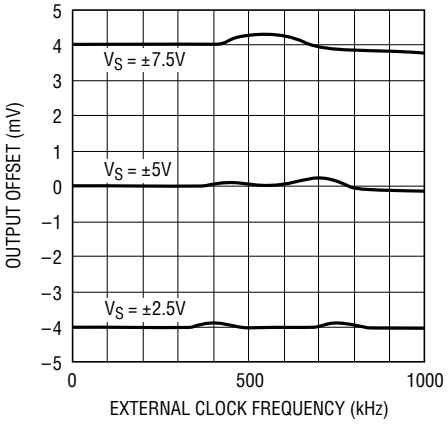
1065 G01

Output Offset vs Clock, Low Clock Rates



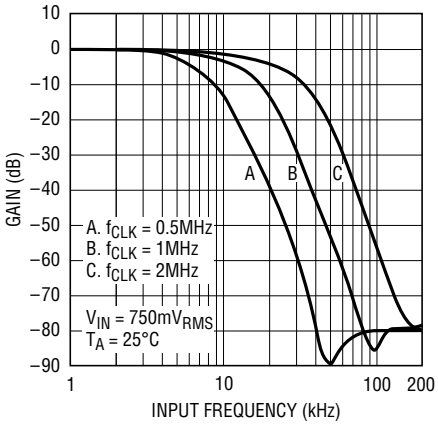
1065 G02

Output Offset vs Clock, Medium Clock Rates



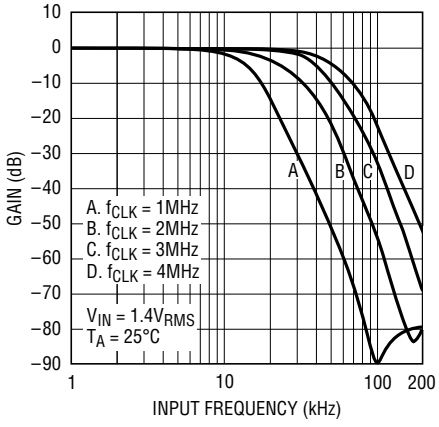
1065 G03

Gain vs Frequency; $V_S = \pm 2.5V$



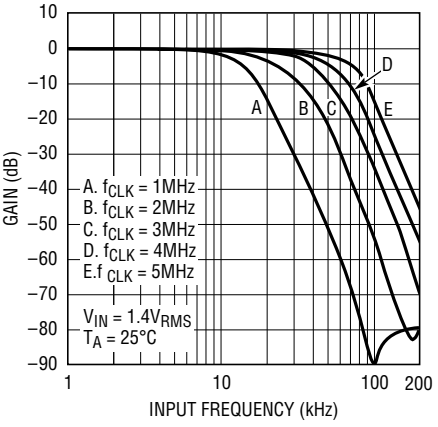
1065 G04

Gain vs Frequency; $V_S = \pm 5V$



1065 G05

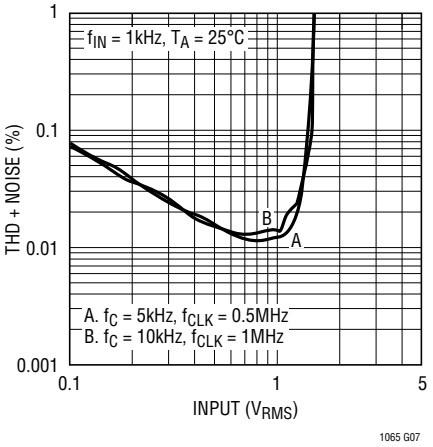
Gain vs Frequency; $V_S = \pm 7.5V$



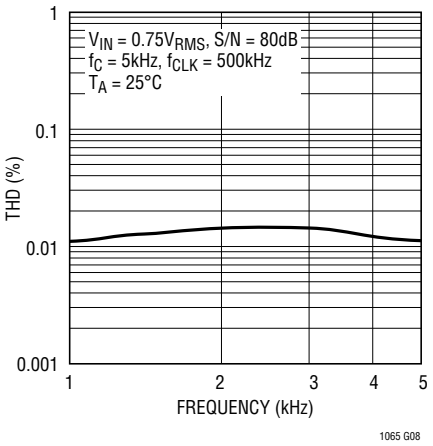
1065 G06

TYPICAL PERFORMANCE CHARACTERISTICS

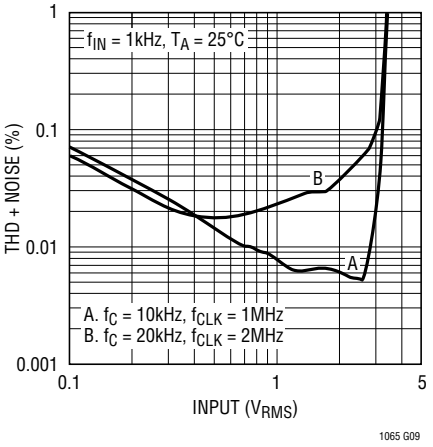
THD + Noise vs Input Voltage; V_S = Single 5V, AGND = 2V



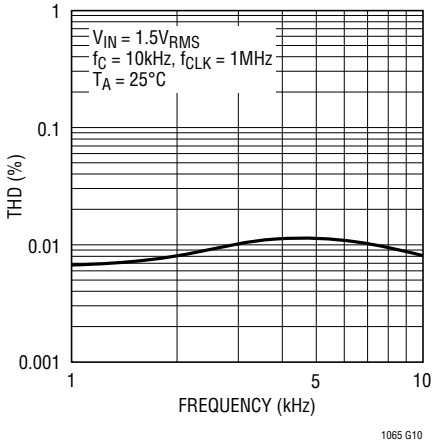
THD vs Frequency; V_S = Single 5V, AGND = 2V



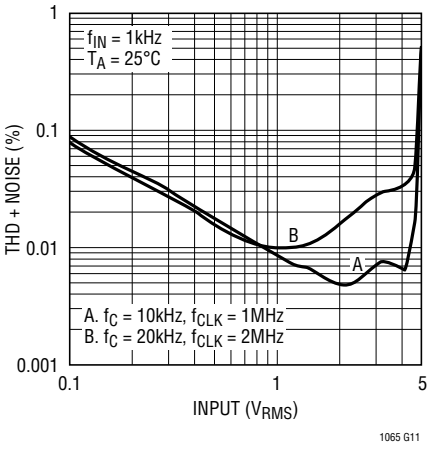
THD + Noise vs Input Voltage; V_S = ±5V



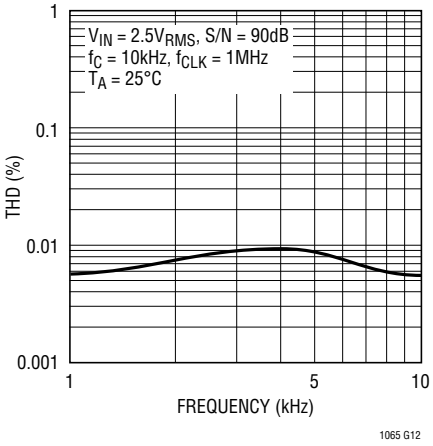
THD vs Frequency; V_S = ±5V



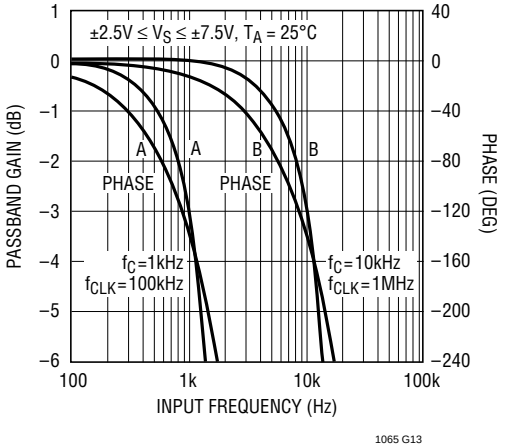
THD + Noise vs Input Voltage; V_S = ±7.5V



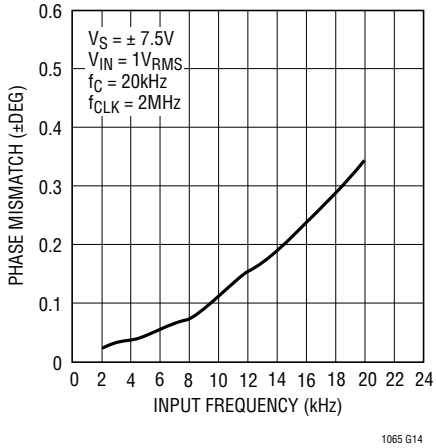
THD vs Frequency; V_S = ±7.5V



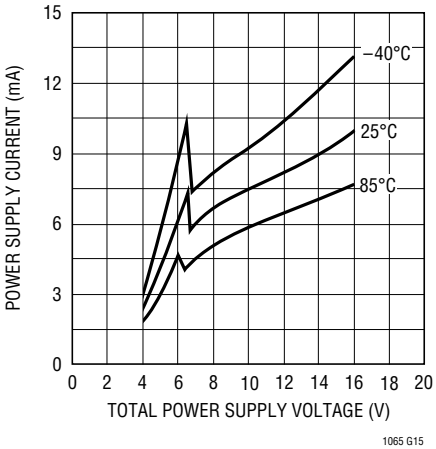
Passband Gain and Phase vs Input Frequency



Typical Phase Matching Device to Device

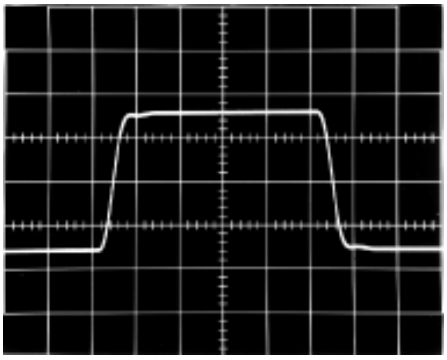


Power Supply Current vs Power Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

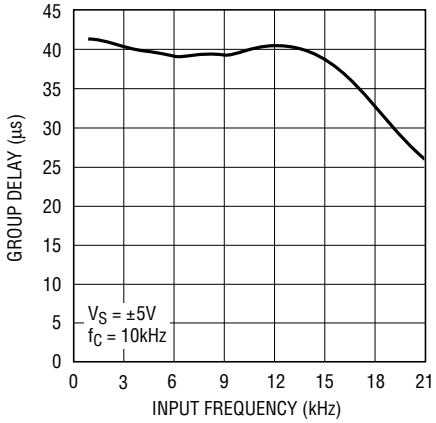
Transient Response



HORIZONTAL: 0.1ms/DIV, VERTICAL: 2V/DIV
V_S = ±5V, f_C = 10kHz, V_{IN} = 1kHz ±3V_P
SQUARE WAVE

1065 G16

Group Delay



1065 G17

PIN FUNCTIONS

Power Supply Pins (Pins 6, 3, N Package)

The positive and negative supply pin should be bypassed with a high quality 0.1µF ceramic capacitor. In applications where the clock pin (5) is externally swept to provide several cutoff frequencies, the output DC offset variation is minimized by connecting an additional 1µF solid tantalum capacitor in parallel with the 0.1µF disc ceramic. This technique was used to generate the graphs of the output DC offset variation versus clock; they are illustrated in the Typical Performance Characteristics section.

When the power supply voltage exceeds ±7V, and when V^- is applied before V^+ (if V^+ is allowed to go below ground) connect a signal diode between the positive supply pin and ground to prevent latch-up (see Typical Applications).

Ground Pin (Pin 2, N Package)

The ground pin merges the internal analog and digital ground paths. The potential of the ground pin is the reference for the internal switched-capacitor resistors, and the reference for the external clock. The positive input of the internal op amp is also tied to the ground pin.

For dual supply operation, the ground pin should be connected to a high quality AC and DC ground. A ground plane, if possible, should be used. A poor ground will degrade DC offset and it will increase clock feedthrough, noise and distortion.

A small amount of AC current flows out of the ground pin whether or not the internal oscillator is used. The frequency of the ground current equals the frequency of the clock. The average value of this current is approximately 55µA, 110µA, 170µA for ±2.5V, ±5V and ±7.5V supplies respectively.

For single supply operation, the ground pin should be preferably biased at half supply (see Typical Applications).

V_{OS} Adjust Pin (Pin 8, N Package)

The V_{OS} adjust pin can be used to trim any small amount of output DC offset voltage or to introduce a desired output DC level. The DC gain from the V_{OS} adjust pin to the filter output pin equals two.

Any DC voltage applied to this pin will reflect at the output pin of the filter multiplied by two.

If the V_{OS} adjust pin is not used, it should be shorted to the ground pin. The DC bias current flowing into the V_{OS} adjust pin is typically 10pA.

The V_{OS} adjust pin should always be connected to an AC ground; AC signals applied to this pin will degrade the filter response.

PIN FUNCTIONS

Input Pin (Pin 1, N Package)

Pin 1 is the filter input and it is connected to an internal switched-capacitor resistor. If the input pin is left floating, the filter output will saturate. The DC input impedance of pin 1 is very high; with ±5V supplies and 1MHz clock, the DC input impedance is typically 1GΩ. A resistor R_{IN} in series with the input pin will not alter the value of the filter's DC output offset (Figure 1). R_{IN} should however, be limited to a maximum value (Table 1), otherwise the filter's pass-band will be affected. Refer to the Applications Information section for more details.

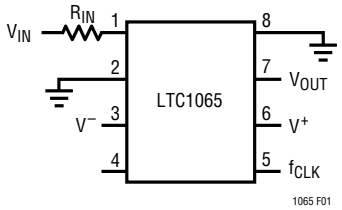


Figure 1.

Table 1. $R_{IN(MAX)}$ vs Clock and Power Supply

	$R_{IN(MAX)}$		
	V_S = ±7.5V	V_S = ±5V	V_S = ±2.5V
f_{CLK} = 4MHz	1.82k	–	–
f_{CLK} = 3MHz	3.01k	2.49k	–
f_{CLK} = 2MHz	4.32k	3.65k	2.37k
f_{CLK} = 1MHz	9.09k	8.25k	7.5k
f_{CLK} = 500kHz	17.8k	16.9k	16.9k
f_{CLK} = 100kHz	95.3k	90.9k	90.9k

Output Pin (Pin 7, N Package)

Pin 7 is the filter output. This pin can typically source over 20mA and sink 2mA. Pin 7 should not drive long coax cables, otherwise the filter's total harmonic distortion will degrade. The maximum load the filter output can drive and still maintain the distortion levels, shown in the Typical Performance Characteristics, is 20k.

Clock Input Pin (Pin 5, N Package)

An external clock, when applied to pin 5, tunes the filter cutoff frequency. The clock-to-cutoff frequency ratio is 100:1. The high (V_{HIGH}) and low (V_{LOW}) clock logic threshold levels are illustrated in Table 2. Square wave clocks with duty cycles between 30% and 50% are strongly recommended. Sinewave clocks are not recommended.

Table 2. Clock Pin Threshold Levels

POWER SUPPLY	V_{HIGH}	V_{LOW}
V_S = ±2.5V	1.5V	0.5V
V_S = ±5V	3V	1V
V_S = ±7.5V	4.5V	1.5V
V_S = ±8V	4.8V	1.6V
V_S = 5V, 0V	4V	3V
V_S = 12V, 0V	9.6V	7.2V
V_S =15V, 0V	12V	9V

Clock Output Pin (Pin 4, N Package)

Any external clock applied to the clock input pin appears at the clock output pin. The duty cycle of the clock output equals the duty cycle of the external clock applied to the clock input pin. The clock output pin swings to the power supply rails. When the LTC1065 is used in a self-clocking mode, the clock of the internal oscillator appears at the clock output pin with a 30% duty cycle. The clock output pin can be used to drive other LTC1065s or other ICs. The maximum capacitance, $C_{L(MAX)}$, the clock output pin can drive is illustrated in Figure 2.

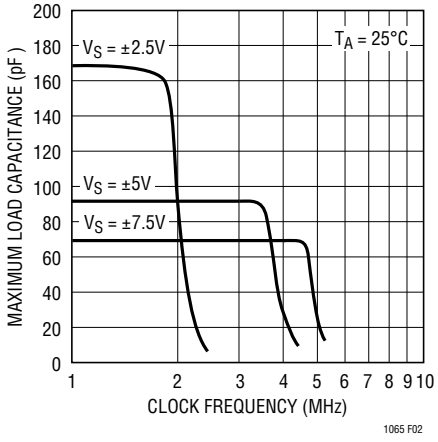


Figure 2. Maximum Load Capacitance at the Clock Output Pin

TEST CIRCUIT

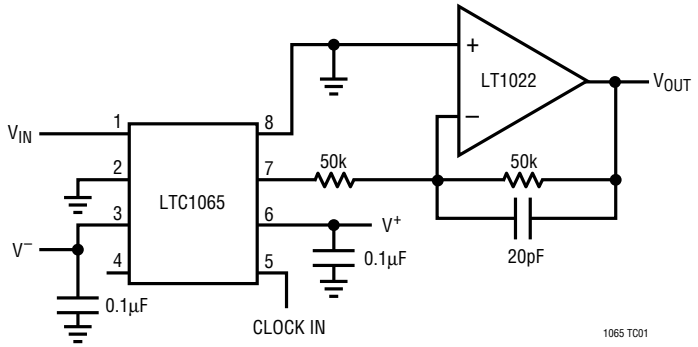


Figure 3. Test Circuit for THD

APPLICATIONS INFORMATION

Self-Clocking Operation

The LTC1065 features an internal oscillator which can be tuned via an external RC. The LTC1065's internal oscillator is primarily intended for generation of clock frequencies below 500kHz. The first curve of the Typical Performance Characteristics section shows how to quickly choose the value of the RC for a given frequency. More precisely, the frequency of the internal oscillator is equal to:

$f_{CLK} = K/RC$

For clock frequencies (f_{CLK}) below 100kHz, K equals 1.07. Figure 4b shows the variation of the parameter K versus clock frequency and power supply. First choose the desired clock frequency ($f_{CLK} < 500kHz$), then through Figure 4b pick the right value of K, set C = 200pF and solve for R.

Example 1: f_{CUTOFF} = 2kHz, f_{CLK} = 200kHz, V_S = ±5V, T_A = 25°C, K = 1.0, C = 200pF

then, $R = (1.0)/(200kHz \times 204pF) = 24.5k$.

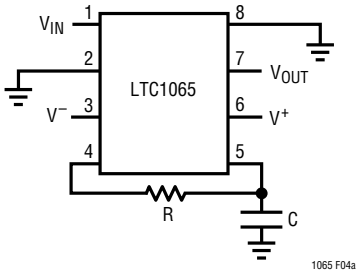


Figure 4a.

Note a 4pF parasitic capacitance is assumed in parallel with the external 200pF timing capacitor. Figure 5 shows the clock frequency variation from –40°C to 85°C. The 200kHz clock of Example 1 will change by –1.75% at 85°C.

For a limited temperature range, the internal oscillator of the LTC1065 can be used to generate clock frequencies above 500kHz (Figures 6 and 7). The data of Figure 6 is derived from several devices. For a given external (RC) value, the observed device-to-device clock frequency variation was ±1% (V_S = ±5V), and ±1.25% for V_S = ±2.5V.

Example 2: f_{CUTOFF} = 20kHz, f_{CLK} = 2MHz, V_S = ±7.5V, T_A = 25°C, C = 10pF

from Figure 6, K = 0.575,

and, $R = (0.575)/(2MHz \times 14pF) = 20.5k$.

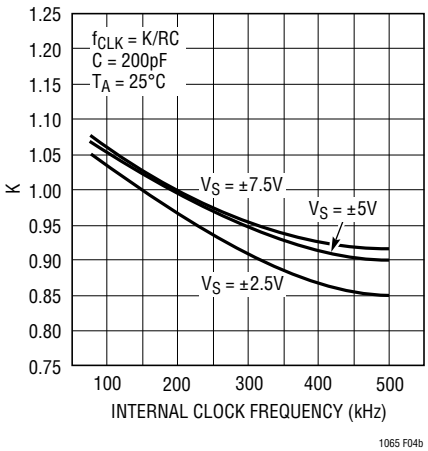


Figure 4b. f_{CLK} vs K

APPLICATIONS INFORMATION

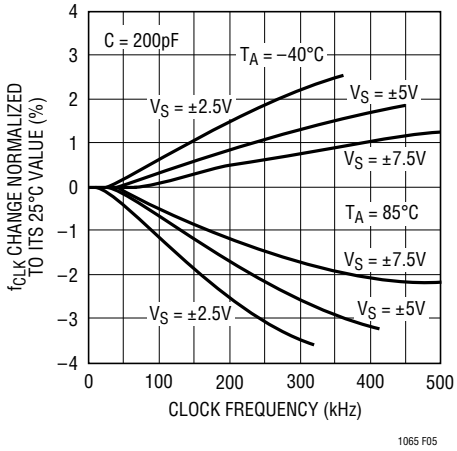


Figure 5. f_{CLK} vs Temperature

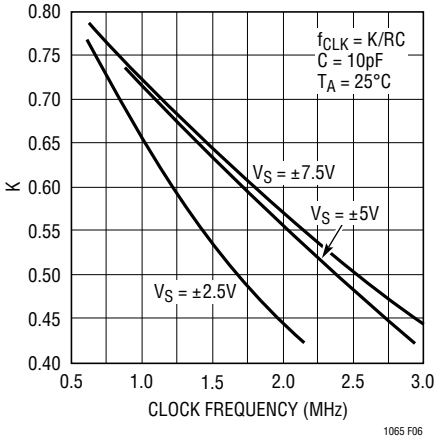


Figure 6. f_{CLK} vs K

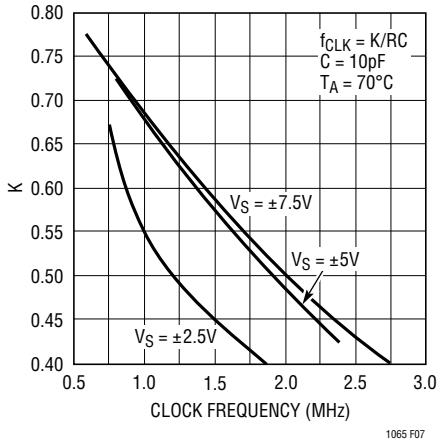


Figure 7. f_{CLK} vs K

A 4pF parasitic capacitance is assumed in parallel with the external 10pF capacitor. A ±1% clock frequency variation from device to device can be expected. The 2MHz clock frequency designed above will typically drift to 1.74MHz at 70°C (Figure 7).

The internal clock of the LTC1065 can be overridden by an external clock provided that the external clock source can drive the timing capacitor C, which is connected from the clock input pin to ground.

Output Offset

The DC output offset of the LTC1065 is trimmed to typically less than ±1mV. The trimming is done at V_S = ±5V. To obtain optimum DC offset performance, appropriate PC layout techniques should be used and the filter IC should be soldered to the PC board. A socket will degrade the output DC offset by typically 1mV. The output DC offset is sensitive to the coupling of the clock output pin 4 (N package) to the negative power supply pin 3 (N package). The negative supply pin should be well decoupled. When the surface mount package is used, all NC pins should be grounded. When the output DC voltage is measured with a voltmeter, the filter output pin should be buffered. Long test leads should be avoided.

With fixed power supplies, the output DC offset should not change by more than ±100µV over 10Hz to 1MHz clock frequency variation. When the filter clock frequency is fixed, the output DC offset will typically change by –4mV (2mV) when the power supply varies from ±5V to ±7.5V (±2.5V). See Typical Performance Characteristics.

Common-Mode Rejection

The common-mode rejection is defined as the change of the output DC offset with respect to the DC change of the input voltage applied to the filter.

$$CMR = 20\log(\Delta V_{OS\ OUT}/\Delta V_{IN})(dB)$$

Table 3 illustrates the common-mode rejection for three power supplies and three temperatures. The common-mode rejection improves if the output offset is adjusted to approximately 0V. The output offset can be adjusted via pin 8 (N package). See Typical Applications.

APPLICATIONS INFORMATION

Table 3. CMR Data, f_{CLK} = 100kHz

POWER SUPPLY	ΔV_{IN}	–40°C	25°C	85°C	25°C (V_{OS} Nulled)
±2.5V	±1.8V	84dB	83dB	80dB	83dB
±5V	±4V	82dB	78dB	77dB	78dB
±7.5V	±6V	80dB	77dB	76dB	80dB

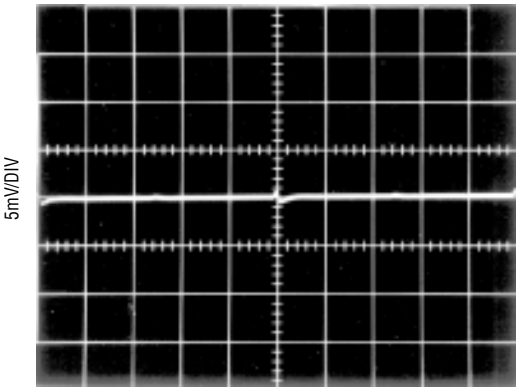
The above data is valid for clock frequencies up to 800kHz, 900kHz, 1MHz, for V_S = ±2.5V, ±5V, ±7.5V respectively.

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics which are present at the filter's output pin. The clock feedthrough is tested with the filter input grounded and it depends on the quality of the PC board layout and power supply decoupling. Any parasitic switching transients during the rise and fall of the incoming clock, are not part of the clock feedthrough specifications; their amplitude strongly depends on scope probing techniques as well as ground quality and power supply bypassing. For a power supply V_S = ±5V, the clock feedthrough of the LTC1065 is 50μV_{RMS}; for V_S = ±7.5V, the clock feedthrough approaches 75μV_{RMS}. Figures 8 and 9 show a typical scope photo of the LTC1065 output pin when the input pin is grounded. The filter cutoff frequency was 1kHz, while scope bandwidth was chosen to be 1MHz so that switching transients above the 100kHz clock frequency would show.

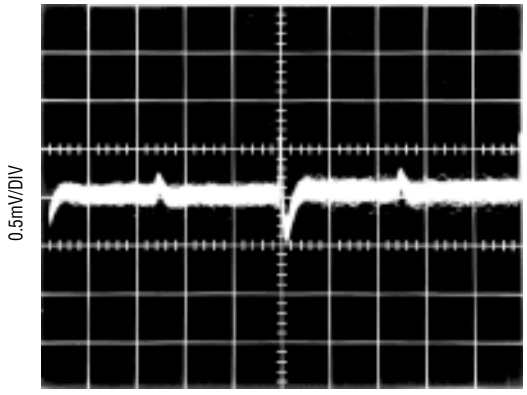
Wideband Noise

The wideband noise data is used to determine the operating signal-to-noise ratio at a given distortion level. The wideband noise (μV_{RMS}) is nearly independent of the value of the clock frequency and excludes the clock feedthrough. The LTC1065's typical wideband noise is 80μV_{RMS}. Figure 9 shows the same scope photo as Figure 8 but with a more sensitive vertical scale. The clock feedthrough is imbedded in the filter's wideband noise. The peak-to-peak wideband noise of the filter can be clearly seen; it is approximately 420μV_{P-P}. Note that 420μV_{P-P} equals the 80μV_{RMS} wideband noise of the part multiplied by a crest factor of 5.25.



f_{CLK} = 100kHz, f_C = 1kHz, V_S = ±5V, 1MHz SCOPE BW

Figure 8. LTC1065 Output Clock Feedthrough + Noise



f_{CLK} = 100kHz, f_C = 1kHz, V_S = ±5V, 1MHz SCOPE BW

Figure 9. LTC1065 Output Clock Feedthrough + Noise

Aliasing

Aliasing is an inherent phenomenon of sampled data filters. It primarily occurs when the frequency of an input signal approaches the sampling frequency. For the LTC1065, an input signal whose frequency is in the range of f_{CLK} ±6% will generate an alias signal into the filter's passband and stopband. Table 4 shows details.

Example: LTC1065, f_{CLK} = 20kHz, f_C = 200kHz,
f_{IN} = (19.6kHz, 100mV_{RMS})
f_{ALIAS} = (400Hz, 3.16mV_{RMS})

APPLICATIONS INFORMATION

Table 4. Aliasing Data

INPUT FREQUENCY	OUTPUT FREQUENCY	OUTPUT AMPLITUDE REFERENCED TO INPUT SIGNAL
0.9995 f_{CLK}	0.0005 f_{CLK}	–0.01 dB
0.995 f_{CLK}	0.005 f_{CLK}	–0.98 dB
0.99 f_{CLK}	0.01 f_{CLK}	–3.13 dB
0.9875 f_{CLK}	0.0125 f_{CLK}	–4.79 dB
0.985 f_{CLK}	0.015 f_{CLK}	–7.21 dB
0.9825 f_{CLK}	0.0175 f_{CLK}	–10.43 dB
0.98 f_{CLK}	0.02 f_{CLK}	–14.14 dB
0.975 f_{CLK}	0.025 f_{CLK}	–21.84 dB
0.97 f_{CLK}	0.03 f_{CLK}	–28.98 dB
0.965 f_{CLK}	0.035 f_{CLK}	–35.31 dB
0.96 f_{CLK}	0.04 f_{CLK}	–40.94 dB
0.955 f_{CLK}	0.045 f_{CLK}	–45.96 dB
0.95 f_{CLK}	0.05 f_{CLK}	–50.46 dB
0.94 f_{CLK}	0.06 f_{CLK}	–58.29 dB
0.93 f_{CLK}	0.07 f_{CLK}	–64.90 dB
0.9 f_{CLK}	0.1 f_{CLK}	–80.20 dB

An input RC can be used to attenuate incoming signals close to the filter clock frequency (Figure 10). A Bessel passband response will be maintained if the value of the input resistor follows Table 1.

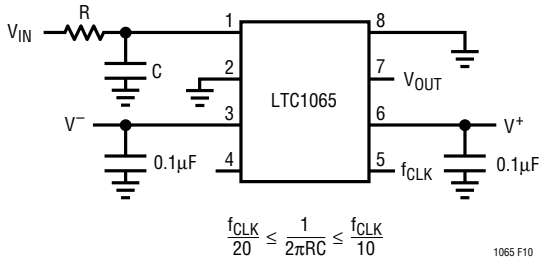
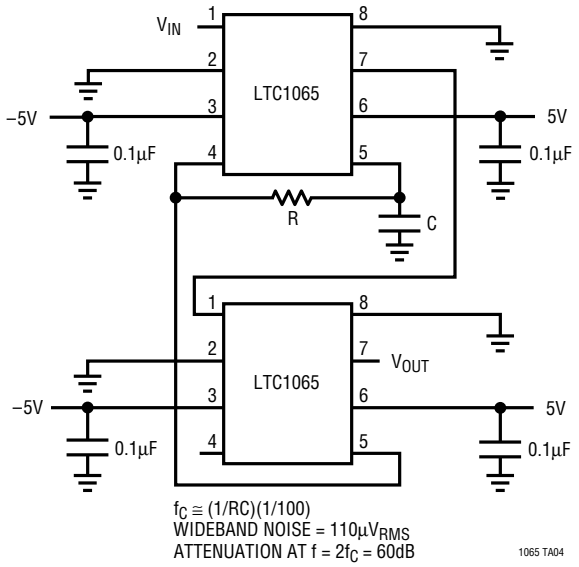


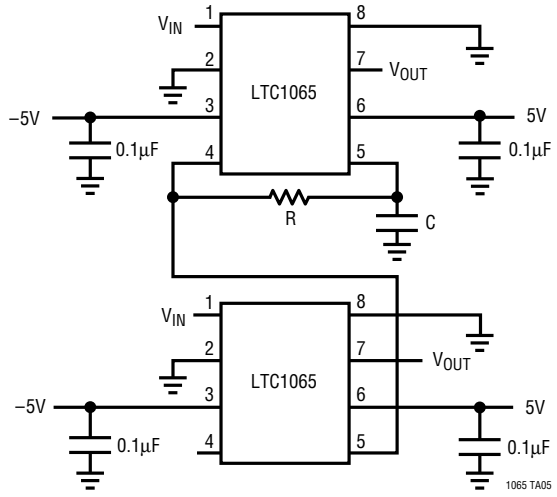
Figure 10. Adding an Input Anti-Aliasing RC

TYPICAL APPLICATIONS

Cascading Two LTC1065s for Steeper Roll-Off

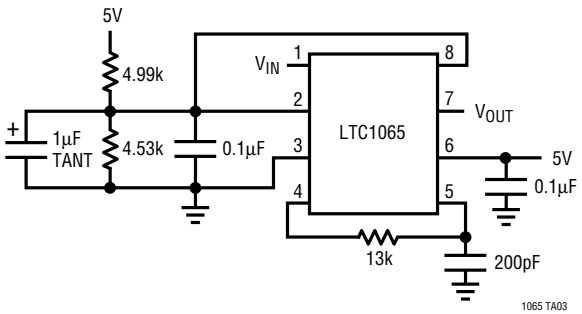


Sharing Clock for Multichannel Applications

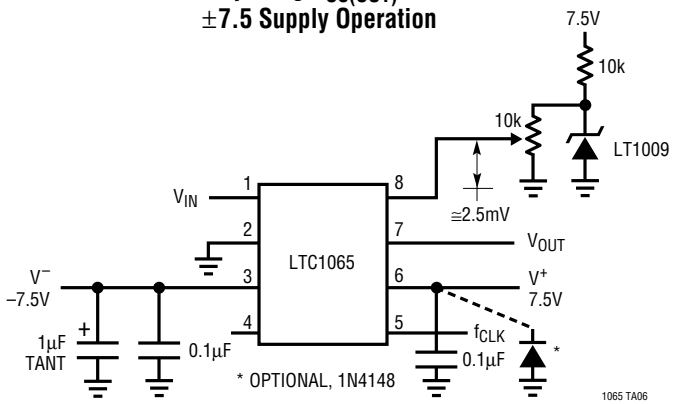


TYPICAL APPLICATIONS

Single 5V Supply Operation (f_C = 3.4kHz)



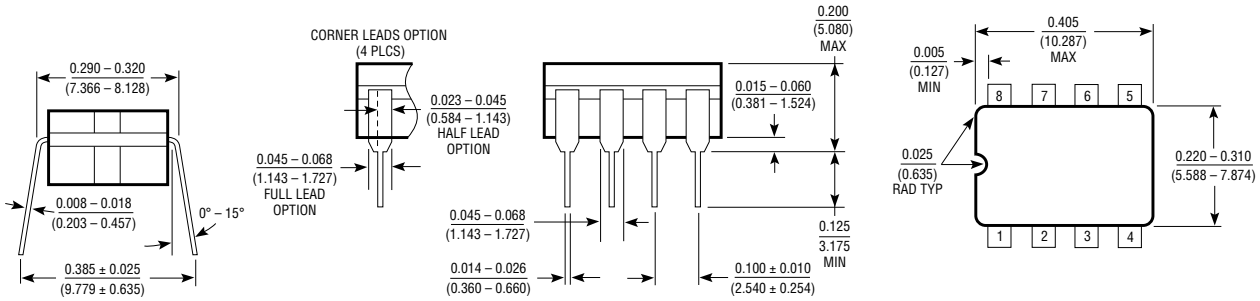
Adjusting $V_{OS(OUT)}$ for ±7.5 Supply Operation



PACKAGE DESCRIPTION

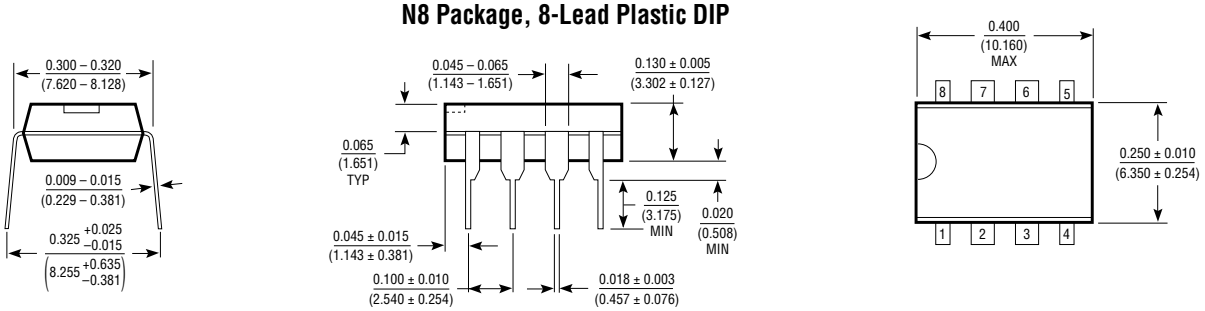
Dimensions in inches (millimeters) unless otherwise noted.

J8 Package, 8-Lead Ceramic DIP

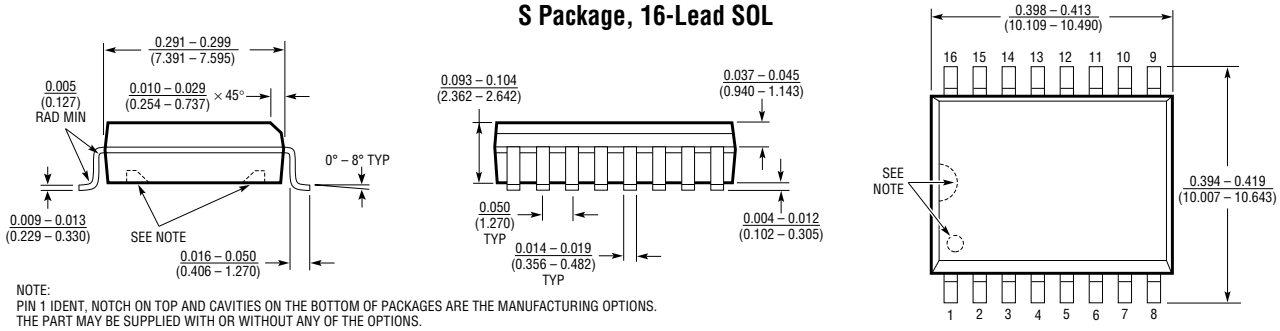


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

N8 Package, 8-Lead Plastic DIP



S Package, 16-Lead SOL



NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

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