

FEATURES

- *Guaranteed* Max. Offset 5 μ V
- *Guaranteed* Max. Offset Drift 0.05 μ V/°C
- Typ. Offset Drift 0.01 μ V/°C
- Excellent Long Term Stability 100nV/ $\sqrt{\text{Month}}$
- *Guaranteed* Max. Input Bias Current 30pA
- Over Operating Temperature Range
 - Guaranteed* Min. Gain 120dB
 - Guaranteed* Min. CMRR 120dB
 - Guaranteed* Min. PSRR 120dB
- Single Supply Operation 4.75V to 16V
 (Input Voltage Range Extends to Ground)
- External Capacitors can be Returned to V⁻ with No Noise Degradation

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

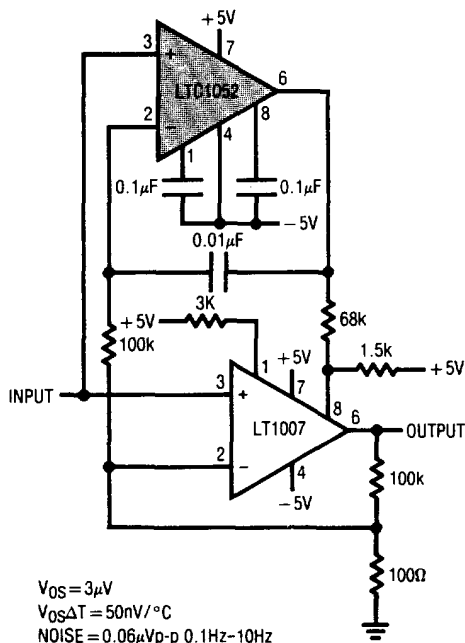
The LTC1052 and LTC7652 are low noise Chopper-stabilized op amps (CSOA™) manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Chopper-stabilization constantly corrects offset voltage errors. Both initial offset and changes in the offset due to time, temperature and common-mode voltage are corrected. This, coupled with picoampere input currents, gives these amplifiers unmatched performance.

Low frequency (1/f) noise is also improved by the chopping technique. Instead of increasing continuously at a 3dB/octave rate, the internal chopping causes noise to decrease at low frequencies.

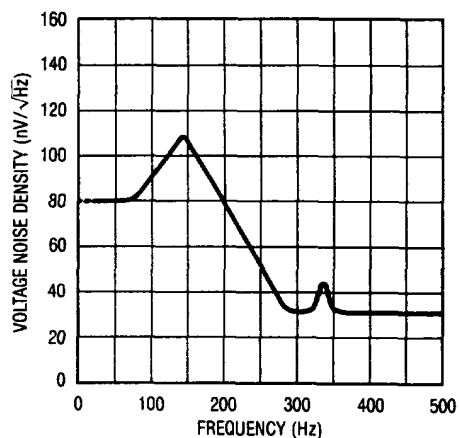
The chopper circuitry is entirely internal and completely transparent to the user. Only two external capacitors are required to alternately sample and hold the offset correction voltage and the amplified input signal. Control circuitry is brought out on the 14-pin version to allow the sampling of the LTC1052 to be synchronized with an external frequency source.

2

Ultra Low Noise, Low Drift Amplifier



LTC1052 Noise Spectrum



CSOA™ and LTCMOS™ are trademarks of Linear Technology Corporation.
 Teflon™ is a trademark of DuPont.

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Total Supply Voltage (V^+ to V^-)	18V
Input Voltage	($V^+ + 0.3V$) to ($V^- - 0.3V$)
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LTC1052C/LTC7652C	-40°C to 85°C
LTC1052M	-55°C to 125°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER	REPLACES
<p>METAL CAN H PACKAGE</p>	LTC7652CH LTC1052CH LTC1052MH	ICL7652CTV ICL7652ITV ICL7650CTV-1 ICL7650ITV-1 ICL7650CTV ICL7650ITV ICL7650MTV
<p>HERMETIC DIP J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>	LTC1052CN8 LTC1052CJ8 LTC1052MJ8	ICL7650CPA ICL7650IJA
<p>HERMETIC DIP J14 PACKAGE PLASTIC DIP N14 PACKAGE</p>	LTC1052CJ LTC1052CN LTC1052MJ	ICL7652IJD ICL7650IJD ICL7652CPD ICL7650CPD ICL7650MJD

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $T_A =$ operating temperature range, test circuit TC1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC1052M			LTC1052C/LTC7652C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$T_A = 25^\circ C$ (Note 3)	± 0.5	± 5		± 0.5	± 5		μV
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Drift	(Note 3)	± 0.01	± 0.05		± 0.01	± 0.05		$\mu V/^\circ C$
$\Delta V_{OS}/\Delta Time$	Long Term Offset Voltage Stability			100			100		nV/ \sqrt{Month}
I_{OS}	Input Offset Current	$T_A = 25^\circ C$	± 5	± 30 ± 2000		± 5	± 30 ± 350		pA pA
I_B	Input Bias Current	$T_A = 25^\circ C$	± 1	± 30 ± 1000		± 1	± 30 ± 175		pA pA
e_{np-p}	Input Noise Voltage	$R_S = 100\Omega$, DC to 10Hz, TC3 $R_S = 100\Omega$, DC to 1Hz, TC3		1.5 0.5			1.5 0.5		$\mu Vp-p$ $\mu Vp-p$
i_n	Input Noise Current	$f = 10Hz$ (Note 5)		0.6			0.6		fA/ \sqrt{Hz}
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to $+2.7V$	120	140		120	140		dB
PSRR	Power Supply Rejection Ratio	$V_{SUPPLY} = \pm 2.375V$ to $\pm 8V$	120	150		120	150		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 10k$, $V_{OUT} = \pm 4V$	120	150		120	150		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	$R_L = 10k$ $R_L = 100k$	± 4.7	± 4.85 ± 4.95		± 4.7	± 4.85 ± 4.95		V V
SR	Slew Rate	$R_L = 10k$, $C_L = 50pF$		4			4		V/ μs
GBW	Gain Bandwidth Product			1.2			1.2		MHz
I_S	Supply Current	No Load, $T_A = 25^\circ C$		1.7 2.0 3.0			1.7 2.0 3.0		mA mA mA
f_S	Internal Sampling Frequency			330			330		Hz
	Clamp On Current	$R_L = 100k$	25	100		25	100		μA
	Clamp Off Current	$-4V < V_{OUT} < +4V$		10 100 2			10 100 1		pA pA nA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1052/LTC7652.

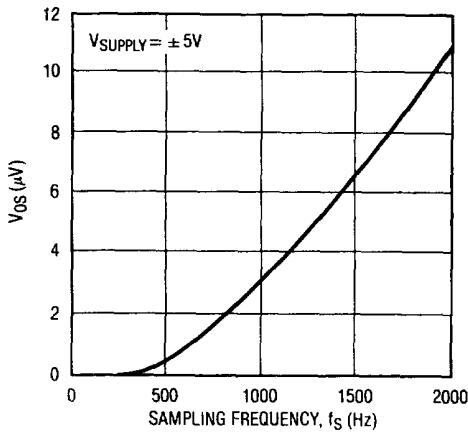
Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic testing. V_{OS} is measured to a limit determined by test equipment capability. Voltages on C_{EXTA} and C_{EXTB} , A_{VOL} , CMRR and PSRR are measured to insure proper operation of the nulling loop to insure meeting the V_{OS} and V_{OS} drift specifications. See Package-Induced V_{OS} in applications section.

Note 4: Output clamp not connected.

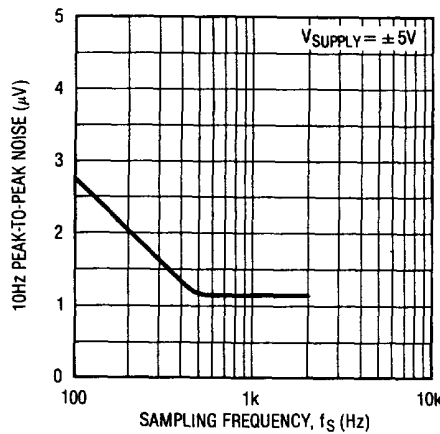
Note 5: Current noise is calculated from the formula: $i_n = (2q I_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb.

TYPICAL PERFORMANCE CHARACTERISTICS

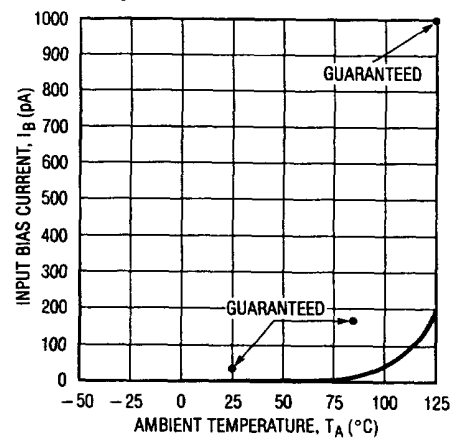
Offset Voltage vs Sampling Frequency



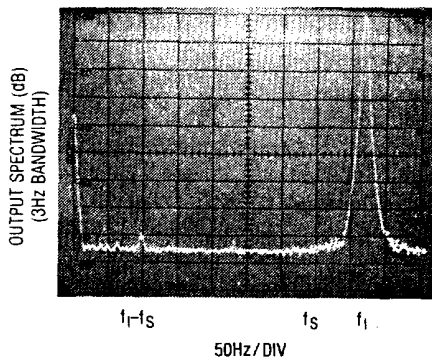
10Hzp-p Noise vs Sampling Frequency



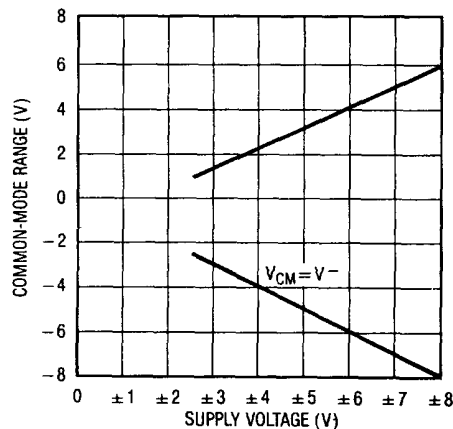
Input Bias Current vs Temperature



Aliasing Error



Common-Mode Input Range vs Supply Voltage



Overload Recovery (Output Clamp Not Used)

