Chopper-Stabilized Operational Amplifier (CSOA™)

FEATURES

- *Guaranteed* Max. Offset 5μV
- *Guaranteed* Max. Offset Drift 0.05μV/°C
- Typ. Offset Drift 0.01μV/°C
- Excellent Long Term Stability 100nV/√Month
- *Guaranteed* Max. Input Bias Current 30pA
- Over Operating Temperature Range
  - *Guaranteed* Min. Gain 120dB
  - *Guaranteed* Min. CMRR 120dB
  - *Guaranteed* Min. PSRR 120dB
- Single Supply Operation 4.75V to 16V (Input Voltage Range Extends to Ground)
- External Capacitors can be Returned to V^- with No Noise Degradation

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Low Level Signal Processing
- Medical Instrumentation

DESCRIPTION

The LTC1052 and LTC7652 are low noise Chopper-stabilized op amps (CSOA™) manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. Chopper-stabilization constantly corrects offset voltage errors. Both initial offset and changes in the offset due to time, temperature and common-mode voltage are corrected. This, coupled with picoampere input currents, gives these amplifiers unmatched performance.

Low frequency (1/f) noise is also improved by the chopping technique. Instead of increasing continuously at a 3dB/octave rate, the internal chopping causes noise to decrease at low frequencies.

The chopper circuitry is entirely internal and completely transparent to the user. Only two external capacitors are required to alternately sample and hold the offset correction voltage and the amplified input signal. Control circuitry is brought out on the 14-pin version to allow the sampling of the LTC1052 to be synchronized with an external frequency source.

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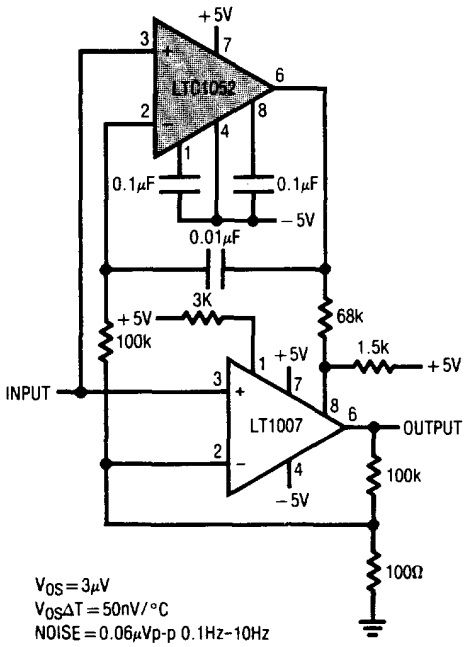
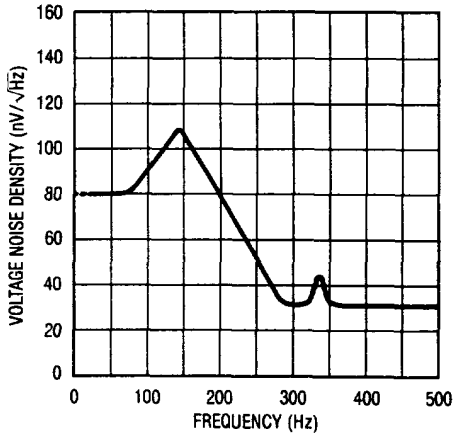
Ultra Low Noise, Low Drift Amplifier



$V_{OS} = 3\mu V$
$V_{OS}\Delta T = 50nV/°C$
NOISE = 0.06μVp-p 0.1Hz-10Hz

LTC1052 Noise Spectrum

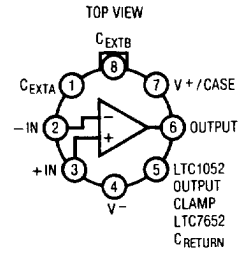


ABSOLUTE MAXIMUM RATINGS

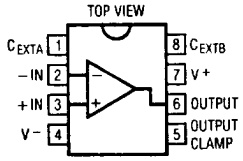
(Notes 1 and 2)

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage . . . . . ($V^+ + 0.3V$) to ($V^- - 0.3V$)
Output Short Circuit Duration . . . . . Indefinite
Operating Temperature Range
LTC1052C/LTC7652C . . . . . −40°C to 85°C
LTC1052M . . . . . −55°C to 125°C
Storage Temperature Range . . . . . −55°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C

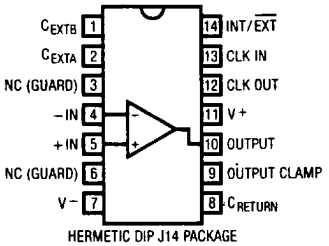
PACKAGE/ORDER INFORMATION



METAL CAN H PACKAGE



HERMETIC DIP J8 PACKAGE
PLASTIC DIP N8 PACKAGE



HERMETIC DIP J14 PACKAGE
PLASTIC DIP N14 PACKAGE

ORDER PART NUMBER	REPLACES
LTC7652CH	ICL7652CTV ICL7652ITV ICL7650CTV-1 ICL7650ITV-1
LTC1052CH	ICL7650CTV ICL7650ITV
LTC1052MH	ICL7650MTV
LTC1052CN8 LTC1052CJ8 LTC1052MJ8	ICL7650CPA ICL7650IJA
LTC1052CJ	ICL7652IJD ICL7650IJD
LTC1052CN	ICL7652CPD ICL7650CPD
LTC1052MJ	ICL7650MJD

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, T_A = operating temperature range, test circuit TC1, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1052M MIN	LTC1052M TYP	LTC1052M MAX	LTC1052C/LTC7652C MIN	LTC1052C/LTC7652C TYP	LTC1052C/LTC7652C MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25°C$ (Note 3)			±0.5	±5		±0.5	±5	μV
$\Delta V_{OS}/\Delta Temp$	Average Input Offset Drift	(Note 3)	●		±0.01	±0.05		±0.01	±0.05	μV/°C
$\Delta V_{OS}/\Delta Time$	Long Term Offset Voltage Stability				100			100		nV/√Month
I_{OS}	Input Offset Current	$T_A = 25°C$			±5	±30		±5	±30	pA
			●			±2000			±350	pA
I_B	Input Bias Current	$T_A = 25°C$			±1	±30		±1	±30	pA
			●			±1000			±175	pA
e_{np-p}	Input Noise Voltage	$R_S = 100\Omega$, DC to 10Hz, TC3			1.5			1.5		μVp-p
		$R_S = 100\Omega$, DC to 1Hz, TC3			0.5			0.5		μVp-p
i_n	Input Noise Current	f = 10Hz (Note 5)			0.6			0.6		fA/√Hz
CMRR	Common-Mode Rejection Ratio	$V_{CM} = V^-$ to +2.7V	●	120	140		120	140		dB
PSRR	Power Supply Rejection Ratio	$V_{SUPPLY} = \pm 2.375V$ to $\pm 8V$	●	120	150		120	150		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 10k$, $V_{OUT} = \pm 4V$	●	120	150		120	150		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	$R_L = 10k$	●	±4.7	±4.85		±4.7	±4.85		V
		$R_L = 100k$			±4.95			±4.95		V
SR	Slew Rate	$R_L = 10k$, $C_L = 50pF$			4			4		V/μs
GBW	Gain Bandwidth Product				1.2			1.2		MHz
I_S	Supply Current	No Load, $T_A = 25°C$			1.7	2.0		1.7	2.0	mA
			●			3.0			3.0	mA
f_S	Internal Sampling Frequency				330			330		Hz
	Clamp On Current	$R_L = 100k$	●	25	100		25	100		μA
	Clamp Off Current	$-4V < V_{OUT} < +4V$			10	100		10	100	pA
			●			2			1	nA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1052/LTC7652.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic testing. V_{OS} is measured to a limit determined by test equipment capability. Voltages on C_{EXTA} and C_{EXTB}, A_{VOL}, CMRR and PSRR are measured to insure proper operation of the nulling loop to insure meeting the V_{OS} and V_{OS} drift specifications. See Package-Induced V_{OS} in applications section.

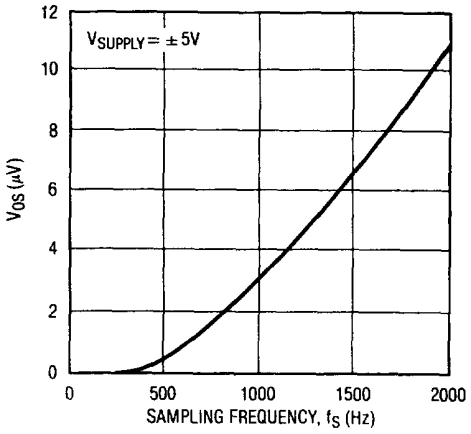
Note 4: Output clamp not connected.

Note 5: Current noise is calculated from the formula: $i_n = (2q\ I_B)^{1/2}$, where $q = 1.6 \times 10^{-19}$ coulomb.

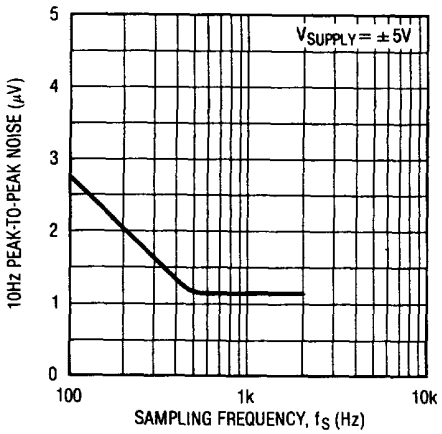
TYPICAL PERFORMANCE CHARACTERISTICS

2

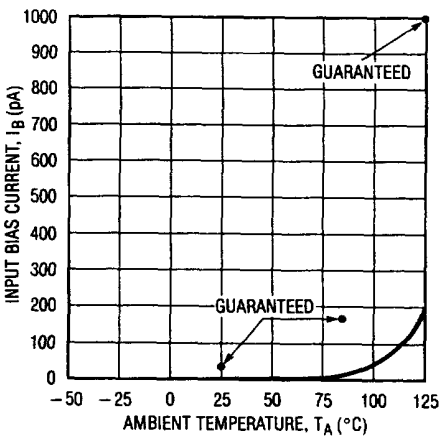
Offset Voltage vs Sampling Frequency



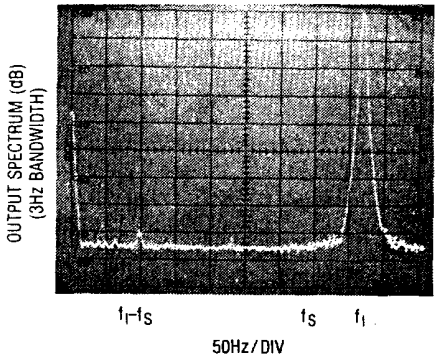
10Hzp-p Noise vs Sampling Frequency



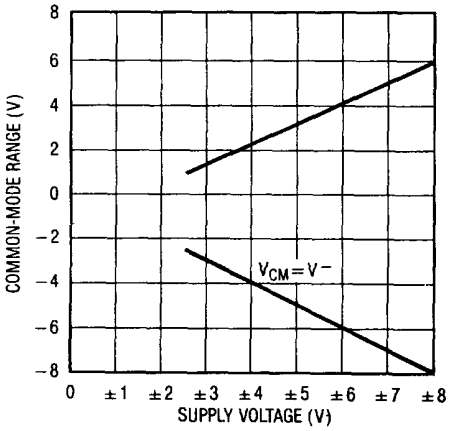
Input Bias Current vs Temperature



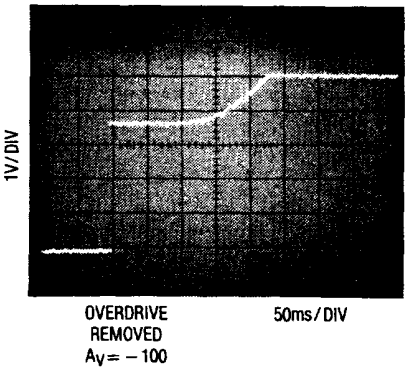
Aliasing Error



Common-Mode Input Range vs Supply Voltage

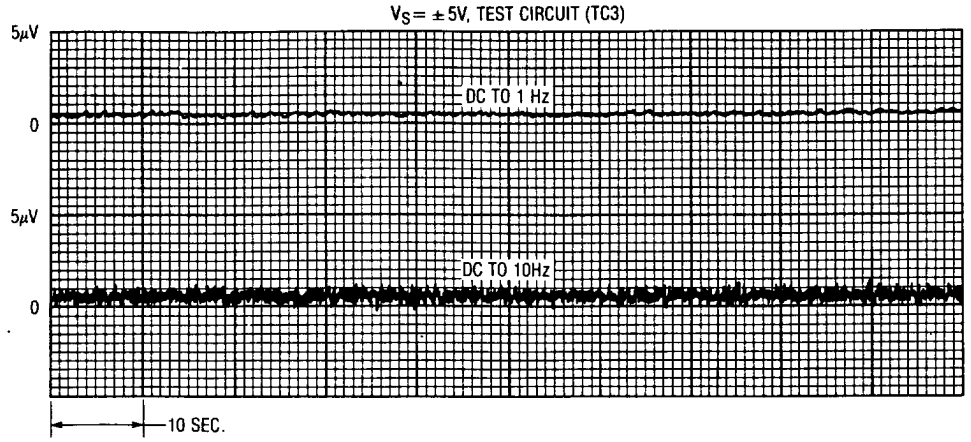


Overload Recovery (Output Clamp Not Used)



TYPICAL PERFORMANCE CHARACTERISTICS

Input Noise Voltage



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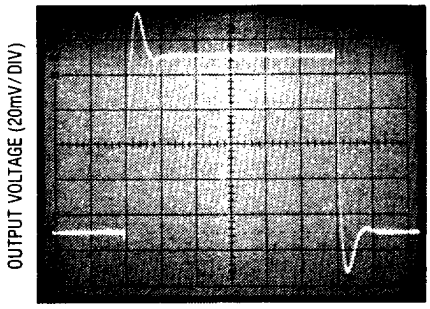
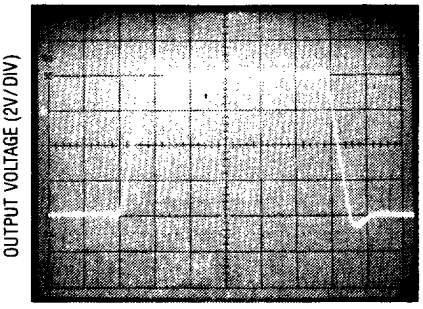
Small Signal Transient Response*



$A_V = +1$ 2μs/DIV
$R_L = 10k$
$C_L = 100pF$
$V_S = \pm 5V$

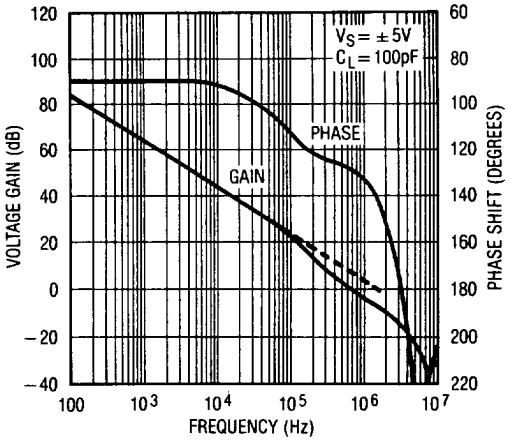
Large Signal Transient Response*



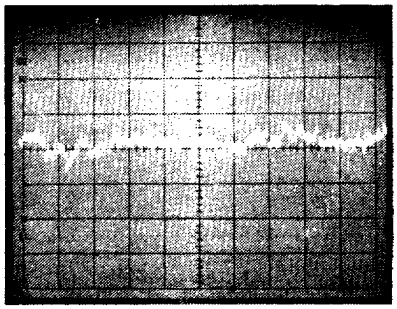
$A_V = +1$ 2μs/DIV
$R_L = 10k$
$C_L = 100pF$
$V_S = \pm 5V$

*RESPONSE IS NOT DEPENDENT ON PHASE OF CLOCK

Gain Phase vs Frequency

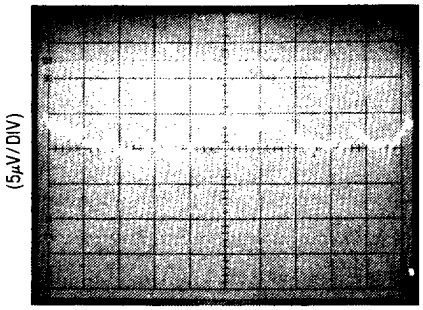


Broadband Noise, $C_{EXT} = 0.1\mu F$



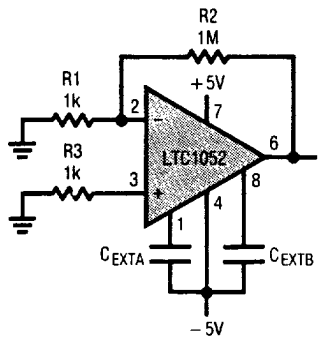
$A_V = -1000$ 1ms/DIV

Broadband Noise, $C_{EXT} = 1.0\mu F$



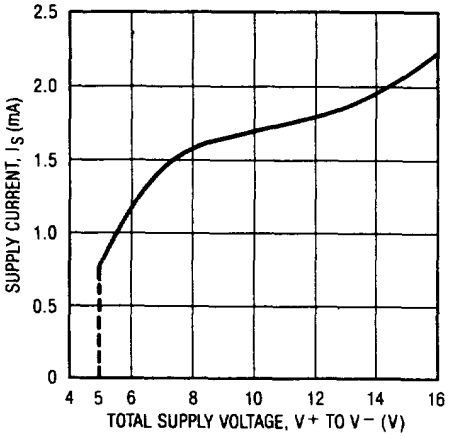
$A_V = -1000$ 1ms/DIV

Broadband Noise Test Circuit (TC2)

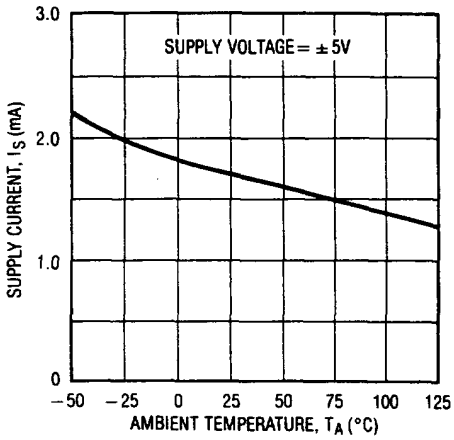


TYPICAL PERFORMANCE CHARACTERISTICS

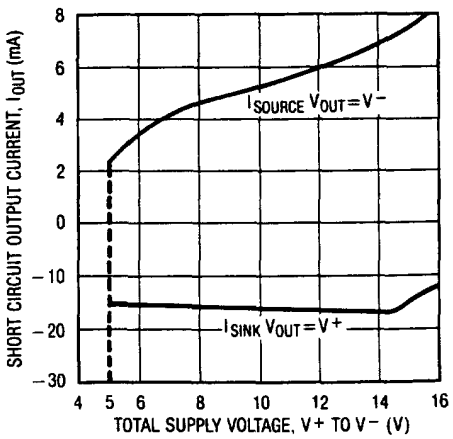
Supply Current vs Supply Voltage



Supply Current vs Temperature

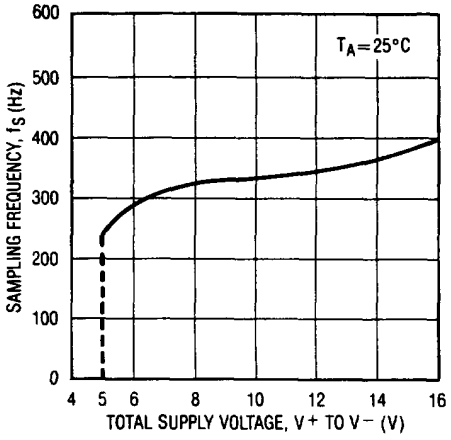


Output Short Circuit Current vs Supply Voltage

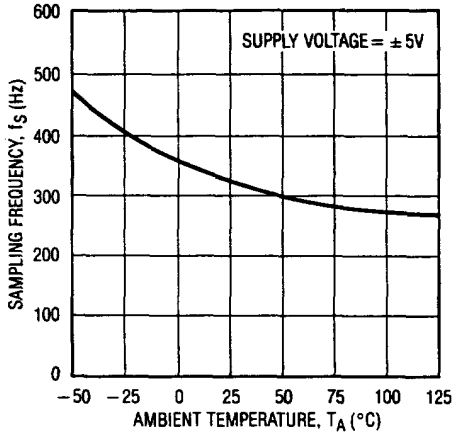


2

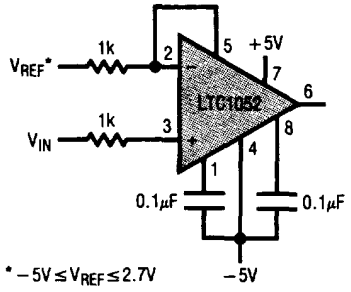
Sampling Frequency vs Supply Voltage



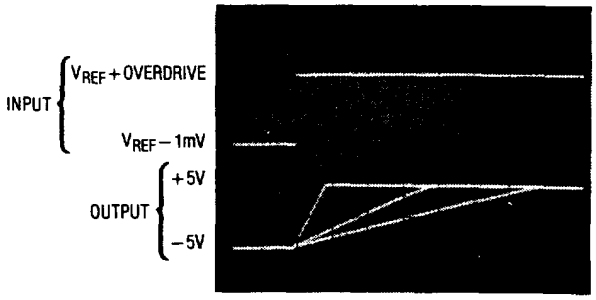
Sampling Frequency vs Temperature



Comparator Operation

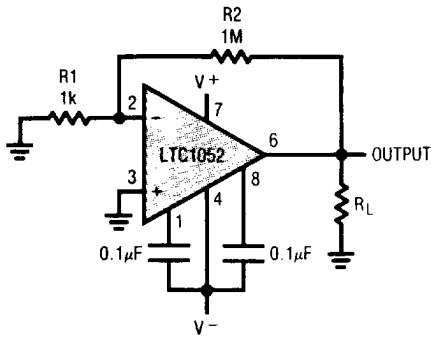


Response Time vs Overdrive

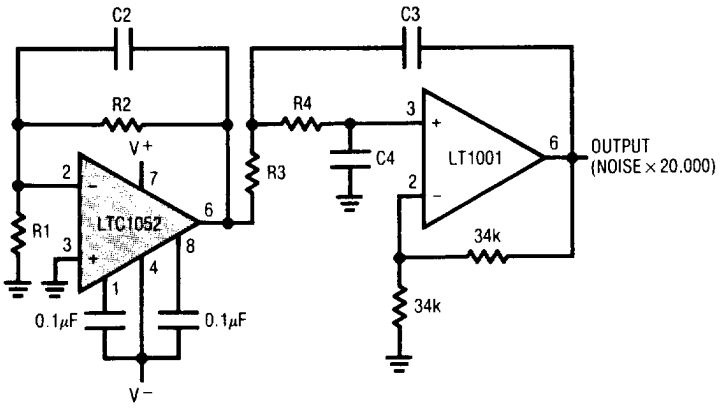


TEST CIRCUITS

Electrical Characteristics Test Circuit (TC1)



DC to 10Hz and DC to 1Hz Noise Test Circuit (TC3)



BANDWIDTH	R1	R2	R3	R4	C2	C3	C4
10Hz	16.2Ω	162k	16.2k	16.2k	0.1μF	1.0μF	1.0μF
1Hz	16.2Ω	162k	162k	162k	1.0μF	1.0μF	1.0μF

THEORY OF OPERATION

DC OPERATION

The shaded portion of the LTC1052 block diagram (Figure 1) entirely determines the amplifier's DC characteristics. During the auto-zero portion of the cycle, the inputs are shorted together and a feedback path is closed around the input stage to null its offset. Switch S2 and capacitor C_{EXTA} act as a sample and hold to store the nulling voltage during the next step—the sampling cycle.

In the sampling cycle, the zeroed amplifier is used to amplify the differential input voltage. Switch S2 connects the amplified input voltage to C_{EXTB} and the output gain stage. C_{EXTB} and S2 act as a sample and hold to store the amplified input signal during the auto-zero cycle. By switching between these two states at a frequency much higher than the signal frequency, a continuous output results.

Notice that during the auto-zero cycle the inputs are not only shorted together, but are also shorted to the negative input. This forces nulling with the common-mode voltage present and accounts for the extremely high CMRR of the LTC1052. In the same fashion, variations in power supply are also nulled. For nulling to take place, the offset voltage, common-mode voltage and power supply must not change at a frequency which is high compared to the frequency response of the nulling loop.

AC OPERATION AND ALIASING ERRORS

So far, the DC performance of the LTC1052 has been explained. As the input signal frequency increases, the problem of aliasing must be addressed. Aliasing is the spurious formation of low and high frequency signals caused by the mixing of the input signal with the sampling frequency, f_S. The frequency of the error signals, f_E, is:

$$f_E = f_S \pm f_I$$

where f_I = input signal frequency.

Normally it is the difference frequency ($f_S - f_I$) which is of concern because the high frequency ($f_S + f_I$) can be easily filtered. As the input frequency approaches the sampling frequency, the difference frequency approaches zero and will cause DC errors—the exact problem that the chopping amplifier is meant to eliminate.

The solution is simple. Filter the input so the sampling loop never sees any frequency near the sampling frequency.

At a frequency well below the sampling frequency, the LTC1052 forces I_1 to equal I_2 (see Figure 1B). This makes δI zero, thus the gain of the sampling loop zero at this and higher frequencies—i.e., a low pass filter. The corner frequency of this low pass filter is set by the output stage pole ($1/R_{L4}\ g_{m5}\ R_{L5}\ C2$).