

FEATURES

- Very Low Noise: $0.75\mu\text{V}_{\text{P-P}}$ Typ, 0.1Hz to 10Hz
- DC to 1Hz Noise Lower Than OP-07
- Full Output Swing into 1k Load
- Offset Voltage: $10\mu\text{V}$ Max
- Offset Voltage Drift: $50\text{nV}/^\circ\text{C}$ Max
- Common-Mode Rejection Ratio: 110dB Min
- Power Supply Rejection Ratio: 115dB Min
- No External Components Required
- Pin-Compatible with Standard 8-Pin Op Amps

APPLICATIONS

- Electronic Scales
- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- High Resolution Data Acquisition
- Low Noise Transducers
- Instrumentation Amplifiers

DESCRIPTION

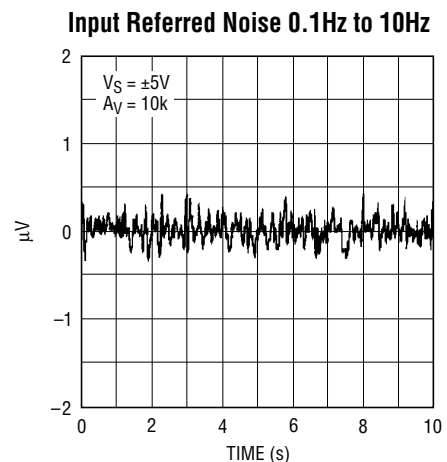
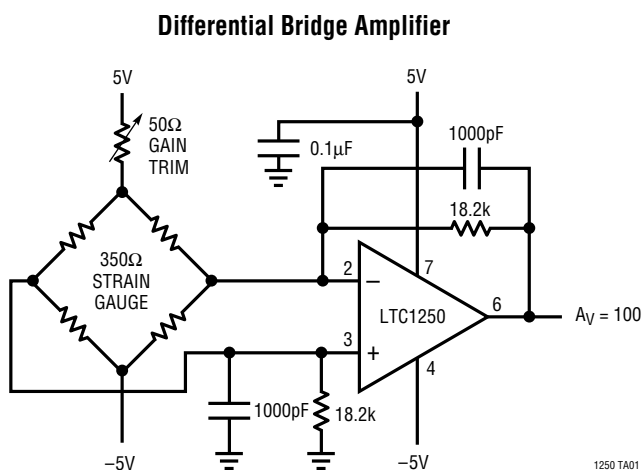
The LTC[®]1250 is a high performance, very low noise zero-drift operational amplifier. The LTC1250's combination of low front-end noise and DC precision makes it ideal for use with low impedance bridge transducers. The LTC1250 features typical input noise of $0.75\mu\text{V}_{\text{P-P}}$ from 0.1Hz to 10Hz, and $0.2\mu\text{V}_{\text{P-P}}$ from 0.1Hz to 1Hz. The LTC1250 has DC to 1Hz noise of $0.35\mu\text{V}_{\text{P-P}}$, surpassing that of low noise bipolar parts including the OP-07, OP-77, and LT1012. The LTC1250 uses the industry-standard single op amp pinout, and requires no external components or nulling signals, allowing it to be a plug-in replacement for bipolar op amps.

The LTC1250 incorporates an improved output stage capable of driving 4.3V into a 1k load with a single 5V supply; it will swing $\pm 4.9\text{V}$ into 5k with $\pm 5\text{V}$ supplies. The input common mode range includes ground with single power supply voltages above 12V. Supply current is 3mA with a $\pm 5\text{V}$ supply, and overload recovery times from positive and negative saturation are 0.5ms and 1.5ms, respectively. The internal nulling clock is set at 5kHz for optimum low frequency noise and offset drift; no external connections are necessary.

The LTC1250 is available in standard 8-pin ceramic and plastic DIPs, as well as an 8-pin SOIC package.

LT and LTC are registered trademarks and LT is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	18V
Input Voltage	($V^+ + 0.3V$) to ($V^- - 0.3V$)
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LTC1250M	-55°C to 125°C
LTC1250C	0°C TO 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

<p>J8 PACKAGE 8-LEAD CERAMIC DIP</p> <p>N8 PACKAGE 8-LEAD PLASTIC DIP</p> <p>S8 PACKAGE 8-LEAD PLASTIC SOIC</p> <p>$T_{JMAX} = 150^\circ\text{C}, \theta_{JA} = 100^\circ\text{C/W (J8)}$ $T_{JMAX} = 110^\circ\text{C}, \theta_{JA} = 130^\circ\text{C/W (N8)}$ $T_{JMAX} = 110^\circ\text{C}, \theta_{JA} = 200^\circ\text{C/W (S8)}$</p>	ORDER PART NUMBER
	LTC1250MJ8 LTC1250CJ8 LTC1250CN8 LTC1250CS8
	S8 PART MARKING
	1250

ELECTRICAL CHARACTERISTICS

$V_{IN} = \pm 5V, T_A = \text{Operating Temperature Range, unless otherwise noted.}$

SYMBOL	PARAMETER	CONDITIONS	LTC1250M			LTC1250C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$T_A = 25^\circ\text{C}$ (Note 1)		± 5	± 10		± 5	± 10	μV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●	± 0.01	± 0.05		± 0.01	± 0.05	$\mu\text{V}/^\circ\text{C}$
	Long Term Offset Drift			50			50		$\text{nV}/\sqrt{\text{Mo}}$
e_n	Input Noise Voltage (Note 2)	$T_A = 25^\circ\text{C}, 0.1\text{Hz to } 10\text{Hz}$ $T_A = 25^\circ\text{C}, 0.1\text{Hz to } 1\text{Hz}$		0.75 0.2	1.0		0.75 0.2	1.0	μV_{P-P} μV_{P-P}
i_n	Input Noise Current	$f = 10\text{Hz}$		4.0			4.0		$\text{fA}/\sqrt{\text{Hz}}$
I_B	Input Bias Current	$T_A = 25^\circ\text{C}$ (Note 3)	●	± 50	± 150 ± 950		± 50	± 200 ± 450	pA pA
I_{OS}	Input Offset Current	$T_A = 25^\circ\text{C}$ (Note 3)	●	± 100	± 300 ± 500		± 100	± 400 ± 500	pA pA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -4V \text{ to } 3V$	●	110	130		110	130	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V \text{ to } \pm 8V$	●	115	130		115	130	dB
A_{VOL}	Large-Signal Voltage Gain	$R_L = 10k, V_{OUT} = \pm 4V$	●	125	170		125	170	dB
	Maximum Output Voltage Swing	$R_L = 1k$ $R_L = 100k$	●	± 4.0	4.3/-4.7 ± 4.92		± 4.0	4.3/-4.7 ± 4.95	V V
SR	Slew Rate	$R_L = 10k, C_L = 50\text{pF}$		10			10		$\text{V}/\mu\text{s}$
GBW	Gain-Bandwidth Product			1.5			1.5		MHz
I_S	Supply Current	No Load, $T_A = 25^\circ\text{C}$	●	3.0	4.0 7.0		3.0	4.0 5.0	mA mA
f_S	Internal Sampling Frequency	$T_A = 25^\circ\text{C}$		4.75			4.75		kHz

$V_{IN} = 5V, T_A = \text{Operating Temperature Range, unless otherwise noted.}$

SYMBOL	PARAMETER	CONDITIONS	LTC1250M			LTC1250C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$T_A = 25^\circ\text{C}$ (Note 1)		± 2	± 5		± 2	± 5	μV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●	± 0.01	± 0.05		± 0.01	± 0.05	$\mu\text{V}/^\circ\text{C}$
e_n	Input Noise Voltage (Note 2)	$T_A = 25^\circ\text{C}, 0.1\text{Hz to } 10\text{Hz}$ $T_A = 25^\circ\text{C}, 0.1\text{Hz to } 1\text{Hz}$		1.0 0.3			1.0 0.3		μV_{P-P} μV_{P-P}
I_B	Input Bias Current	$T_A = 25^\circ\text{C}$ (Note 3)		± 20	± 100		± 20	± 100	pA
I_{OS}	Input Offset Current	$T_A = 25^\circ\text{C}$ (Note 3)		± 40	± 200		± 40	± 200	pA

ELECTRICAL CHARACTERISTICS $V_{IN} = 5V$, $T_A =$ Operating Temperature Range, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LTC1250M			LTC1250C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Maximum Output Voltage Swing	$R_L = 1k$	4.0	4.3		4.0	4.3		V
		$R_L = 100k$		4.95			4.95		V
I_S	Supply Current	$T_A = 25^\circ C$		1.8	2.5		1.8	2.5	mA
f_S	Sampling Frequency	$T_A = 25^\circ C$		3			3		kHz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels during automated testing.

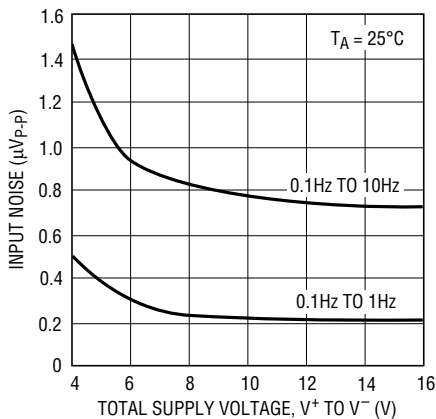
Note 2: 0.1Hz to 10Hz noise is specified DC coupled in a 10s window; 0.1Hz to 1Hz noise is specified in a 100s window with an RC high-pass

filter at 0.1Hz. The LTC1250 is sample tested for noise; for 100% tested parts contact LTC Marketing Dept.

Note 3: At $T \leq 0^\circ C$ these parameters are guaranteed by design and not tested.

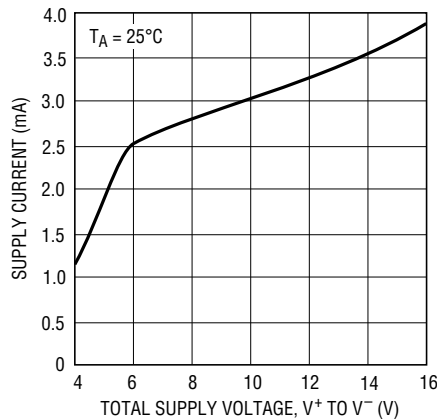
TYPICAL PERFORMANCE CHARACTERISTICS

Input Noise vs Supply Voltage



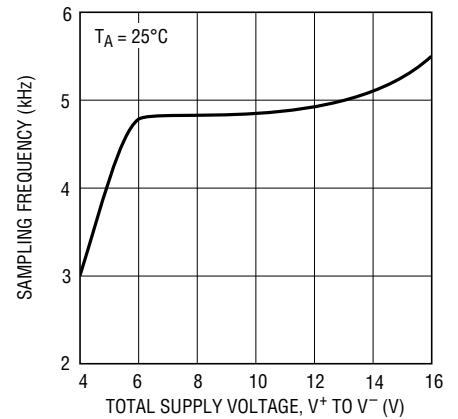
LTC1250 G01

Supply Current vs Supply Voltage



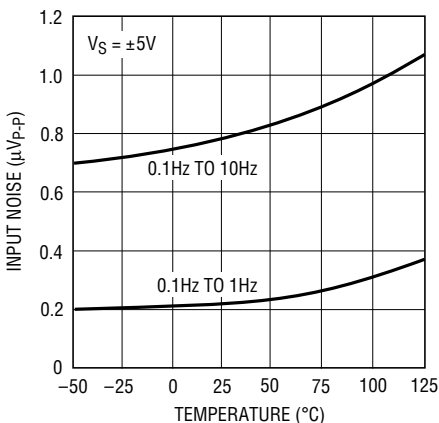
LTC1250 G02

Sampling Frequency vs Supply Voltage



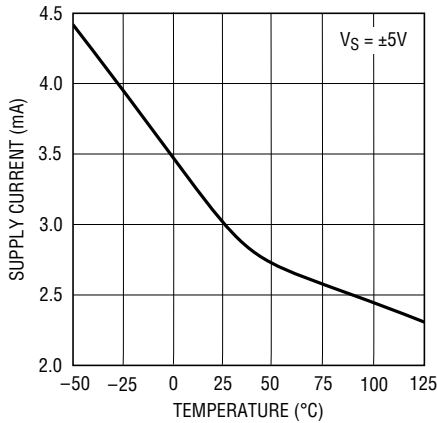
LTC1250 G03

Input Noise vs Temperature



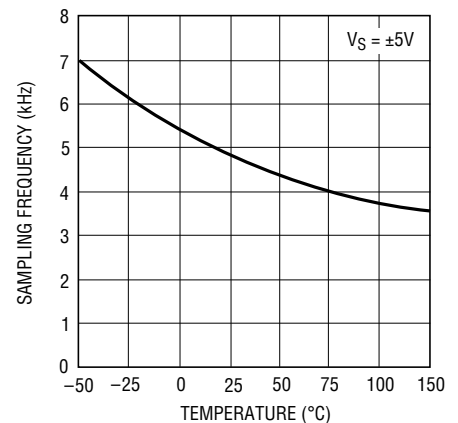
LTC1250 G04

Supply Current vs Temperature



LTC1250 G05

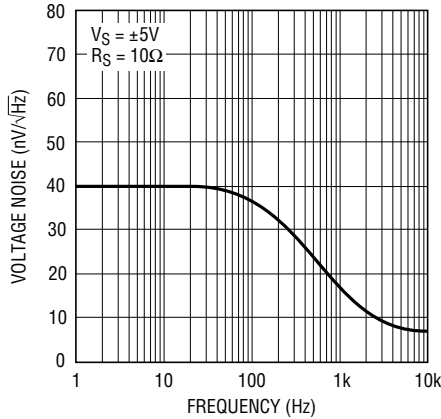
Sampling Frequency vs Temperature



LTC1250 G06

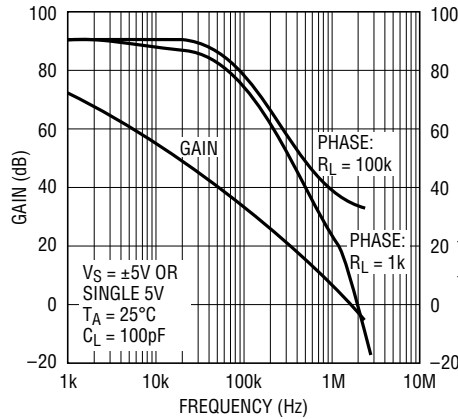
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Noise vs Frequency



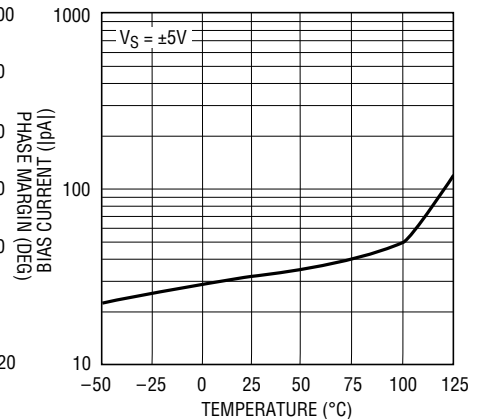
LTC1250 G11

Gain/Phase vs Frequency



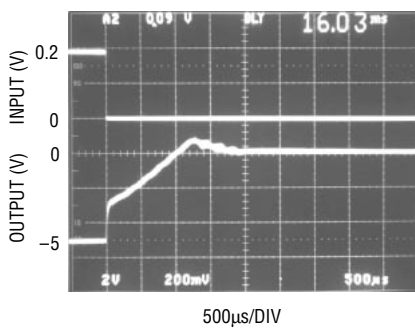
LTC1250 G10

Bias Current (Magnitude) vs Temperature



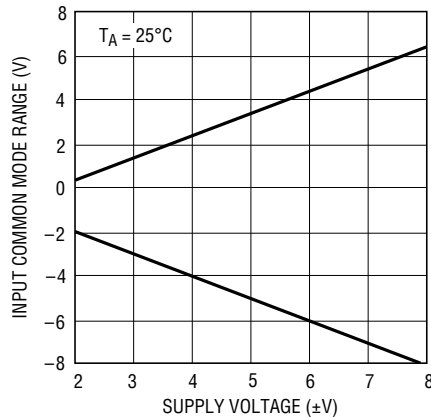
LTC1250 G14

Overload Recovery



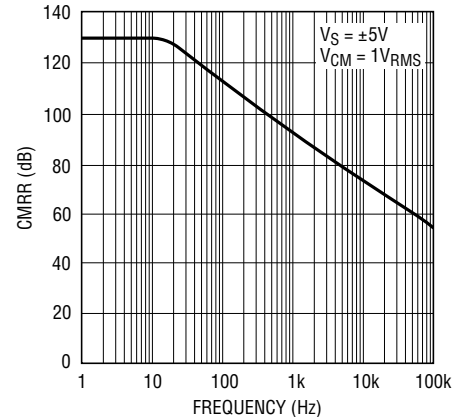
$A_V = 100$, $R_L = 100k$, $C_L = 50pF$, $V_S = \pm 5V$

Common-Mode Input Range vs Supply Voltage



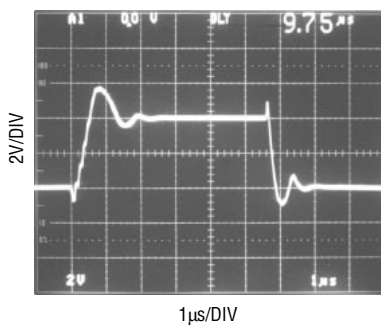
LTC1250 G07

Common-Mode Rejection Ratio vs Frequency



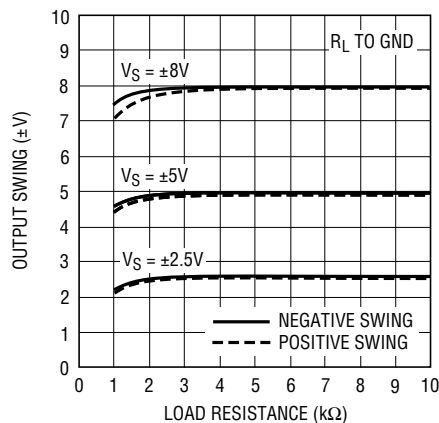
LTC1250 G12

Transient Response



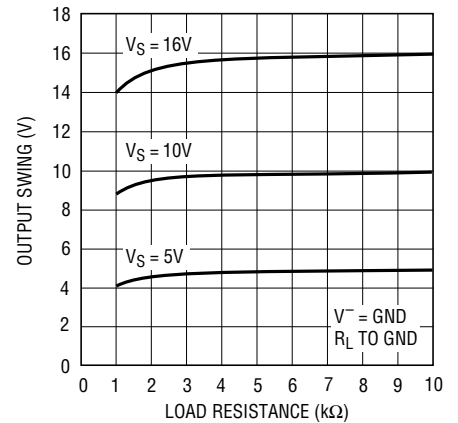
$A_V = 1$, $R_L = 100k$, $C_L = 50pF$, $V_S = \pm 5V$

Output Swing vs Load Resistance, Dual Supplies



LTC1250 G08

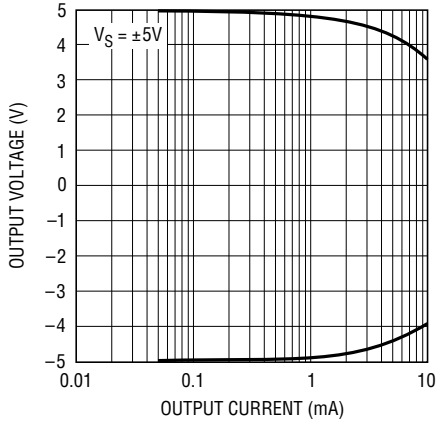
Output Voltage Swing vs Load Resistance, Single Supply



LTC1250 G09

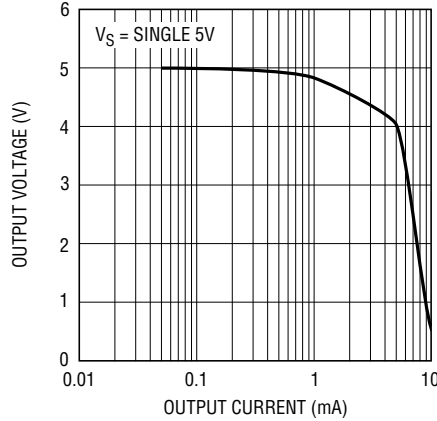
TYPICAL PERFORMANCE CHARACTERISTICS

Output Swing vs Output Current, $\pm 5V$ Supply



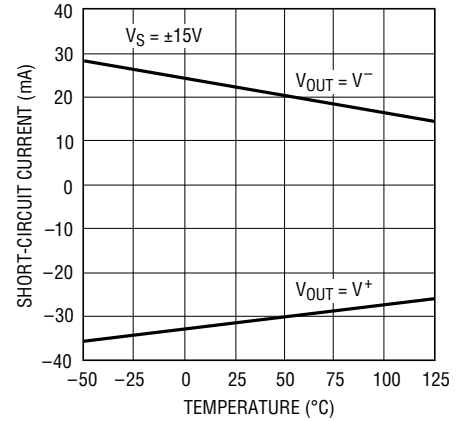
LTC1250 G16

Output Swing vs Output Current, Single 5V Supply



LTC1250 G17

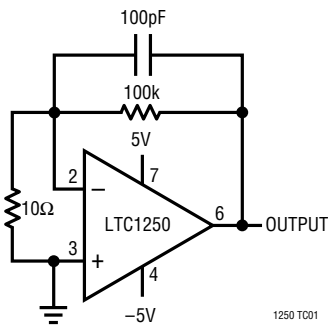
Short-Circuit Current vs Temperature



LTC1250 G18

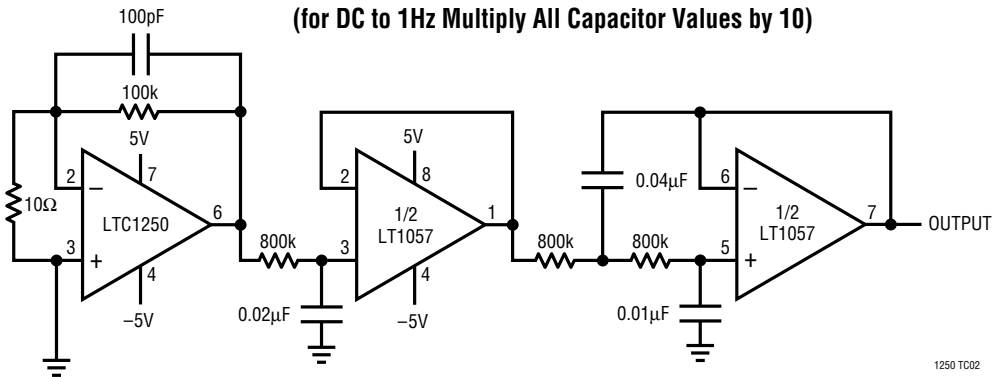
TEST CIRCUITS

Offset Test Circuit



1250 TC01

DC to 10Hz Noise Test Circuit
(for DC to 1Hz Multiply All Capacitor Values by 10)

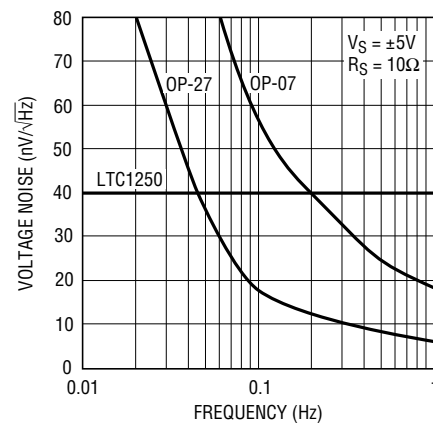


1250 TC02

APPLICATIONS INFORMATION

Input Noise

The LTC1250, like all CMOS amplifiers, exhibits two types of low frequency noise: thermal noise and 1/f noise. The LTC1250 uses several design modifications to minimize these noise sources. Thermal noise is minimized by raising the g_M of the front-end transistors by running them at high bias levels and using large transistor geometries. 1/f noise is combated by optimizing the zero-drift nulling loop to run at twice the 1/f corner frequency, allowing it to reduce the inherently high CMOS 1/f noise to near thermal levels at low frequencies. The resultant noise spectrum is quite low at frequencies below the internal 5kHz clock



LTC1250 F01

Figure 1. Voltage Noise vs Frequency

APPLICATIONS INFORMATION

frequency, approaching the best bipolar op amps at 10Hz and surpassing them below 1Hz (Figure 1). All this is accomplished in an industry-standard pinout; the LTC1250 requires no external capacitors, no nulling or clock signals, and conforms to industry-standard 8-pin DIP and 8-pin SOIC packages.

Input Capacitance and Compensation

The large input transistors create a parasitic 55pF capacitance from each input to V^+ . This input capacitance will react with the external feedback resistors to form a pole which can affect amplifier stability. In low gain, high impedance configurations, the pole can land below the unity-gain frequency of the feedback network and degrade phase margin, causing ringing, oscillation, and other unpleasantness. This is true of any op amp, however, the 55pF capacitance at the LTC1250's inputs can affect stability with a feedback network impedance as low as 1.9k. This effect can be eliminated by adding a capacitor across the feedback resistor, adding a zero which cancels the input pole (Figure 2). The value of this capacitor should be:

$$C_F \geq \frac{55\text{pF}}{A_V}$$

where A_V = closed-loop gain. Note that C_F is not dependent on the value of R_F . Circuits with higher gain ($A_V > 50$) or low loop impedance should not require C_F for stability.

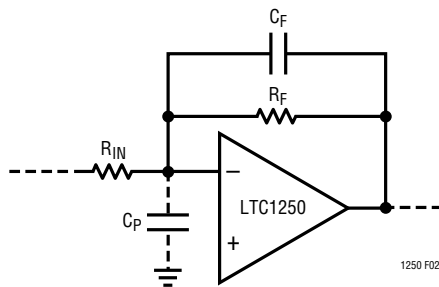


Figure 2. C_F Cancels Phase Shift Due to Parasitic C_P

Larger values of C_F , commonly used in band-limited DC circuits, may actually increase low frequency noise. The nulling circuitry in the LTC1250 closes a loop that includes the external feedback network during part of its cycle. This loop must settle to its final value within 150 μ s or it will not

fully cancel the 1/f noise spectrum and the low frequency noise of the part will rise. If the loop is underdamped (large R_F , no C_F) it will ring for more than 150 μ s and the noise and offset will suffer.

The solution is to add C_F as above but beware! Too large a value of C_F will overdamp the loop, again preventing it from reaching a final value by the 150 μ s deadline. This condition doesn't affect the LTC1250's offset or output stability, but 1/f noise begins to rise. As a rule of thumb, the $R_F C_F$ feedback pole should be $\geq 7\text{kHz}$ (1/150 μ s, the frequency at which the loop settles) for best 1/f performance; values between 100pF and 500pF work well with feedback resistors below 100k. This ensures adequate gain at 7kHz for the LTC1250 to properly null. High value feedback resistors (above 1M) may require experimentation to find the correct value because parasitics, both in the LTC1250 and on the PC board, play an increasing role. Low value resistors (below 5k) may not require a capacitor at all.

Input Bias Current

The inputs of the LTC1250, like all zero-drift op amps, draw only small switching spikes of AC bias current; DC leakage current is negligible except at very high temperatures. The large front-end transistors cause switching spikes 3 to 4 times greater than standard zero-drift op amps: the $\pm 50\text{pA}$ bias current spec is still many times better than most bipolar parts. The spikes don't match from one input pin to the other, and are sometimes (but not always) of opposite polarity. As a result, matching the impedances at the inputs (Figure 3) will not cancel the bias current, and may cause additional errors. Don't do it.

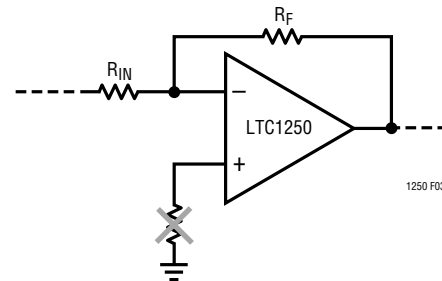


Figure 3. Extra Resistor Will *Not* Cancel Bias Current Errors

APPLICATIONS INFORMATION

Output Drive

The LTC1250 includes an enhanced output stage which provides nearly symmetrical output source/sink currents. This output is capable of swinging a minimum of $\pm 4V$ into a 1k load with $\pm 5V$ supplies, and can sink or source $>20mA$ into low impedance loads. Lightly loaded ($R_L \geq 100k$), the LTC1250 will swing to within millivolts of either rail. In single supply applications, it will typically swing 4.3V into a 1k load with a 5V supply.

Minimizing External Errors

The input noise, offset voltage, and bias current specs for the LTC1250 are all well below the levels of circuit board parasitics. Thermocouples between the copper pins of the LTC1250 and the tin/lead solder used to connect them can overwhelm the offset voltage of the LTC1250, especially if a soldering iron has been around recently. Note also that when the LTC1250's output is heavily loaded, the chip may dissipate substantial power, raising the temperature of the package and aggravating thermocouples at the inputs. Although the LTC1250 will maintain its specified accuracy under these conditions, care must be taken in the layout to prevent or compensate circuit errors. Be especially careful of air currents when measuring low frequency noise; nearby moving objects (like people) can create very large noise peaks with an unshielded circuit board. For more detailed explanations and advice on how to avoid these errors, see the LTC1051/LTC1053 data sheet.

Sampling Behavior

The LTC1250's zero-drift nulling loop samples the input at $\approx 5kHz$, allowing it to process signals below 2kHz with no aliasing. Signals above this frequency may show aliasing behavior, although wideband internal circuitry generally keeps errors to a minimum. The output of the LTC1250 will have small spikes at the clock frequency and its harmonics; these will vary in amplitude with different feedback configurations. Low frequency or band-limited systems should not be affected, but systems with higher bandwidth (oversampling A/Ds, for example) may need to filter out these clock artifacts. Output spikes can be minimized with a large feedback capacitor, but this will adversely affect noise performance (see Input Capacitance and Compensation on

the previous page). Applications which require spike-free output in addition to minimum noise will need a low-pass filter after the LTC1250; a simple RC will usually do the job (Figure 4). The LTC1051/LTC1053 data sheet includes more information about zero-drift amplifier sampling behavior.

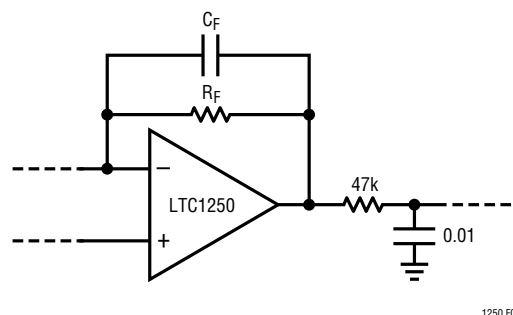


Figure 4. RC Output Pole Limits Bandwidth to 330Hz

Single Supply Operation

The LTC1250 will operate with single supply voltages as low as 4.5V, and the output swings to within millivolts of either supply when lightly loaded. The input stage will common mode to within 250mV of ground with a single 5V supply, and will common mode to ground with single supplies above 11V. Most bridge transducers bias their inputs above ground when powered from single supplies, allowing them to interface directly to the LTC1250 in single supply applications. Single-ended, ground-referenced signals will need to be level shifted slightly to interface to the LTC1250's inputs.

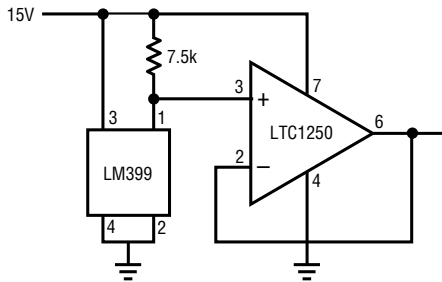
Fault Conditions

The LTC1250 is designed to withstand most external fault conditions without latch-up or damage. However, unusually severe fault conditions can destroy the part. All pins are protected against faults of $\pm 25mA$ or 5V beyond either supply, whichever comes first. If the external circuitry can exceed these limits, series resistors or voltage clamp diodes should be included to prevent damage.

The LTC1250 includes internal protection against ESD damage. All data sheet parameters are maintained to 1kV ESD on any pin; beyond 1kV, the input bias and offset currents will increase, but the remaining specs are unaffected and the part remains functional to 5kV at the input pins and 8kV at the output pin. Extreme ESD conditions should be guarded against by using standard anti-static precautions.

TYPICAL APPLICATIONS

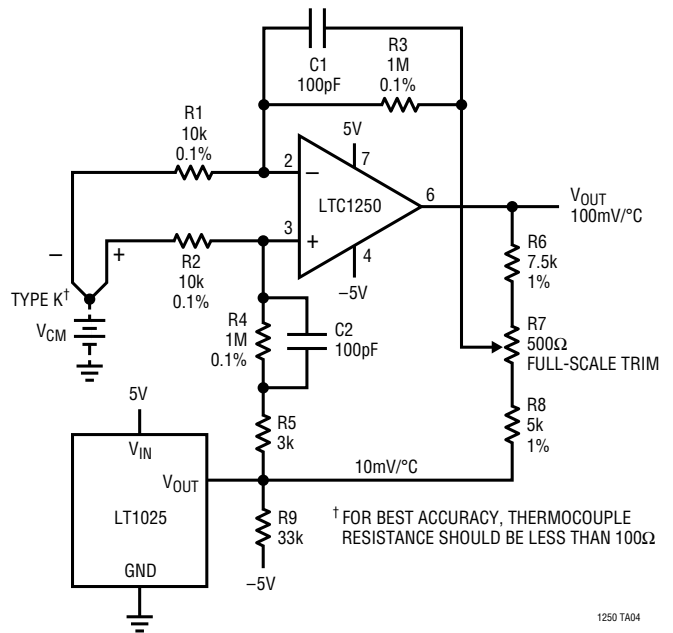
Reference Buffer



±10ppm ERROR AT ±15mA
 1μV_{p-p} OUTPUT NOISE
 2.5μV/°C DRIFT (DUE TO LM399)

1250 TA03

Differential Thermocouple Amplifier

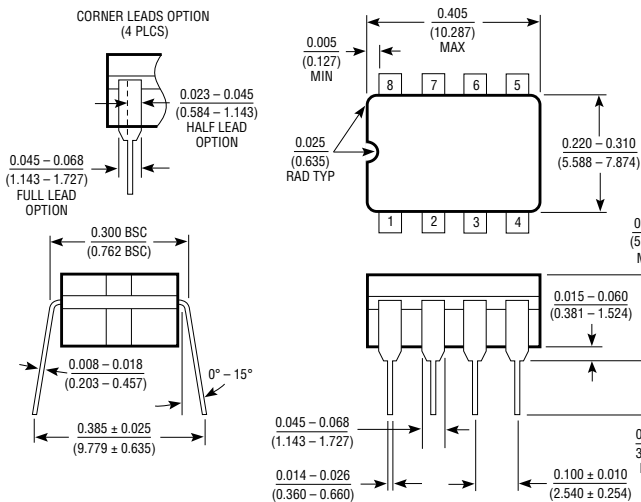


† FOR BEST ACCURACY, THERMOCOUPLE RESISTANCE SHOULD BE LESS THAN 100Ω

1250 TA04

PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

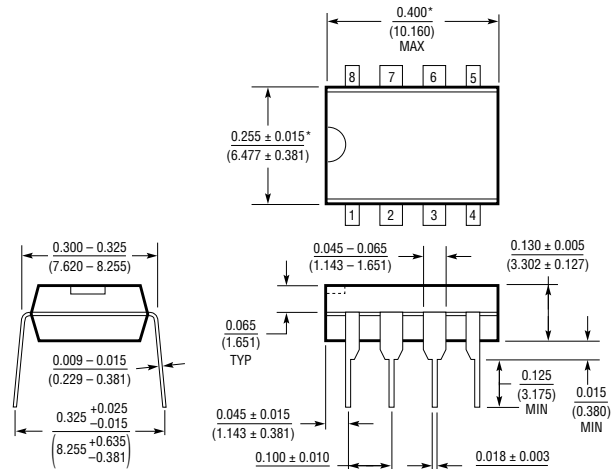
J8 Package 8-Lead Ceramic DIP



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J8 0894

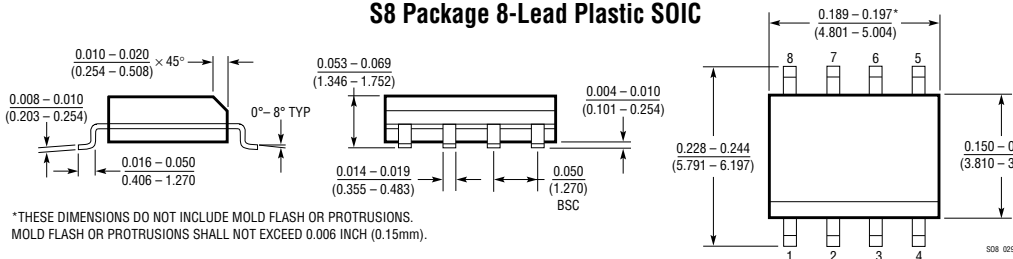
N8 Package 8-Lead Plastic DIP



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm).

N8 0894

S8 Package 8-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

S08 0284