Low Power Video Difference Amplifier

FEATURES

- Differential or Single-Ended Gain Block (Adjustable)
- –3dB Bandwidth, $A_V = \pm 2$ 50MHz
- Slew Rate 165V/µs
- Low Supply Current 13mA
- Output Current ±20mA
- CMRR at 10MHz 40dB
- LT1193 Pin Compatible
- Low Cost
- Single 5V Operation
- Drives Cables Directly
- Output Shutdown

APPLICATIONS

- Line Receivers
- Video Signal Processing
- Cable Drivers
- Tape and Disc Drive Systems

DESCRIPTION

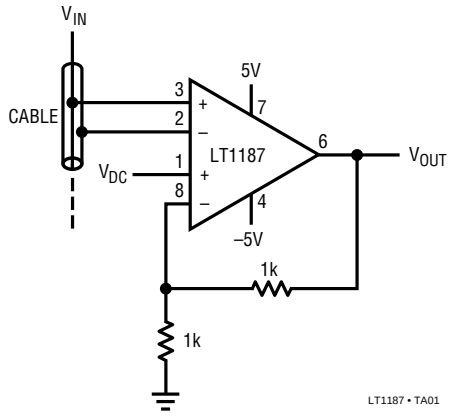
The LT1187 is a difference amplifier optimized for operation on ±5V, or a single 5V supply, and gain ≥2. This versatile amplifier features uncommitted high input impedance (+) and (–) inputs, and can be used in differential or single-ended configurations. Additionally, a second set of inputs give gain adjustment and DC control to the difference amplifier.

The LT1187's high slew rate, 165V/µs, wide bandwidth, 50MHz, and ±20mA output current require only 13mA of supply current. The shutdown feature reduces the power dissipation to a mere 15mW, and allows multiple amplifiers to drive the same cable.

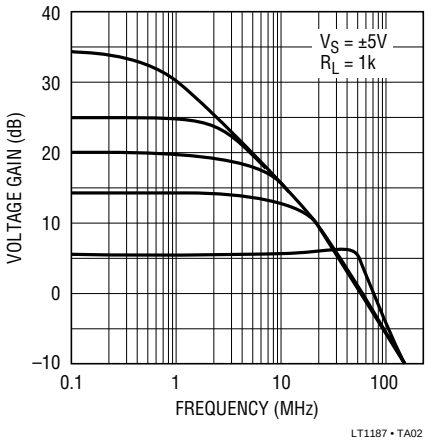
The LT1187 is a low power version of the popular LT1193, and is available in 8-pin miniDIPs and SO packages. For applications with gains of 10 or more, see the LT1189 data sheet.

TYPICAL APPLICATION

Cable Sense Amplifier for Loop Through Connections with DC Adjust



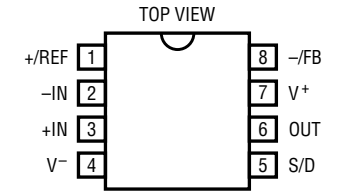
Closed-Loop Gain vs Frequency



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage ..... ±6V
Input Voltage ..... $\pm V_S$
Output Short Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range
LT1187M ..... –55°C to 150°C
LT1187C ..... 0°C to 70°C
Junction Temperature (Note 2)
Plastic Package (CN8,CS8) ..... 150°C
Ceramic Package (CJ8,MJ8) ..... 175°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD HERMETIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

LT1187 • POI01

T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J8)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1187MJ8 LT1187CJ8 LT1187CN8 LT1187CS8
S8 PART MARKING
1187

Consult factory for Industrial grade parts.

±5V ELECTRICAL CHARACTERISTICS

T_A = 25°C, (Note 3)

V_S = ±5V, V_{REF} = 0V, R_{FB1} = 900Ω from pins 6 to 8, R_{FB2} = 100Ω from pin 8 to ground, R_L = R_{FB1} + R_{FB2} = 1k, C_L ≤ 10pF, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1187M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		2.0	10	mV
		SOIC Package		2.0	11	mV
I_{OS}	Input Offset Current	Either Input		0.2	1.0	µA
I_B	Input Bias Current	Either Input		±0.5	±2.0	µA
e_n	Input Noise Voltage	f_O = 10kHz		65		nV/√Hz
i_n	Input Noise Current	f_O = 10kHz		1.5		pA/√Hz
R_{IN}	Input Resistance	Differential		100		kΩ
C_{IN}	Input Capacitance	Either Input		2.0		pF
$V_{IN\ LIM}$	Input Voltage Limit	(Note 5)		±380		mV
	Input Voltage Range		–2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = –2.5V to 3.5V	70	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±8V	70	85		dB
V_{OUT}	Output Voltage Swing	V_S = ±5V, R_L = 1k, A_V = 50	±3.8	±4.0		V
		V_S = ±8V, R_L = 1k, A_V = 50	±6.7	±7.0		
		V_S = ±8V, R_L = 300Ω, A_V = 50, (Note 3)	±6.4	±6.8		
G_E	Gain Error	V_O = ±1V, A_V = 10, R_L = 1k		0.2	1.0	%
SR	Slew Rate	(Note 6, 10)	100	165		V/µs
FPBW	Full Power Bandwidth	V_O = $1V_{P-P}$, (Note 7)		53		MHz
BW	Small Signal Bandwidth	A_V = 10		5.7		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 50, V_O = ±1.5V, 20% to 80% (Note 10)	150	230	325	ns
t_{PD}	Propagation Delay	R_L= 1k, V_O = ±125mV, 50% to 50%		26		ns
	Overshoot	V_O = ±50mV		0		%
t_s	Settling Time	3V Step, 0.1%, (Note 8)		100		ns
Diff A_V	Differential Gain	R_L = 1k, A_V = 4, (Note 9)		0.6		%
Diff Ph	Differential Phase	R_L = 1k, A_V = 4, (Note 9)		0.8		DEG_{P-P}
I_S	Supply Current			13	16	mA
	Shutdown Supply Current	Pin 5 at V^-		0.8	1.5	mA

±5V ELECTRICAL CHARACTERISTICS

T_A = 25°C, (Note 3)

V_S = ±5V, V_{REF} = 0V, R_{FB1} = 900Ω from pins 6 to 8, R_{FB2} = 100Ω from pin 8 to ground, R_L = R_{FB1} + R_{FB2} = 1k, C_L ≤ 10pF, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1187M/C MIN	TYP	MAX	UNITS
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA
t_{ON}	Turn On Time	Pin 5 from V^- to Ground, R_L = 1k		500		ns
t_{OFF}	Turn Off Time	Pin 5 from Ground to V^-, R_L = 1k		600		ns

5V ELECTRICAL CHARACTERISTICS

T_A = 25°C, (Note 3)

V_S^+ = 5V, V_S^- = 0V, V_{REF} = 2.5V, R_{FB1} = 900Ω from pins 6 to 8, R_{FB2} = 100Ω from pin 8 to V_{REF}, R_L = R_{FB1} + R_{FB2} = 1k, C_L ≤ 10pF, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS		LT1187M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4) SOIC Package			2.0 2.0	10 12	mV mV
I_{OS}	Input Offset Current	Either Input			0.2	1.0	µA
I_B	Input Bias Current	Either Input			±0.5	±2.0	µA
	Input Voltage Range			2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 2.0V to 3.5V		70	100		dB
V_{OUT}	Output Voltage Swing	R_L = 300Ω to Ground (Note 3)	V_{OUT} High	3.6	4.0		V
			V_{OUT} Low		0.15	0.4	
SR	Slew Rate	V_O = 1.5V to 3.5V			130		V/µs
BW	Small-Signal Bandwidth	A_V = 10			5.3		MHz
I_S	Supply Current				12	15	mA
	Shutdown Supply Current	Pin 5 at V^-			0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

±5V ELECTRICAL CHARACTERISTICS

−55°C ≤ T_A ≤ 125°C, (Note 3)

V_S = ±5V, V_{REF} = 0V, R_{FB1} = 900Ω from pins 6 to 8, R_{FB2} = 100Ω from pin 8 to ground, R_L = R_{FB1} + R_{FB2} = 1k, C_L ≤ 10pF, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1187M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		2.0	15	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			8.0		µV/°C
I_{OS}	Input Offset Current	Either Input		0.2	1.5	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
	Input Voltage Range		−2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = −2.5V to 3.5V	70	100		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±8V	60	85		dB
V_{OUT}	Output Voltage Swing	V_S = ±5V, R_L = 1k, A_V = 50	±3.7	±4.0		V
		V_S = ±8V, R_L = 1k, A_V = 50	±6.6	±7.0		
		V_S = ±8V, R_L = 300Ω, A_V = 50, (Note 3)	±6.4	±6.8		
G_E	Gain Error	V_O = ±1V, A_V = 10, R_L = 1k		0.2	1.2	%
I_S	Supply Current			13	17	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)		0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

±5V ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, (Note 3)

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \le 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS	LT1187C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4)		2.0	12	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			9.0		µV/°C
I_{OS}	Input Offset Current	Either Input		0.2	1.5	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
	Input Voltage Range		–2.5		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = -2.5V$ to 3.5V	70	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to ±8V	65	85		dB
V_{OUT}	Output Voltage Swing	$V_S = \pm5V$, $R_L = 1k$, $A_V = 50$	±3.7	±4.0		V
		$V_S = \pm8V$, $R_L = 1k$, $A_V = 50$	±6.6	±7.0		
		$V_S = \pm8V$, $R_L = 300\Omega$, $A_V = 50$, (Note 3)	±6.4	±6.8		
G_E	Gain Error	$V_O = \pm1V$, $A_V = 10$, $R_L = 1k$		0.2	1.0	%
I_S	Supply Current			13	17	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)		0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		5	25	µA

5V ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, (Note 3)

$V_S^+ = 5V$, $V_S^- = 0V$, $V_{REF} = 2.5V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to V_{REF}, $R_L = R_{FB1} + R_{FB2} = 1k$, $C_L \le 10pF$, pin 5 open.

SYMBOL	PARAMETER	CONDITIONS		LT1187C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Either Input, (Note 4) SOIC Package			2.0 2.0	12.0 13.0	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift				9.0		µV/°C
I_{OS}	Input Offset Current	Either Input			0.2	1.5	µA
I_B	Input Bias Current	Either Input			±0.5	±3.5	µA
	Input Voltage Range			2.0		3.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 2.0V$ to 3.5V		70	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 300\Omega$ to Ground	V_{OUT} High	3.5	4.0		V
		(Note 3)	V_{OUT} Low		0.15	0.4	
I_S	Supply Current				12	16	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 11)			0.8	1.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			5	25	µA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted continuously.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1187MJ8,LT1187CJ8: $T_J = T_A + (P_D \times 100°C/W)$
LT1187CN8: $T_J = T_A + (P_D \times 100°C/W)$
LT1187CS8: $T_J = T_A + (P_D \times 150°C/W)$

Note 3: When $R_L = 1k$ is specified, the load resistor is $R_{FB1} + R_{FB2}$, but when $R_L = 300\Omega$ is specified, then an additional 430Ω is added to the output such that ($R_{FB1} + R_{FB2}$) in parallel with 430Ω is $R_L = 300\Omega$.

Note 4: V_{OS} measured at the output (pin 6) is the contribution from both input pair, and is input referred.

Note 5: $V_{IN\ LIM}$ is the maximum voltage between $-V_{IN}$ and $+V_{IN}$ (pin 2 and pin 3) for which the output can respond.

Note 6: Slew rate is measured between ±0.5V on the output, with a V_{IN} step of ±0.75V, $A_V = 3$ and $R_L = 1k$.

Note 7: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi Vp$.

Note 8: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985.

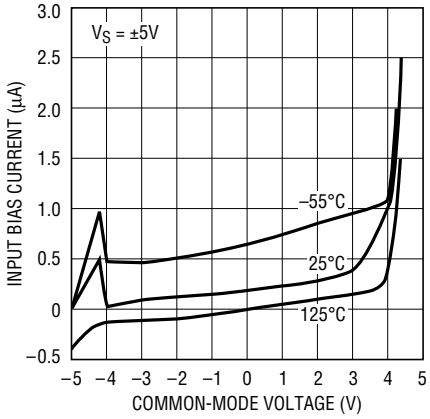
Note 9: NTSC (3.58MHz).

Note 10: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J8 and N8 suffix) and are sample tested on every lot of the SO packaged parts (S8 suffix).

Note 11: See Application section for shutdown at elevated temperatures. Do not operate shutdown above $T_J > 125°C$.

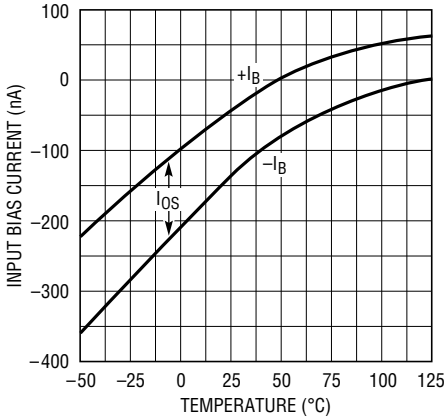
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Common-Mode Voltage



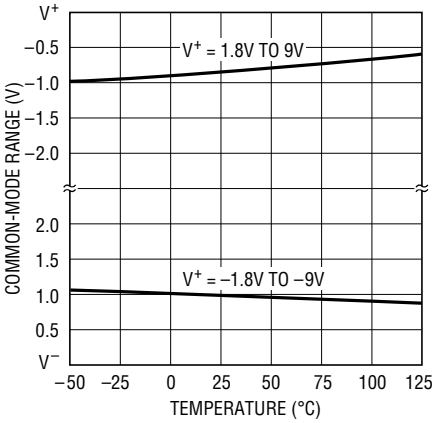
LT1187 • TPC01

Input Bias Current vs Temperature



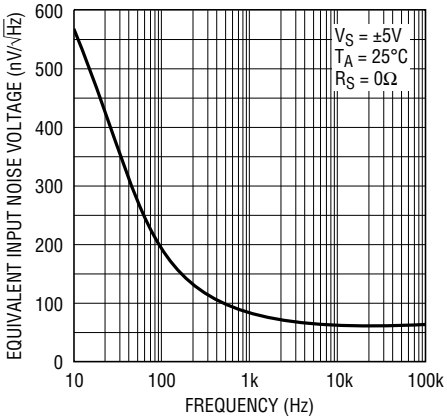
LT1187 • TPC02

Common-Mode Voltage vs Temperature



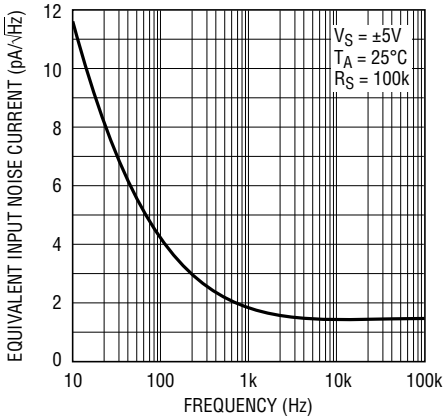
LT1187 • TPC03

Equivalent Input Noise Voltage vs Frequency



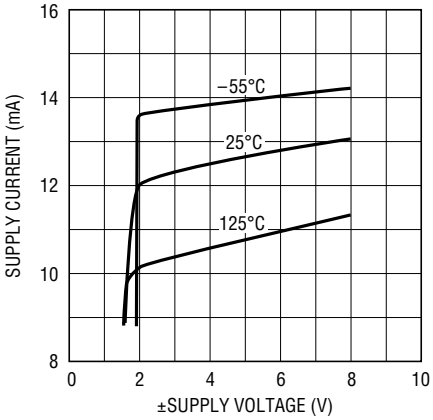
LT1187 • TPC04

Equivalent Input Noise Current vs Frequency



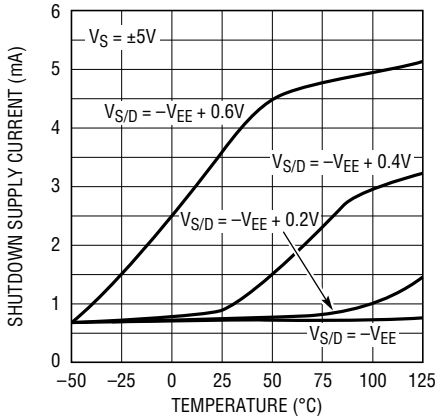
LT1187 • TPC05

Supply Current vs Supply Voltage



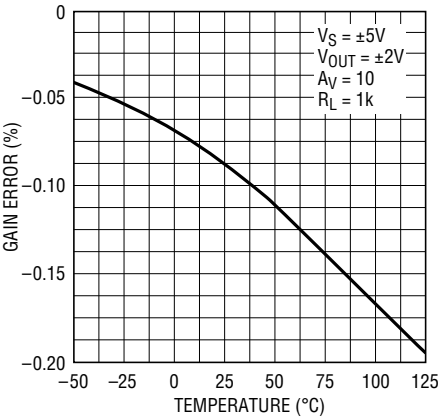
LT1187 • TPC06

Shutdown Supply Current vs Temperature



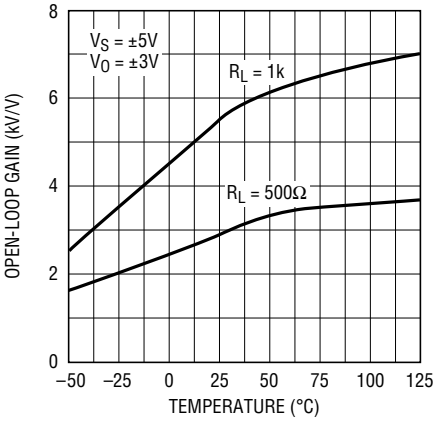
LT1187 • TPC07

Gain Error vs Temperature



LT1187 • TPC08

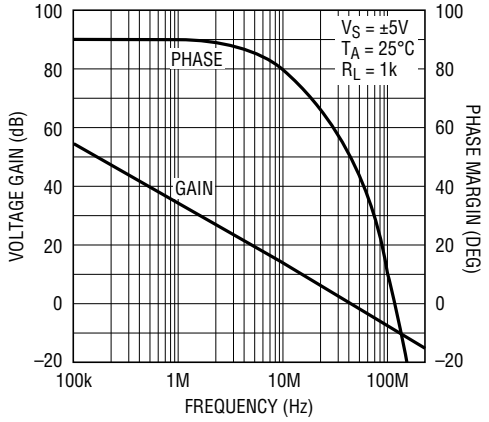
Open-Loop Gain vs Temperature



LT1187 • TPC09

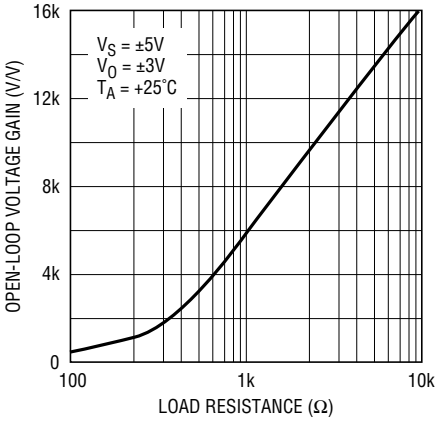
TYPICAL PERFORMANCE CHARACTERISTICS

Gain, Phase vs Frequency

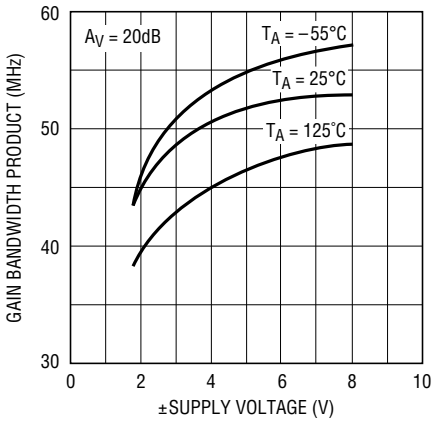


LT1187 • TPC11

Open-Loop Voltage Gain vs Load Resistance

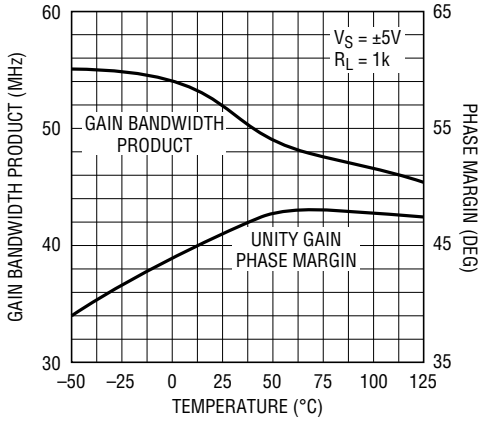


Gain Bandwidth Product vs Supply Voltage



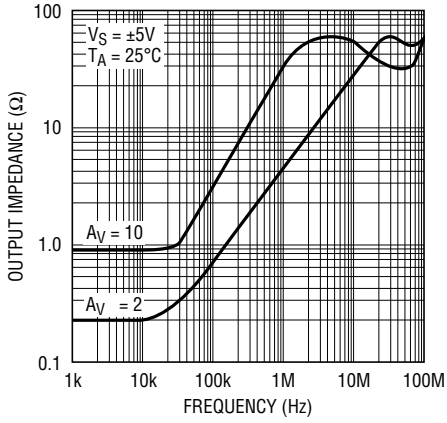
LT1187 • TPC12

Gain Bandwidth Product and Unity Gain Phase Margin vs Temperature



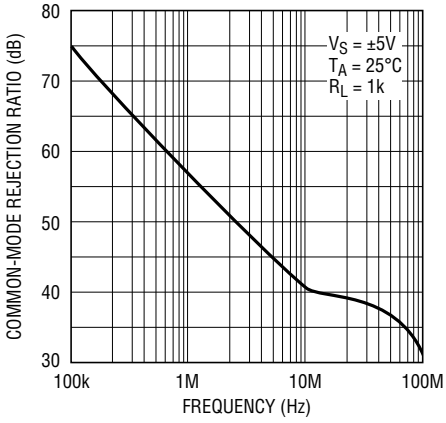
LT1187 • TPC13

Output Impedance vs Frequency



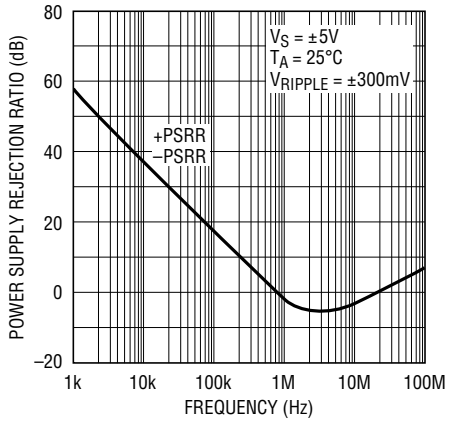
LT1187 • TPC14

Common-Mode Rejection Ratio vs Frequency



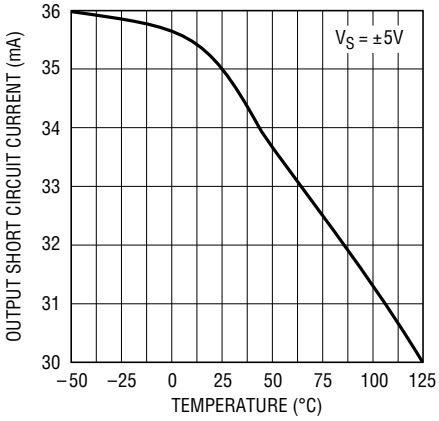
LT1187 • TPC15

Power Supply Rejection Ratio vs Frequency



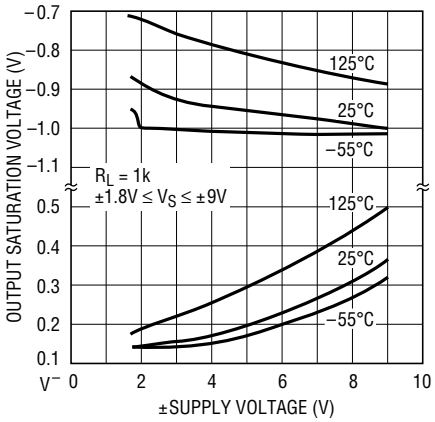
LT1187 • TPC16

Output Short Circuit Current vs Temperature



LT1187 • TPC17

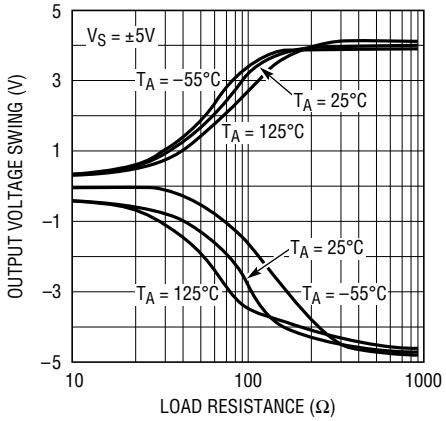
V+ ± Output Swing vs Supply Voltage



LT1187 • TPC18

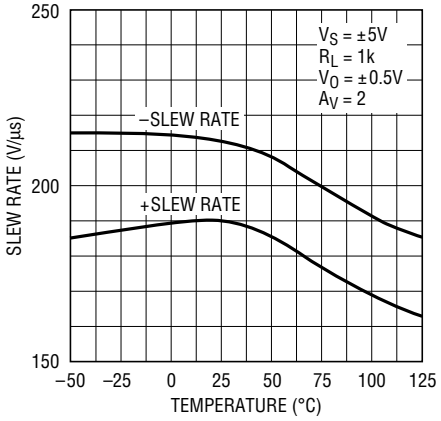
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Load Resistance



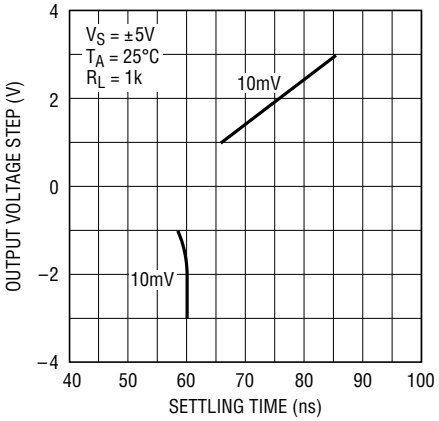
LT1187 • TPC19

Slew Rate vs Temperature



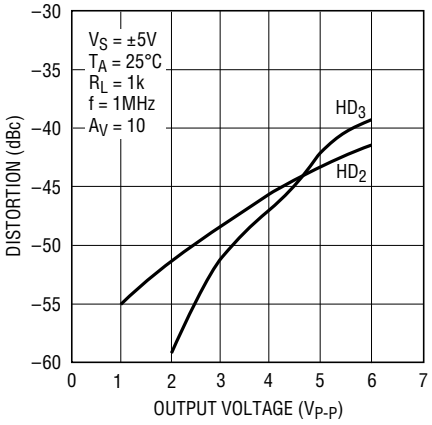
LT1187 • TPC20

Output Voltage Step vs Settling Time, A_V = 2



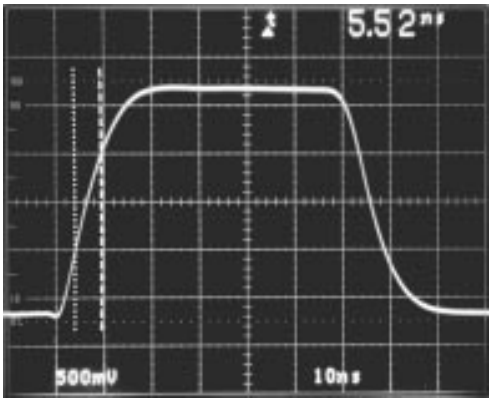
LT1187 • TPC21

Harmonic Distortion vs Output Voltage



LT1187 • TPC22

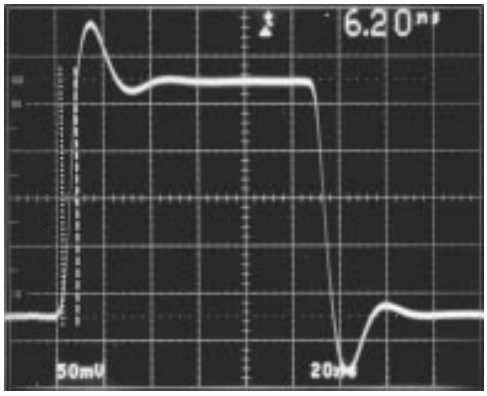
Large-Signal Transient Response



INPUT IN LIMITING, A_V = 3, SR = 180V/µs

LT1187 • TPC23

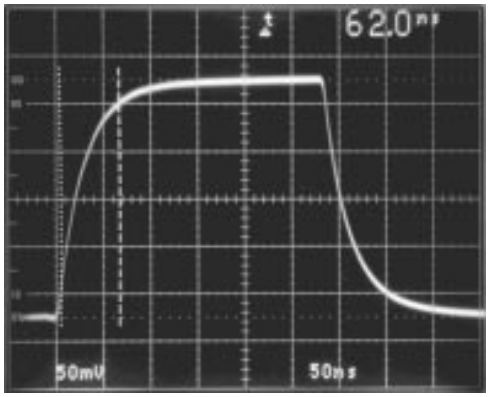
Small-Signal Transient Response



A_V = 2, R_{FB} = 1k, OVERSHOOT = 25%

LT1187 • TPC24

Small-Signal Transient Response



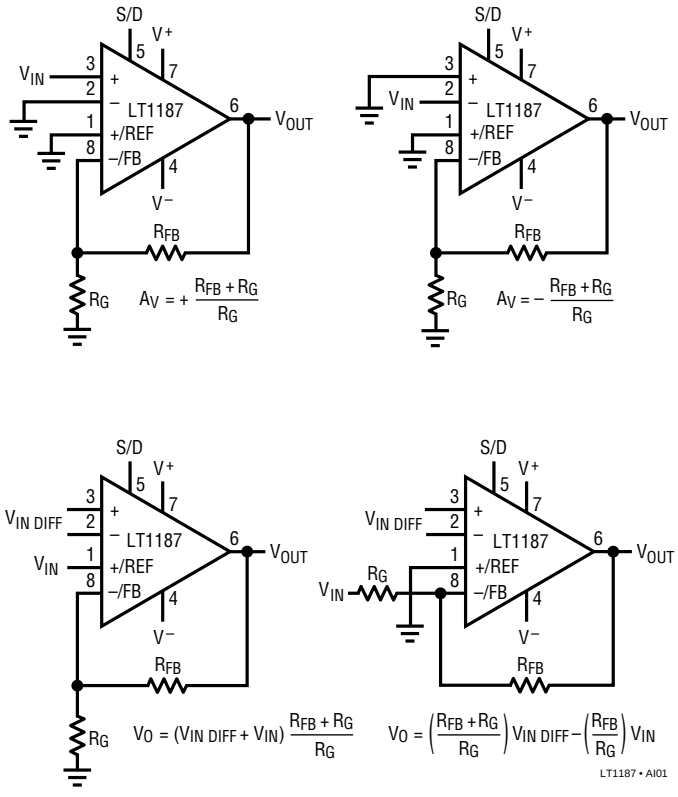
A_V = 2, R_{FB} = 1k, OVERSHOOT = 25%

LT1187 • TPC25

APPLICATIONS INFORMATION

The primary use of the LT1187 is in converting high speed differential signals to a single-ended output. The LT1187 video difference amplifier has two uncommitted high input impedance (+) and (–) inputs. The amplifier has another set of inputs which can be used for reference and feedback. Additionally, this set of inputs give gain adjust and DC control to the difference amplifier. The voltage gain of the LT1187 is set like a conventional operational amplifier. Feedback is applied to pin 8, and it is optimized for gains of 2 or greater. The amplifier can be operated single-ended by connecting either the (+) or (–) inputs to the +/REF (pin 1). The voltage gain is set by the resistors: $(R_{FB} + R_G)/R_G$.

Like the single-ended case, the differential voltage gain is set by the external resistors: $(R_{FB} + R_G)/R_G$. The maximum input differential signal for which the output will respond is approximately ±0.38V.



Power Supply Bypassing

The LT1187 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. In applications requiring good settling time, it is important to use multiple bypass capacitors. A 0.1µF ceramic disc in parallel with a 4.7µF tantalum is recommended.

Calculating the Output Offset Voltage

Both input stages contribute to the output offset voltage at pin 6. The feedback correction forces balance in the input stages by introducing an Input V_{OS} at pin 8. The complete expression for the output offset voltage is:

$$V_{OUT} = (V_{OS} + I_{OS}(R_S) + I_B(R_{REF})) \times (R_{FB}+R_G)/R_G + I_B(R_{FB})$$

R_S represents the input source resistance, typically 75Ω, and R_{REF} represents the finite source impedance from the DC reference voltage, for V_{REF} grounded, R_{REF} = 0Ω. The I_{OS} is normally a small contributor and the expression simplifies to:

$$V_{OUT} = V_{OS}(R_{FB}+R_G)/R_G + I_B(R_{FB})$$

If R_{FB} is limited to 1k the last term of the equation contributes only 2mV, since I_B is less than 2µA.

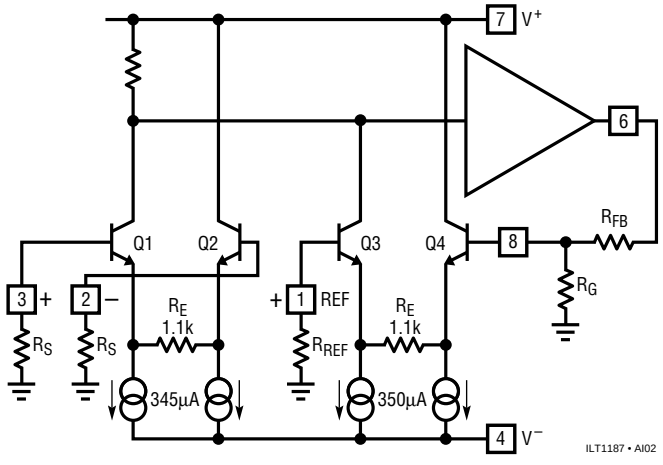


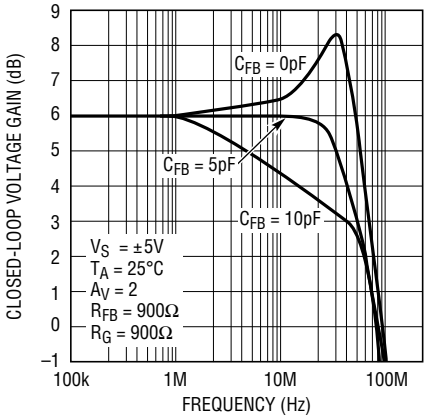
Figure 1. Simplified Input Stage Schematic

APPLICATIONS INFORMATION

Operating with Low Closed-Loop Gains

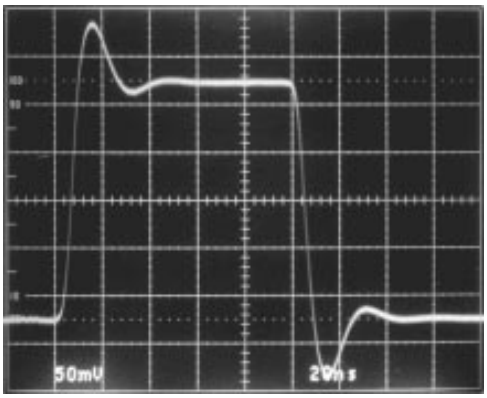
The LT1187 has been optimized for closed-loop gains of 2 or greater. For a closed-loop gain of 2 the response peaks about 2dB. Peaking can be eliminated by placing a capacitor across the feedback resistor, (feedback zero). This peaking shows up as time domain overshoot of about 25%.

Closed-Loop Voltage Gain vs Frequency



LT1187 • AI03

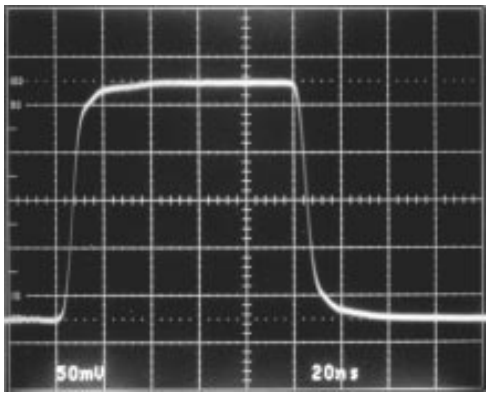
Small-Signal Transient Response



A_V = 2, OVERSHOOT = 25%, $R_{FB} = R_G$ = 1k

LT1187 • AI04

Small-Signal Transient Response



A_V = 2, WITH 8pF FEEDBACK CAPACITOR

LT1187 • AI05

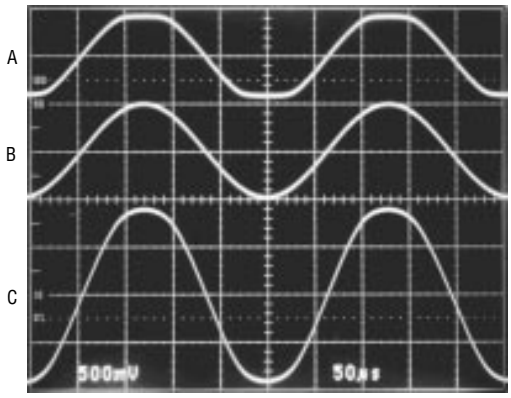
Extending the Input Range

Figure 1 shows a simplified schematic of the LT1187. In normal operation the REF pin 1 is grounded or taken to a DC offset control voltage and differential signals are applied between pins 2 and 3. The input responds linearly until all of the 345µA current flows through the 1.1k resistor and Q1 (or Q2) turns off. Therefore the maximum input swing is 380mV$_P$ or 760mV$_{P-P}$. The second differential pair, Q3 and Q4, is running at slightly larger current so that when the first input stage limits, the second stage remains biased to maintain the feedback.

Occasionally it is necessary to handle signals larger than 760mV$_{P-P}$ at the input. The LT1187 input stage can be tricked to handle up to 1.5V$_{P-P}$. To do this, it is necessary to ground pin 3 and apply the differential input signal between pin 1 and 2. The input signal is now applied across two 1.1k resistors in series. Since the input signal is applied to both input pairs, the first pair will run out of bias current before the second pair, causing the amplifier to go open-loop. The results of this technique are shown in the following scope photo.

APPLICATIONS INFORMATION

LT1187 in Unity Gain



(A) STANDARD INPUTS, PINS 2 TO 3, V_{IN} = 1.0V_{P-P}
(B) EXTENDED INPUTS, PINS 2 TO 2, V_{IN} = 1.0V_{P-P}
(C) EXTENDED INPUTS, PINS 1 TO 2, V_{IN} = 2.0V_{P-P}

LT1187 • AI06

Using the Shutdown Feature

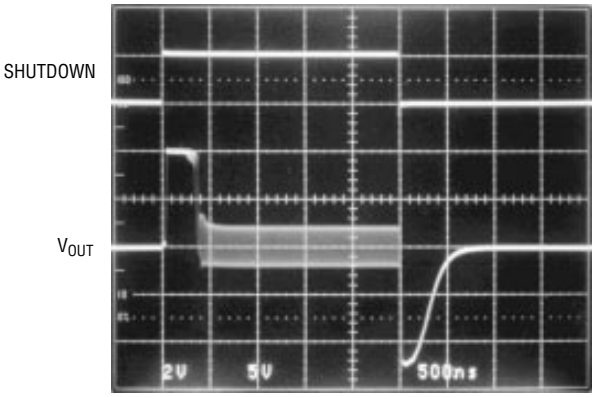
The LT1187 has a unique feature that allows the amplifier to be shutdown for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of 20k in parallel with the feedback resistors. For MUX applications, the amplifiers may be configured inverting, noninverting, or differential. When the output is loaded with as little 1k from the amplifier's feedback resistors, the amplifier shuts off in 600ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

The ability to maintain shutoff is shown on the curve Shutdown Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperature it is important to hold the shutdown pin close to the negative supply to keep the supply current from increasing.

Send Color Video Over Twisted-Pair

With an LT1187 it is possible to send and receive color composite video signals more than 1000 feet on a low cost twisted-pair. A bidirectional "video bus" consists of the LT1195 op amp and the LT1187 video difference amplifier. A pair of LT1195s at TRANSMIT 1, is used to generate differential signals to drive the line which is back-terminated in its characteristic impedance. The LT1187, twisted-pair receiver, converts signals from differential to single-ended. Topology of the LT1187 provides for cable compensation at the amplifier's feedback node as shown. In this case, 1000 feet of twisted-pair is compensated with 1000pF and 50Ω to boost the 3dB bandwidth of the system from 750kHz to 4MHz. This bandwidth is adequate to pass a 3.58MHz chroma subcarrier, and the 4.5MHz sound subcarrier. Attenuation in the cable can be compensated by lowering the gain set resistor R_G. At TRANSMIT 2, another pair of LT1195s serve the dual function to provide cable termination via low output impedance, and generate differential signals for TRANSMIT 2. Cable termination is made up of a 15Ω and 33Ω attenuator to reduce the differential input signal to the LT1187. Maximum input signal for the LT1187 is 760mV_{P-P}.

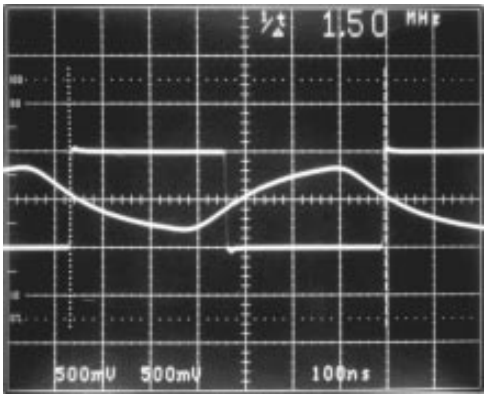
1MHz Sine Wave Gated Off with Shutdown Pin



A_V = 2, R_{FB} = R_G = 1k

LT1187 • AI07

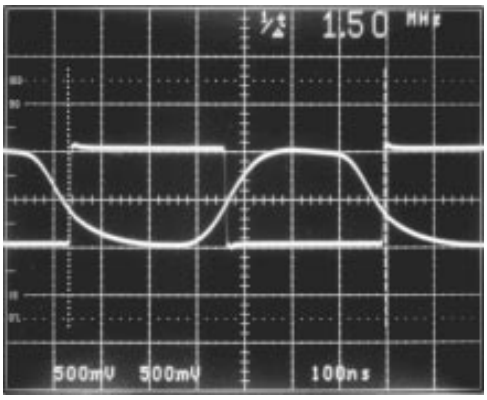
1.5MHz Square Wave Input and Unequalized Response Through 1000 Feet of Twisted-Pair



LT1187 • AI08

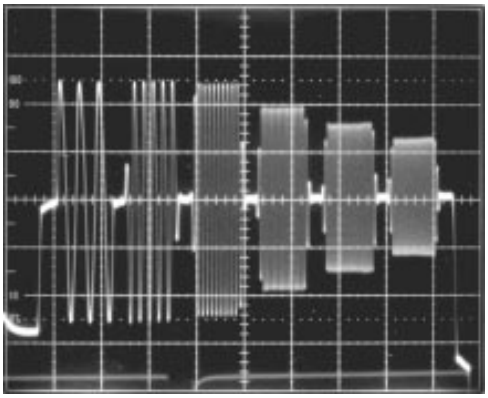
APPLICATIONS INFORMATION

1.5MHz Square Wave Input and Equalized Response Through 1000 Feet of Twisted-Pair



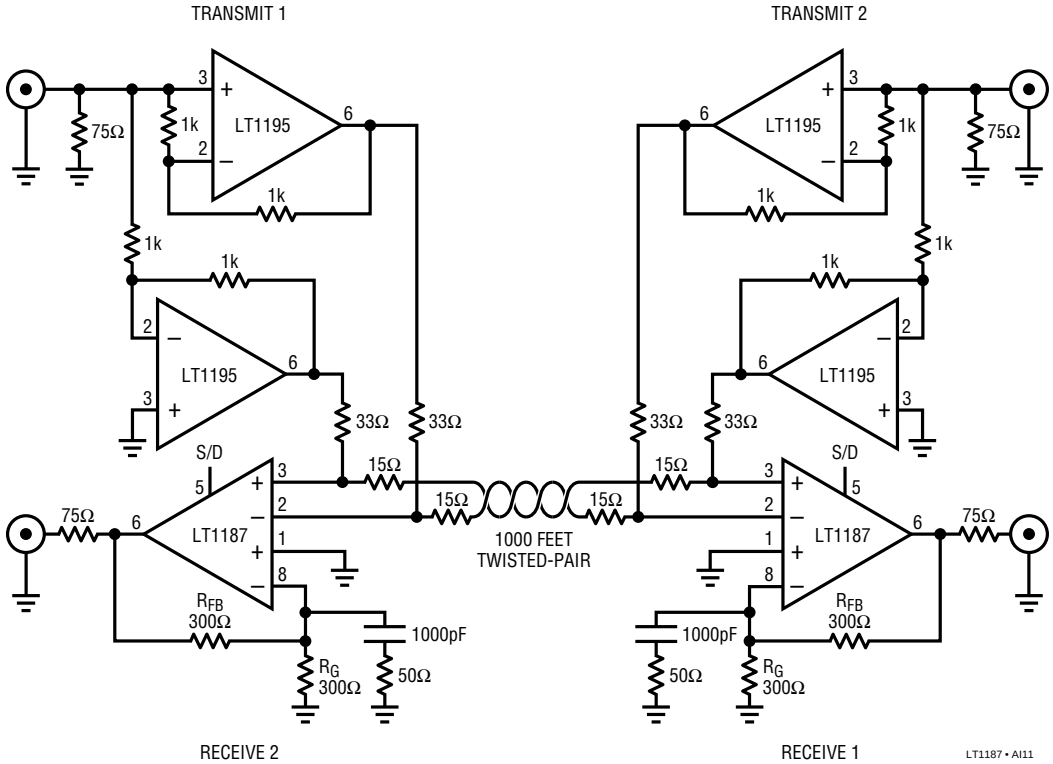
LT1187 • AI09

Multiburst Pattern Passed Through 1000 Feet of Twisted-Pair



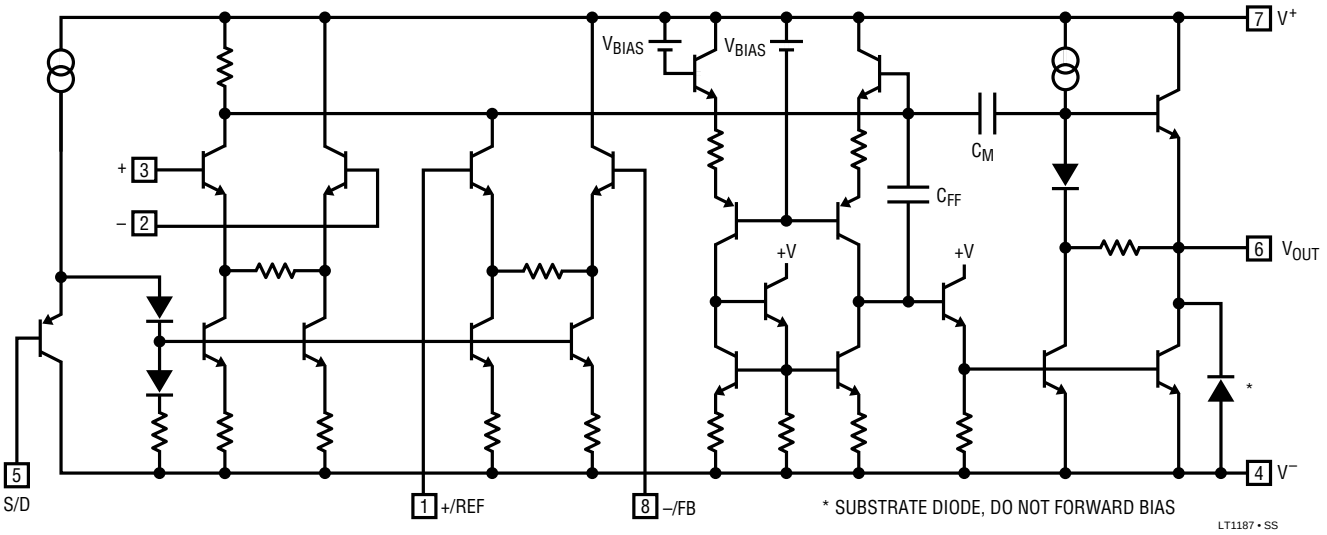
LT1187 • AI10

Bidirectional Video Bus



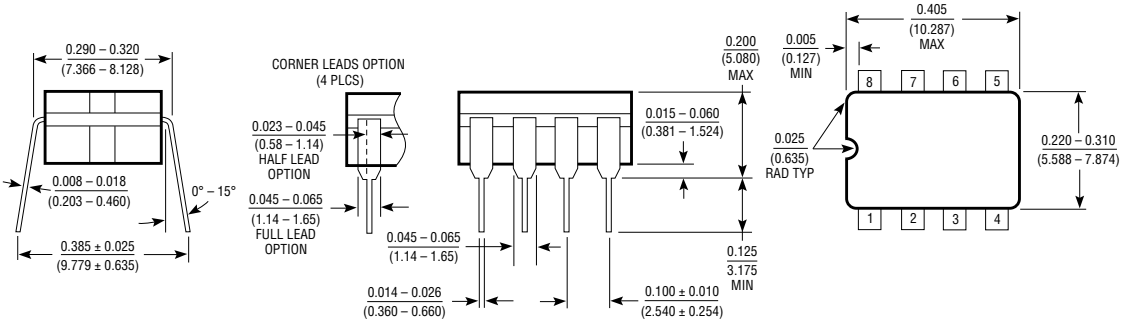
LT1187 • AI11

SIMPLIFIED SCHEMATIC

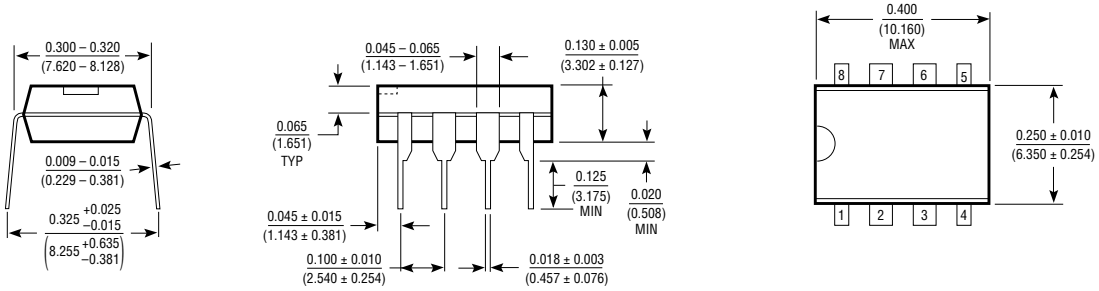


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

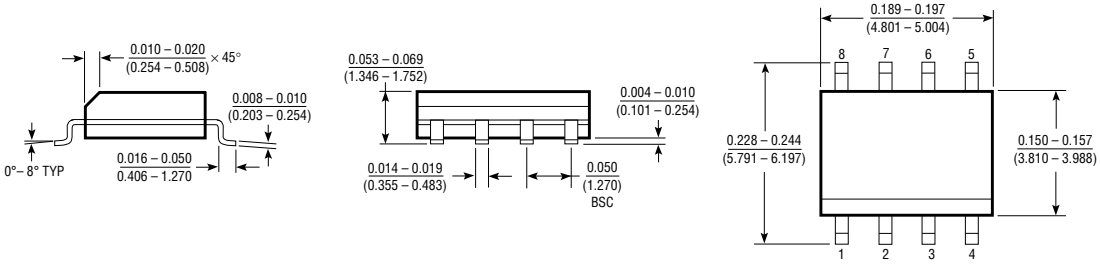
J8 Package
8-Lead Hermetic DIP



N8 Package
8-Lead Plastic DIP



S8 Package
8-Lead Plastic SOIC



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BA/LT/GP 0293 10K REV0