LT1122

Fast Settling, JFET Input Operational Amplifier

FEATURES

- 100% Tested Settling Time to 1mV at Sum Node, 10V Step Tested with Fixed Feedback Capacitor — 340ns Typ, 540ns Max
- Slew Rate — 60V/µs Min
- Gain Bandwidth Product — 14MHz
- Power Bandwidth (20Vp-p) — 1.2 MHz
- Unity Gain Stable; Phase Margin — 60°
- Input Offset Voltage — 600µV Max
- Input Bias Current — 25°C 75pA Max; 70°C 600pA Max
- Input Offset Current — 25°C 40pA Max; 70°C 150pA Max
- Low Distortion

APPLICATIONS

- Fast 12-Bit D/A Output Amplifiers
- High Speed Buffers
- Fast Sample and Hold Amplifiers
- High Speed Integrators
- Voltage to Frequency Converters
- Active Filters
- Log Amplifiers
- Peak Detectors

DESCRIPTION

The LT1122 JFET input operational amplifier combines high speed and precision performance.

A unique poly-gate JFET process minimizes gate series resistance and gate-to-drain capacitance, facilitating wide bandwidth performance, without degrading JFET transistor matching.

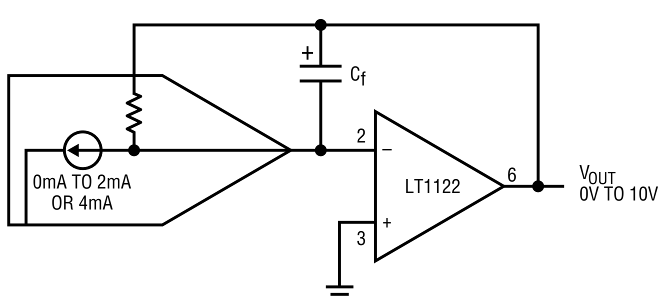
It slews at 80V/µs and settles in 340ns. The LT1122 is internally compensated to be unity gain stable, yet it has a bandwidth of 14MHz at a supply current of only 7mA. Its speed makes the LT1122 an ideal choice for fast settling 12-bit data conversion and acquisition systems.

The LT1122 offset voltage of 120µV, and voltage gain of 500,000 also support the 12-bit accurate applications.

The input bias current of 10pA and offset current of 4pA combined with its speed allow the LT1122 to be used in such applications as high speed sample and hold amplifiers, peak detectors, and integrators.

TYPICAL APPLICATION

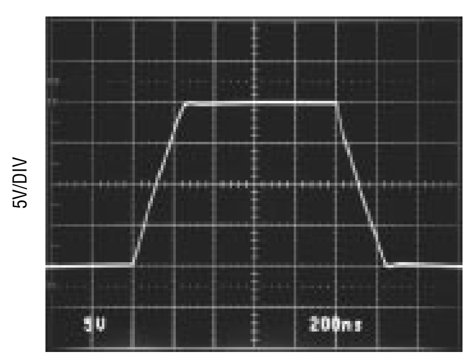
12-Bit Voltage Output D/A Converter



12-BIT CURRENT OUTPUT D/A CONVERTER
C_f = 5pF TO 17pF
(DEPENDING ON D/A CONVERTER USED)

LT1122•TA01

Large-Signal Response



200ns/DIV
AV = –1

1122 TA07

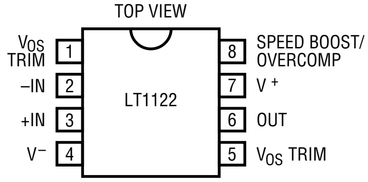
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±20V
Differential Input Voltage .... ±40V
Input Voltage .... ±20V
Output Short Circuit Duration .... Indefinite
Lead Temperature (Soldering, 10 sec.)................. 300°C

Operating Temperature Range
LT1122AM/BM/CM/DM .... – 55°C to 125°C
LT1122AC/BC/CC/DC/CS/DS .... – 40°C to 85°C
Storage Temperature Range
All Devices .... – 65°C to 150°C

PACKAGE/ORDER INFORMATION

TOP VIEW

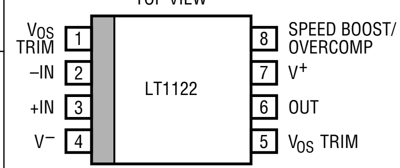


N8 PACKAGE 8-LEAD PLASTIC DIP
J8 PACKAGE 8-LEAD HERMETIC DIP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 175°C, θ_{JA} = 100°C/W (J8)

ORDER PART NUMBER	
LT1122AMJ8	LT1122CCJ8
LT1122BMJ8	LT1122DCJ8
LT1122CMJ8	LT1122ACN8
LT1122DMJ8	LT1122BCN8
LT1122ACJ8	LT1122CCN8
LT1122BCJ8	LT1122DCN8

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SOIC

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

ORDER PART NUMBER
LT1122CS8
LT1122DS8
PART MARKING
1122C
1122D

Consult factory for Industrial grade parts.

ELECTRICAL CHARACTERISTICS V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	LT1122AM/BM LT1122AC/BC MIN	TYP	MAX	LT1122CM/DM LT1122CC/DC LT1122CS/DS MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			120	600		130	900	µV
I_{OS}	Input Offset Current			4	40		5	50	pA
I_B	Input Bias Current			10	75		12	100	pA
	Input Resistance Differential Common Mode	 V_{CM} = – 10V to + 8V V_{CM} = + 8V to + 11V		 10^{12} 10^{12} 10^{11}			 10^{12} 10^{12} 10^{11}		 Ω Ω Ω
	Input Capacitance			4			4		pF
S_R	Slew Rate	A_V = – 1	60	80		50	75		V/µs
	Settling Time (Note 2)	+ 10V to 0V, – 10V to 0V 100% Tested: A and C Grades to 1mV at Sum Node B and D Grades to 1mV at Sum Node All Grades to 0.5mV at Sum Node		 340 350 450	 540		 350 360 470	 590	 ns ns ns
GBW	Gain Bandwidth Product Power Bandwidth	 V_{OUT} = 20Vp-p		14 1.2			13 1.1		MHz MHz
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2kΩ V_{OUT} = ±10V, R_L = 600Ω	180 130	500 250		150 110	450 220		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10V	83	99		80	98		dB
	Input Voltage Range	(Note 3)	±10.5	±11		±10.5	±11		V
PSRR	Power Supply Rejection Ratio	V_S = ±10V to ±18V	86	103		82	101		dB
	Input Noise Voltage	0.1Hz to 10Hz		3.0			3.3		μV_{P-P}
	Input Noise Voltage Density	f_O = 100Hz f_O = 10kHz		25 14			27 15		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
	Input Noise Current Density	f_O = 100Hz, f_O = 10kHz		2			2		$fA/\sqrt{Hz}$

LINEAR TECHNOLOGY

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1122AM/BM LT1122AC/BC MIN	TYP	MAX	LT1122CM/DM LT1122CC/DC LT1122CS/DS MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage Swing	$R_L = 2k\Omega$	±12	±12.5		±12	±12.5		V
		$R_L = 600\Omega$	±11.5	±12		±11.5	±12		V
I_S	Supply Current			7.5	10		7.8	11	mA
	Minimum Supply voltage	(Note 4)	±5			±5			V
	Offset Adjustment Range	$R_{POT} \geq 10k$, Wiper to V^+	±4	±10		±4	±10		mV

$V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1122AC/BC MIN	TYP	MAX	LT1122CC/DC LT1122CS/DS MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		•		350	1400		400	2000	µV
	Average Temperature Coefficient of Input Offset Voltage		●		5	18		6	25	µV/°C
I_{OS}	Input Offset Current		●		12	150		15	200	pA
I_B	Input Bias Current		●		80	600		90	800	pA
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	120	380		100	340		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	82	98		78	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	84	101		80	99		dB
	Input Voltage Range		●	±10	±10.8		±10	±10.8		V
V_{OUT}	Output Voltage Swing	$R_L = 2k\Omega$	●	±11.5	±12.4		±11.5	±12.4		V
S_R	Slew Rate	$A_V = -1$	●	50	70		40	65		V/µs

$V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted. (Note 1)

SYMBOL	PARAMETER	CONDITIONS		LT1122AM/BM MIN	TYP	MAX	LT1122CM/DM MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		650	2400		800	3400	µV
	Average Temperature Coefficient of Input Offset Voltage		●		6	18		7	25	µV/°C
I_{OS}	Input Offset Current		●		0.5	6		0.6	9	nA
I_B	Input Bias Current		●		6	25		7	35	nA
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	●	70	230		60	200		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	80	97		76	94		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	83	100		78	98		dB
	Input Voltage Range		●	±10	±10.5		±10	±10.5		V
V_{OUT}	Output Voltage Swing	$R_L = 2k\Omega$	●	±11.3	±12.1		±11.3	±12.1		V
S_R	Slew Rate	$A_V = -1$	●	45	60		35	55		V/µs

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: The LT1122 is measured in an automated tester in less than one second after application of power. Depending on the package used, power dissipation, heat sinking, and air flow conditions, the fully warmed up chip temperature can be 10°C to 50°C higher than the ambient temperature.

Note 2: Settling time is 100% tested for A and C grades using the settling time test circuit shown. This test is not included in quality assurance sample testing.

Note 3: Input voltage range functionality is assured by testing offset voltage at the input voltage range limits to a maximum of 4mV (A, B grades), to 5.7mV (C, D grades).

Note 4: Minimum supply voltage is tested by measuring offset voltage to 7mV maximum at ±5V supplies.

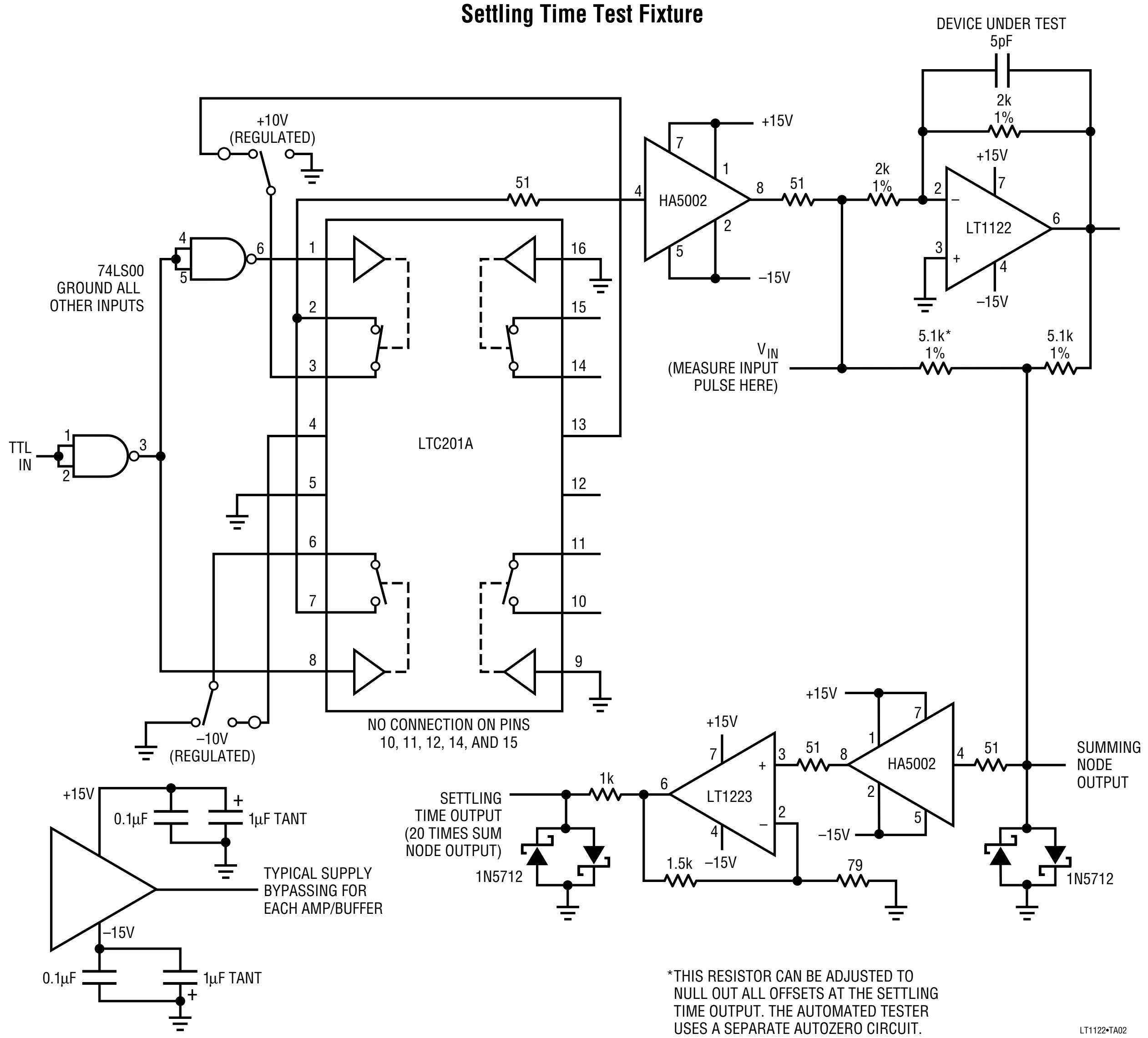
Note 5: The LT1122 is not tested and not quality-assurance-sampled at – 40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from – 55°C, 0°C, 25°C, 70°C and/or 125°C tests.

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 5)

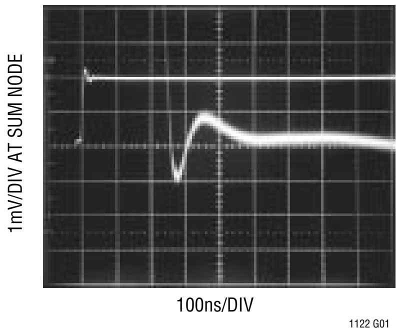
SYMBOL	PARAMETER	CONDITIONS		LT1122AC/BC MIN	LT1122AC/BC TYP	LT1122AC/BC MAX	LT1122CC/DC LT1122CS/DS MIN	LT1122CC/DC LT1122CS/DS TYP	LT1122CC/DC LT1122CS/DS MAX	UNITS
V_{OS}	Input Offset Voltage		●		450	1900		500	2700	µV
	Average Temperature Coefficient of Input Offset Voltage		●		6	20		7	28	µV/°C
I_{OS}	Input Offset Current		●		30	600		40	900	pA
I_B	Input Bias Current		●		230	2000		260	2700	pA
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \ge 2k\Omega$	●	95	340		80	300		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	80	98		76	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	83	100		78	98		dB
	Input Voltage Range		●	±10	±10.6		±10	±10.6		V
V_{OUT}	Output Voltage Swing	$R_L = 2k\Omega$	●	±11.3	±12.2		±11.3	±12.2		V
S_R	Slew Rate	$A_V = -1$	●	45	65		35	60		V/µs

Settling Time Test Fixture

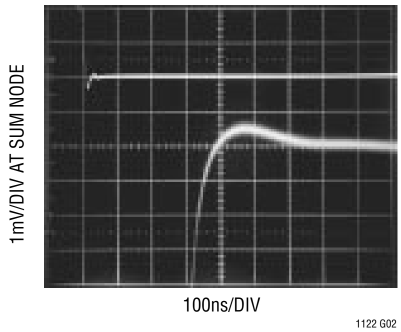


TYPICAL PERFORMANCE CHARACTERISTICS

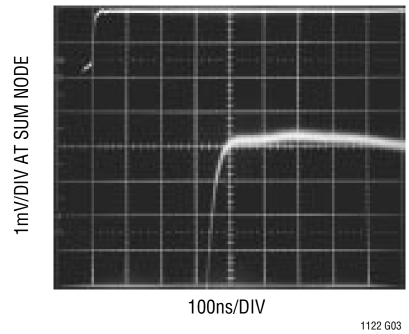
Settling Time (Input From –10V to 0V)



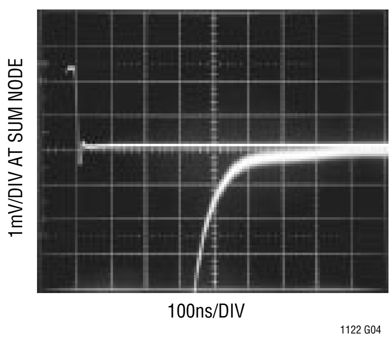
Settling Time (Input From +10V to 0V)



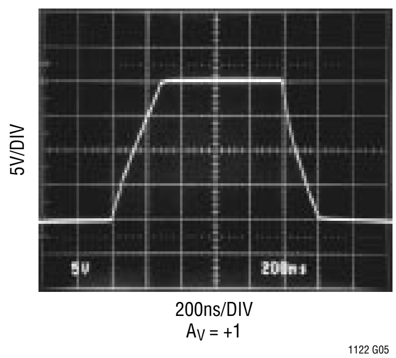
Settling Time (Input From 0V to +10V)



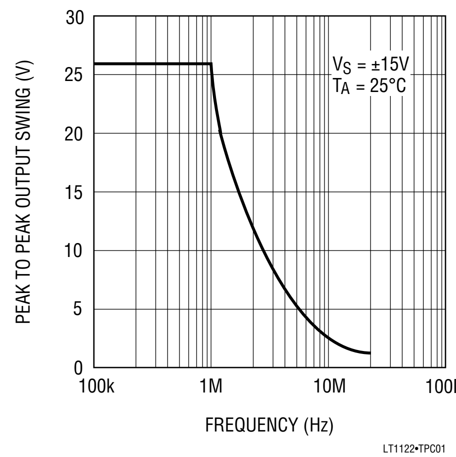
Settling Time (Input From 0V to –10V)



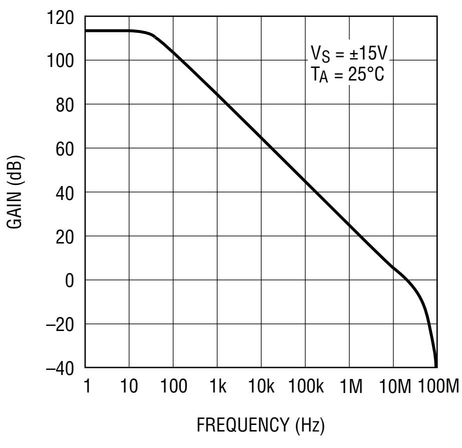
Large Signal Response



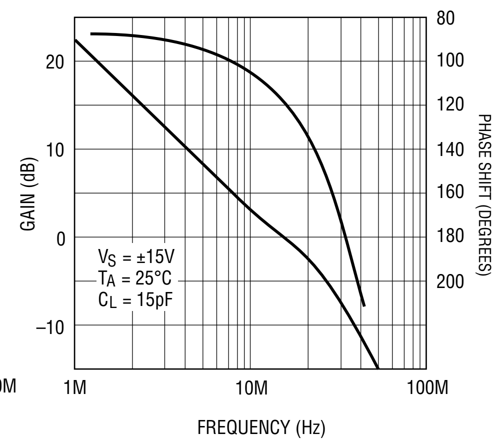
Undistorted Output Swing vs Frequency



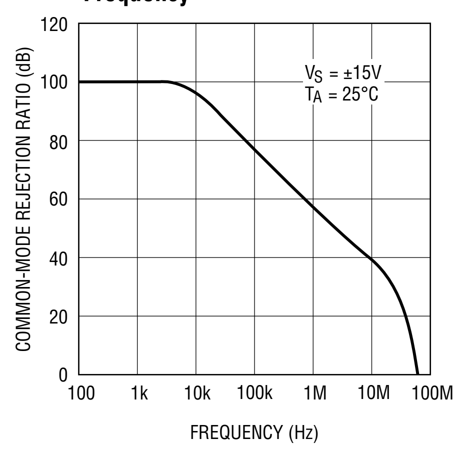
Voltage Gain vs Frequency



Gain, Phase vs Frequency

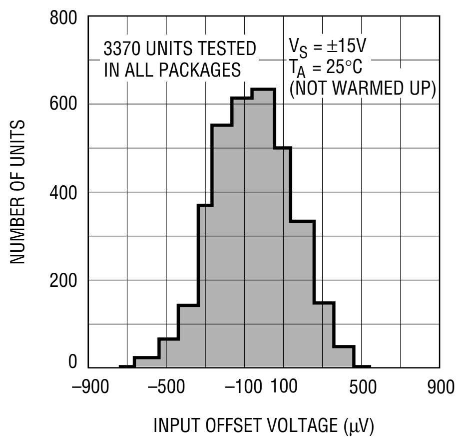


Common Mode Rejection vs Frequency



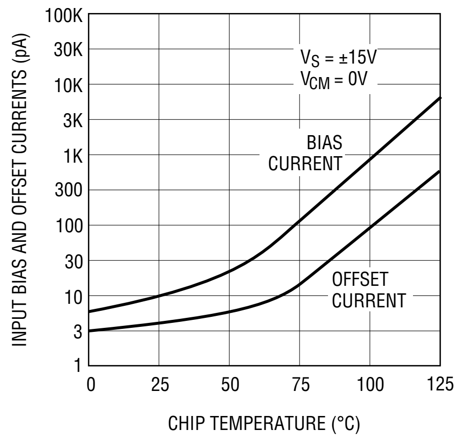
TYPICAL PERFORMANCE CHARACTERISTICS

Distribution of Input Offset Voltage



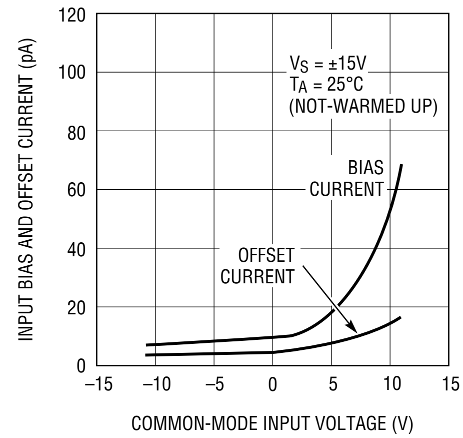
LT1122•TPC05

Input Bias and Offset Currents Over Temperature



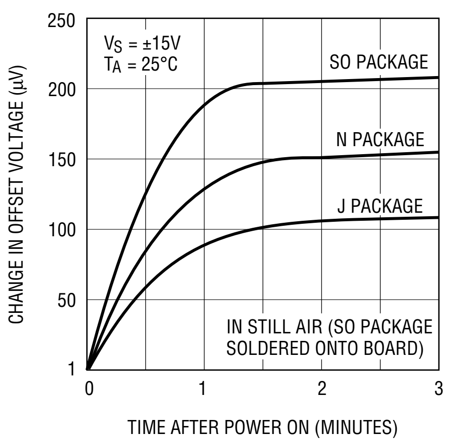
LT1122•TPC06

Bias and Offset Currents Over The Common-Mode Range



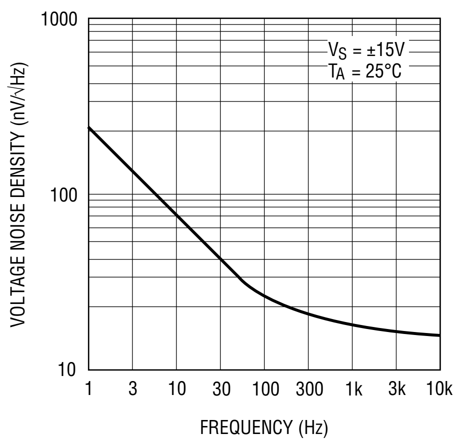
LT1122•TPC07

Warm-up Drift



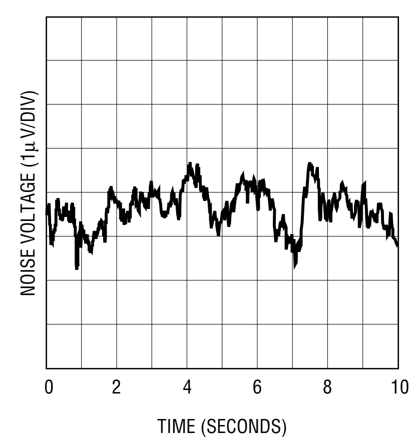
LT1122•TPC08

Noise Spectrum



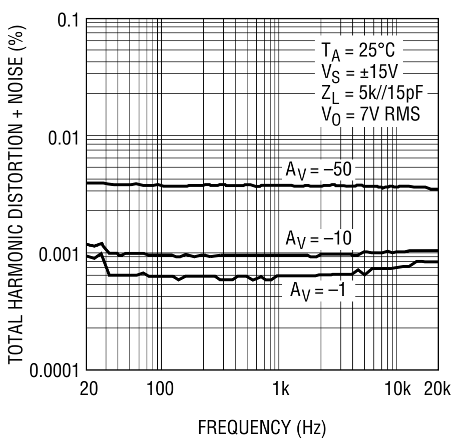
LT1122•TPC09

0.1Hz to 10Hz Noise



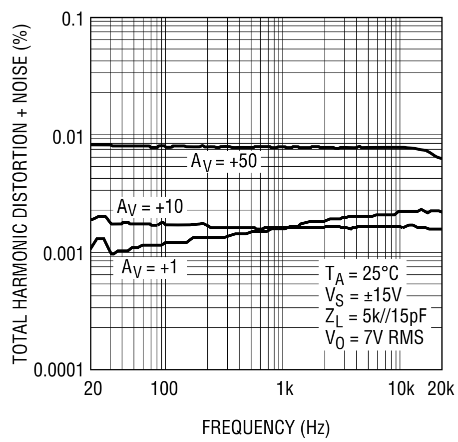
LT1122•TPC10

Total Harmonic Distortion + Noise vs Frequency Inverting Gain



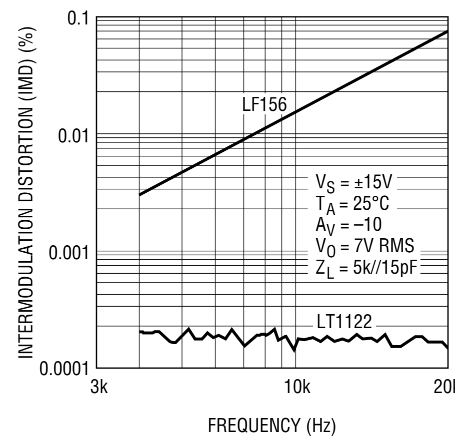
LT1122•TPC11

Total Harmonic Distortion + Noise vs Frequency Non-Inverting Gain



LT1122•TPC12

Intermodulation Distortion (CCIF Method) vs Frequency LT1122 and LF156*



*SEE LT1115 DATA SHEET FOR DEFINITION OF CCIF TESTING

LT1122•TPC13

LINEAR TECHNOLOGY

APPLICATIONS INFORMATION

Settling Time Measurements

Settling time test circuits shown on some competitive devices' data sheets require:

1. A "flat top" pulse generator. Unfortunately, flat top pulse generators are not commercially available.
2. A variable feedback capacitor around the device under test. This capacitor varies over a four to one range. Presumably, as each op amp is measured for settling time, the capacitor is fine tuned to optimize settling time for that particular device.
3. A small inductor load to optimize settling.

The LT1122's settling time is 100% tested in the test circuit shown. No "flat top" pulse generator is required. The test circuit can be readily constructed, using commercially available ICs. Of course, standard high frequency board construction techniques should be followed. All LT1122s are measured with a constant feedback capacitor. No fine tuning is required.

Speed Boost/Overcompensation Terminal

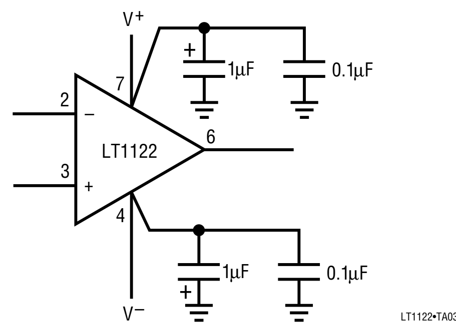
Pin 8 of the LT1122 can be used to change the input stage operating current of the device. Shorting pin 8 to the positive supply (Pin 7) increases slew rate and bandwidth by about 25%, but at the expense of a reduction in phase margin by approximately 18 degrees. Unity gain capacitive load handling decreases from typically 500pF to 100pF.

Conversely, connecting a 15k resistor from pin 8 to ground pulls 1mA out of pin 8 (with V^+ = 15V). This reduces slew rate and bandwidth by 25%. Phase margin and capacitive load handling improve; the latter typically increasing to 800pF.

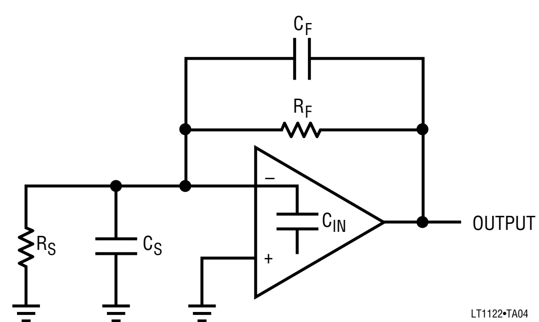
High Speed Operation

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress and component placement.

The power supply connections to the LT1122 must maintain a low impedance to ground over a bandwidth of 20MHz. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1μF ceramic and a 1μF electrolytic capacitor, as shown, placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications.

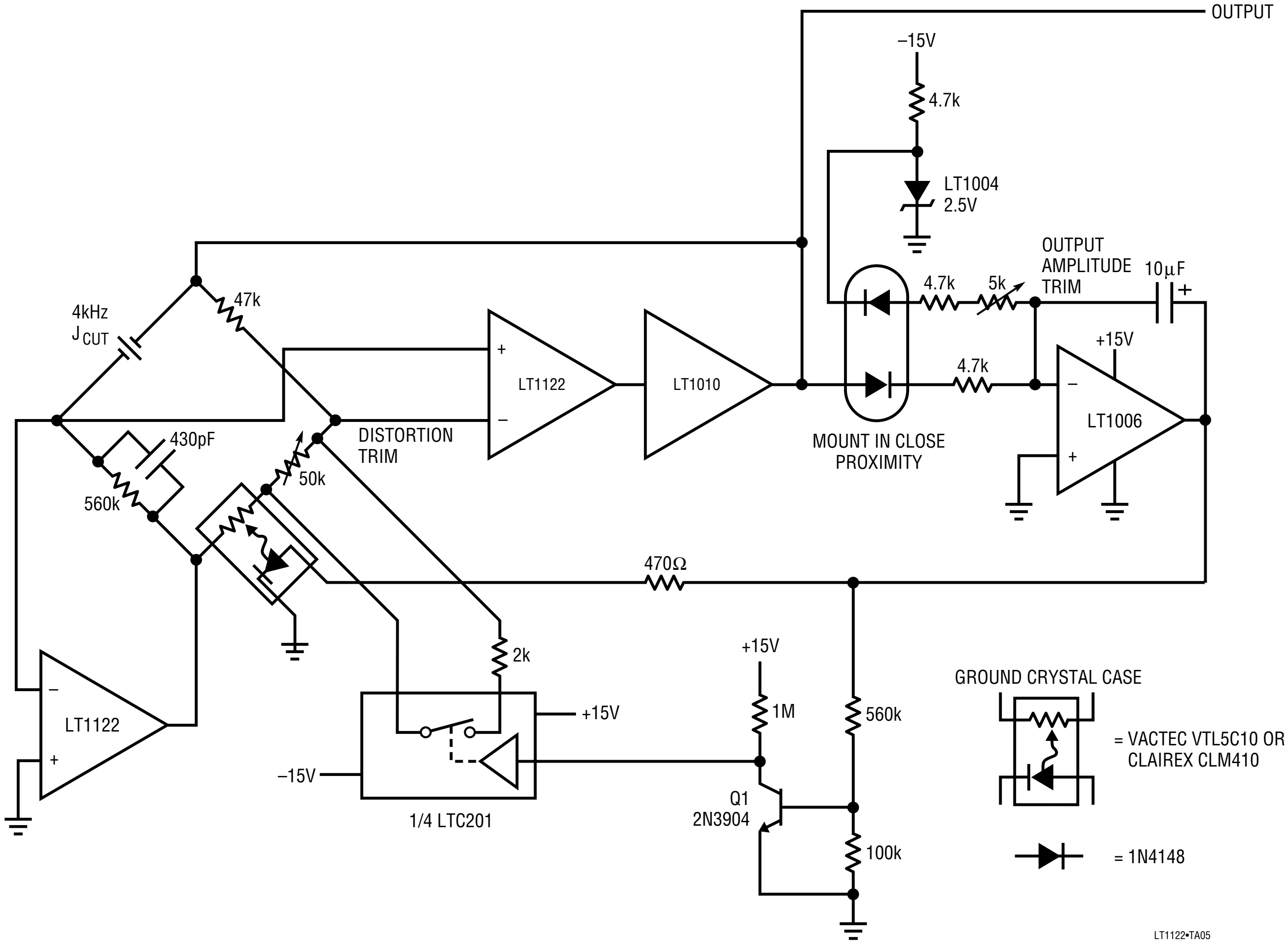


When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx$ 4pF). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_FC_F$, the effect of the feedback pole is completely removed.

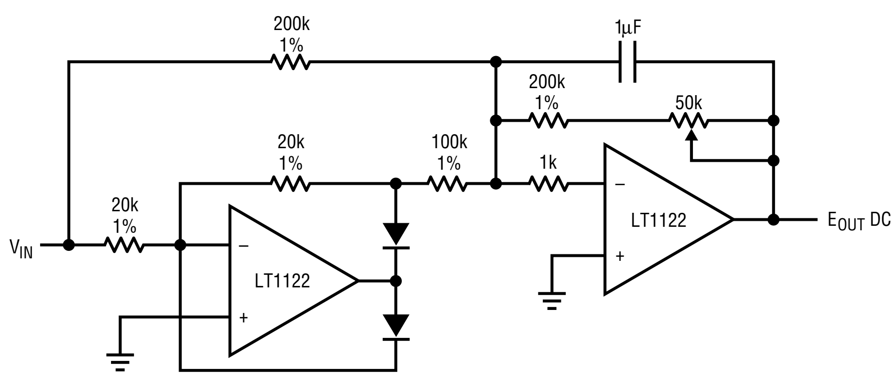


TYPICAL APPLICATIONS

Quartz Stabilized Oscillator With 9ppm Distortion



Wide-Band, Filtered, Full Wave Rectifier



PACKAGE DESCRIPTION

Please see the *1994 Linear Databook Volume III* for package descriptions.