International IƱR Rectifier

Data Sheet No. PD60251

IRS2112(-1,-2,S)PbF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground +/- 5 V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant

Product Summary

| V_{OFFSET}	600 V max.
I_O+/-	200 mA / 440 mA
V_{OUT}	10 V - 20 V
$t_{on/off}$ (typ.)	135 ns & 105 ns
Delay Matching	30 ns

Description

The IRS2112 is a high voltage, high speed power MOSFET and IGBT driver with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Packages

14-Lead PDIP
IRS2112

16-Lead PDIP
(w/o leads 4 & 5)
IRS2112-2

14-Lead PDIP
(w/o lead 4)
IRS2112-1

16-Lead SOIC
IRS2112S

Typical Connection

up to 600 V

TO LOAD

(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

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1

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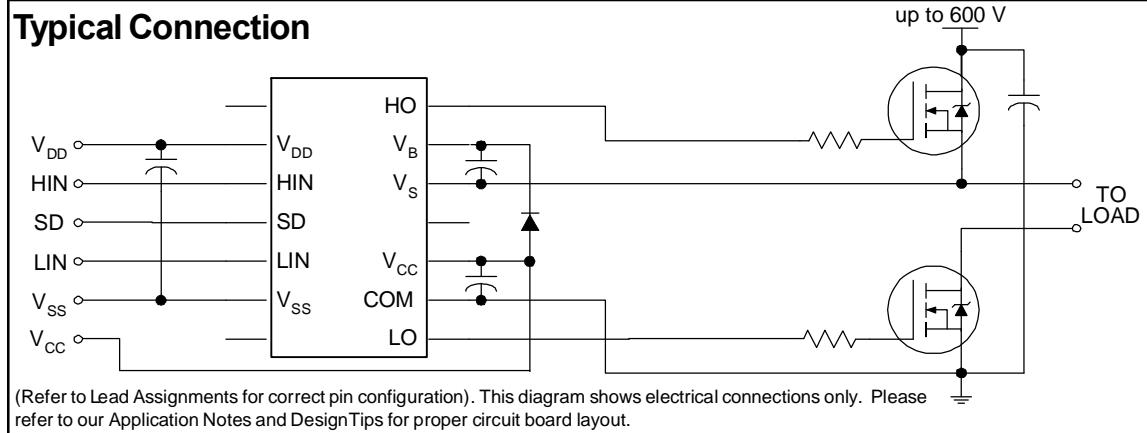
Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figs. 28 through 35.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating supply voltage		-0.3	625	
V_S	High-side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side fixed supply voltage		-0.3	25	V
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage		-0.3	V_{SS} + 25	
V_{SS}	Logic supply offset voltage		V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (Fig. 2)		—	50	V/ns
P_D	Package power dissipation @ TA ≤ +25 °C	(14 Lead DIP)	—	1.6	W
		(16 Lead SOIC)	—	1.25	
RTH_{JA}	Thermal resistance, junction to ambient	(14 Lead DIP)	—	75	°C/W
		(16 Lead SOIC)	—	100	
T_J	Junction temperature		—	150	
T_S	Storage temperature		-55	150	°C
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15 V differential. Typical ratings at other bias conditions are shown in Figs. 36 and 37.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply absolute voltage	V_S + 10	V_S + 20	
V_S	High-side floating supply offset voltage	Note 1	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	V
V_{DD}	Logic supply voltage	V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic supply offset voltage	-5 (Note 2)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).
Note 2: When V_{DD} < 5 V, the minimum V_{SS} offset is limited to -V_{DD}.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V, C_L = 1000 pF, T_A = 25 °C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	135	180		V_S = 0 V
t_{off}	Turn-off propagation delay	—	130	160		V_S = 600 V
t_{sd}	Shutdown propagation delay	—	130	160	ns	
t_r	Turn-on rise time	—	75	130		
t_f	Turn-off fall time	—	35	65		
MT	Delay matching, HS & LS Turn-on/off	—	—	30		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V, T_A = 25 °C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN, and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	9.5	—	—		
V_{IL}	Logic "0" input voltage	—	—	6.0	V	
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.05	0.2		I_O = 2 mA
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{LK}	Offset supply leakage current	—	—	50		$V_B = V_S$ = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	25	100		
I_{QCC}	Quiescent V_{CC} supply current	—	80	180		V_{IN} = 0 V or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	—	2.0	30	µA	
I_{IN+}	Logic "1" input bias current	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" input bias current	—	—	1.0		V_{IN} = 0 V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.4	8.5	9.6		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.0	8.1	9.2	V	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.2	8.2	9.2		
I_{O+}	Output high short circuit pulsed current	200	290	—	mA	V_O = 0 V, $V_{IN} = V_{DD}$ PW $\leq$ 10 µs
I_{O-}	Output low short circuit pulsed current	420	600	—		V_O = 15 V, V_{IN} = 0 V PW $\leq$ 10 µs

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Functional Block Diagram
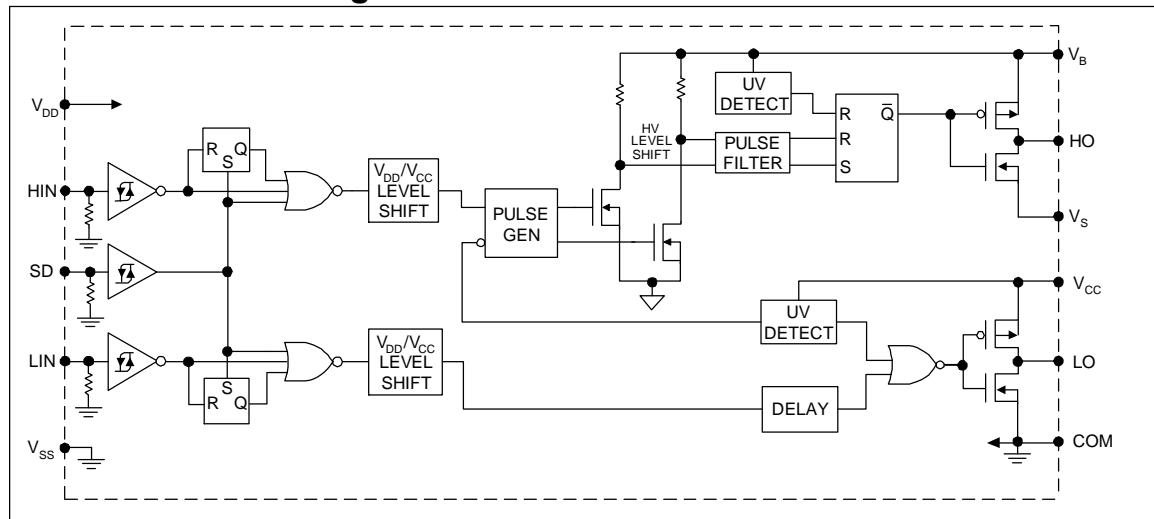
Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high-side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low-side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side supply
LO	Low-side gate drive output
COM	Low-side return

Lead Assignments
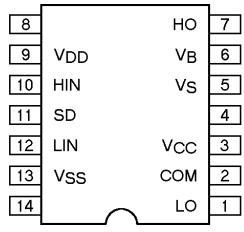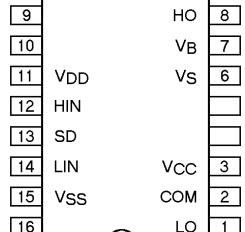
14 Lead PDIP **IRS2112**	16 Lead SOIC (Wide Body) **IRS2112S**
14 Lead PDIP w/o lead 4 **IRS2112-1**	16 Lead PDIP w/o leads 4 & 5 **IRS2112-2**
Part Number	
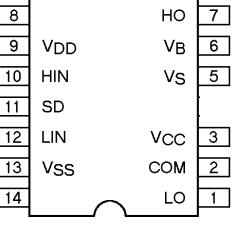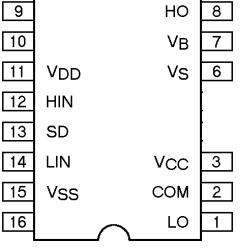
14 Lead PDIP — IRS2112

Pin	Signal	Signal	Pin
8		HO	7
9	VDD	VB	6
10	HIN	VS	5
11	SD		4
12	LIN	VCC	3
13	VSS	COM	2
14		LO	1

16 Lead SOIC (Wide Body) — IRS2112S

Pin	Signal	Signal	Pin
9		HO	8
10		VB	7
11	VDD	VS	6
12	HIN		
13	SD		
14	LIN	VCC	3
15	VSS	COM	2
16		LO	1

14 Lead PDIP w/o lead 4 — IRS2112-1

Pin	Signal	Signal	Pin
8		HO	7
9	VDD	VB	6
10	HIN	VS	5
11	SD		
12	LIN	VCC	3
13	VSS	COM	2
14		LO	1

16 Lead PDIP w/o leads 4 & 5 — IRS2112-2

Pin	Signal	Signal	Pin
9		HO	8
10		VB	7
11	VDD	VS	6
12	HIN		
13	SD		
14	LIN	VCC	3
15	VSS	COM	2
16		LO	1

IRS2112(-1,-2,S)PbF

Figure 1. Input/Output Timing Diagram
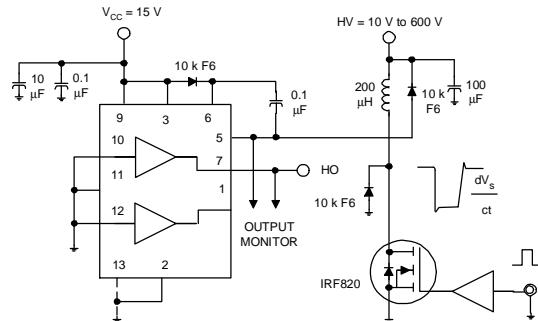
Figure 2. Floating Supply Voltage Transient Test Circuit
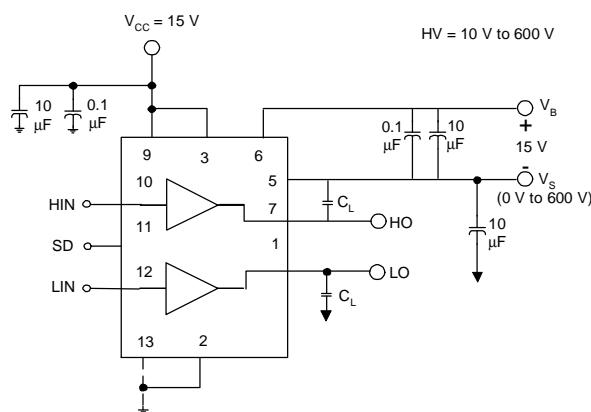
Figure 3. Switching Time Test Circuit
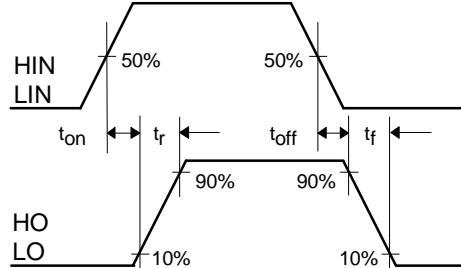
Figure 4. Switching Time Waveform Definition
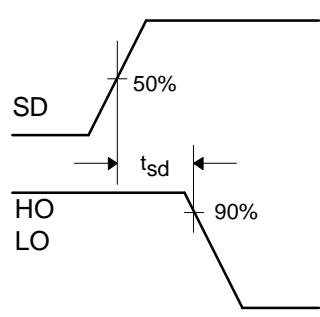
Figure 5. Shutdown Waveform Definitions
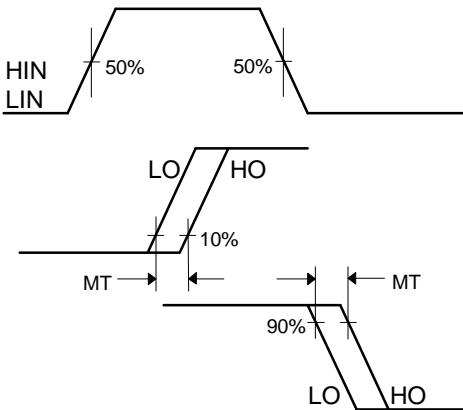
Figure 6. Delay Matching Waveform Definitions

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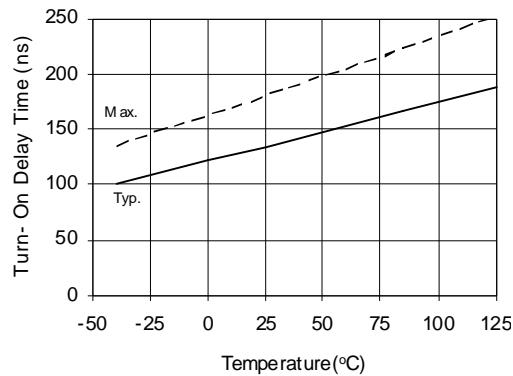
Figure 7A. Turn-On Propagation Delay Time vs. Temperature
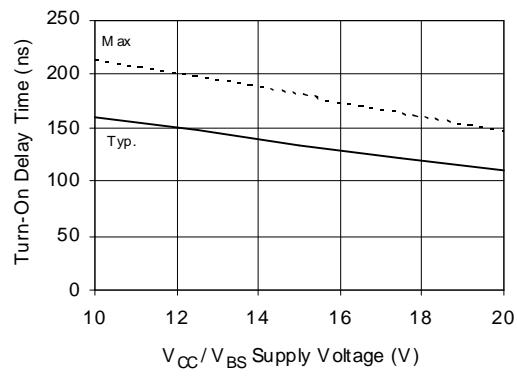
Figure 7B. Turn-On Propagation Delay Time vs. V_{CC}/V_{BS} Supply Voltage
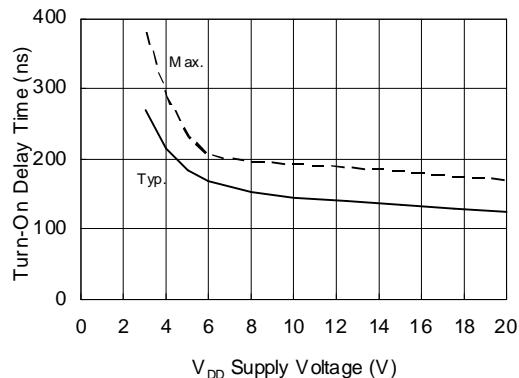
Figure 7C. Turn-On Propagation Delay Time vs. V_{DD} Supply Voltage
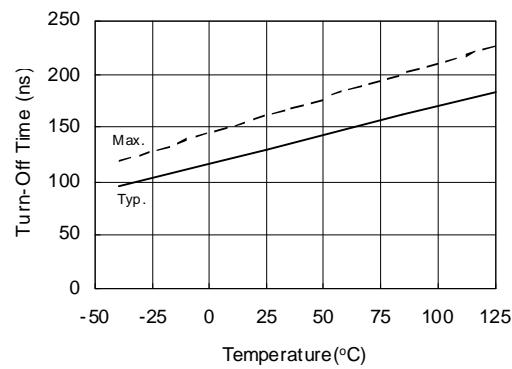
Figure 8A. Turn-Off Propagation Delay Time vs. Temperature
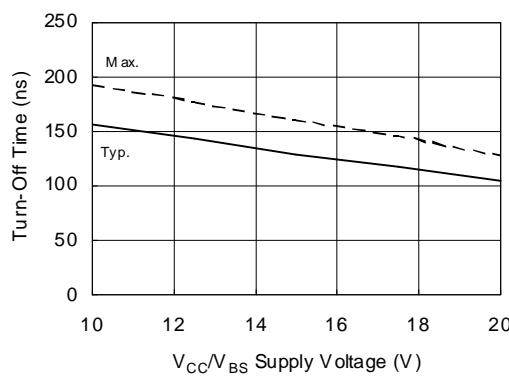
Figure 8B. Turn-Off Propagation Delay Time vs. V_{CC}/V_{BS} Supply Voltage
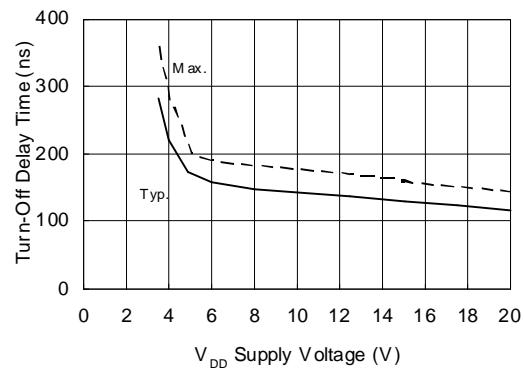
Figure 8C. Turn-Off Propagation Delay Time vs. V_{DD} Supply Voltage

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7

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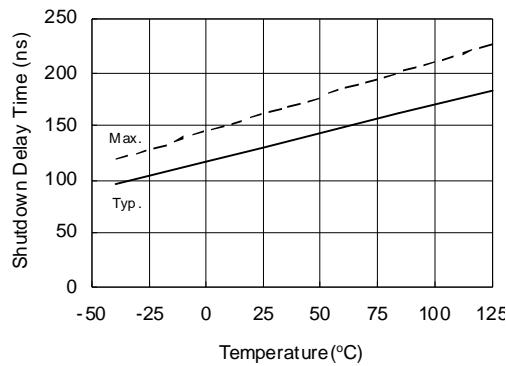
**Figure 9A. Shutdown Delay Time
vs. Temperature**
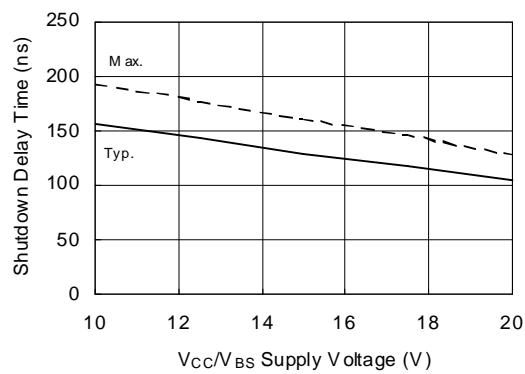
**Figure 9B. Shutdown Delay Time
vs. V_{CC}/V_{BS} Supply Voltage**
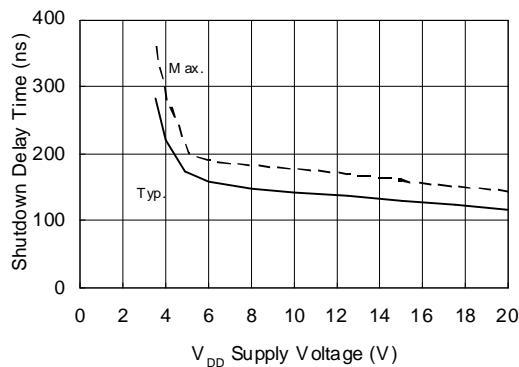
Figure 9C. Shutdown Time vs. V_{DD} Supply Voltage
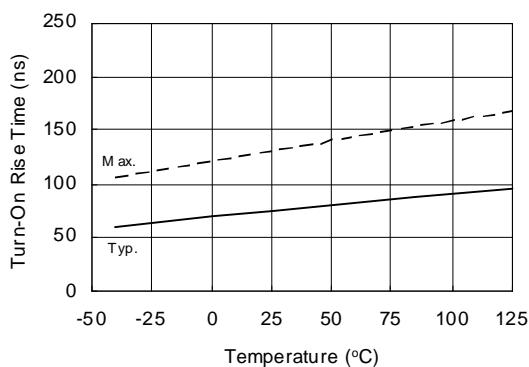
Figure 10A. Turn-On Rise Time vs. Temperature
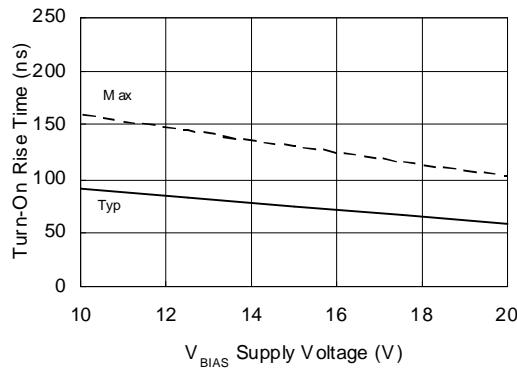
Figure 10B. Turn-On Rise Time vs. Voltage
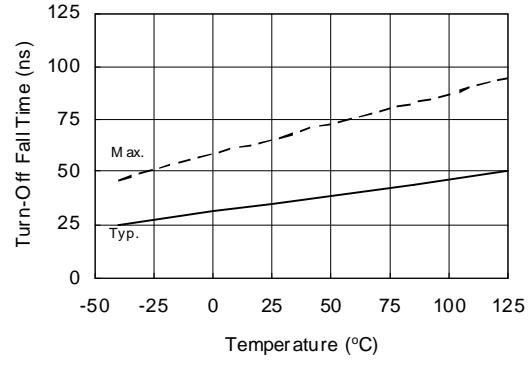
Figure 11A. Turn-Off Fall Time vs. Temperature

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8

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Figure 11B. Turn-Off Fall Time vs. Supply Voltage
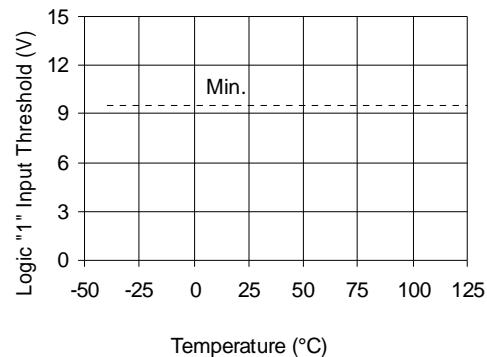
**Figure 12A. Logic "I" Input Threshold
vs. Temperature**
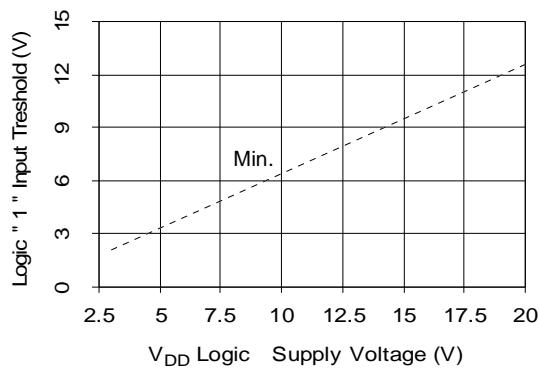
**Figure 12B. Logic "I" Input Threshold
vs. Voltage**
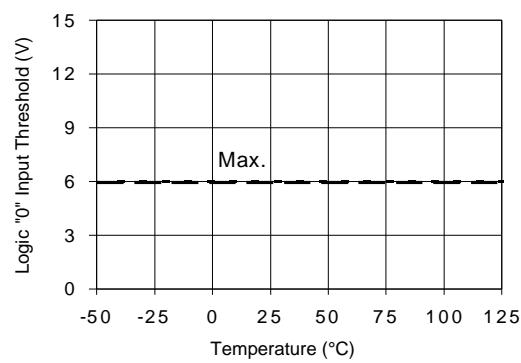
**Figure 13A. Logic "0" Input Threshold
vs. Temperature**
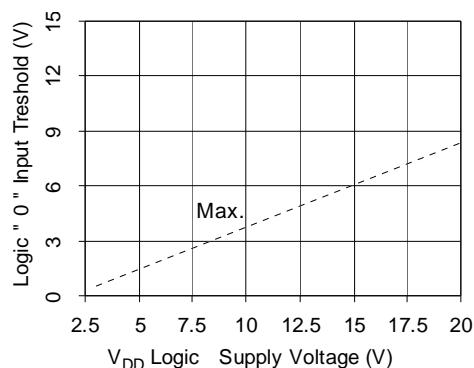
**Figure 13B. Logic "0" Input Threshold
vs. Voltage**
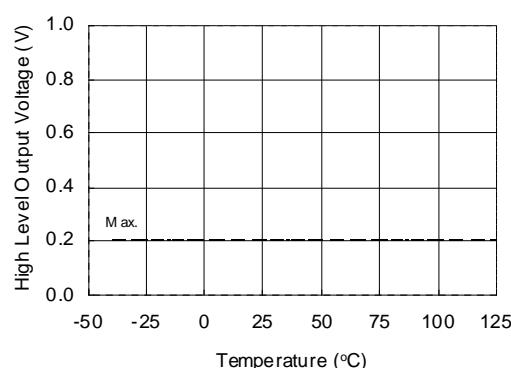
**Figure 14A. High Level Output Voltage
vs. Temperature (I_O = 2 mA)**

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9
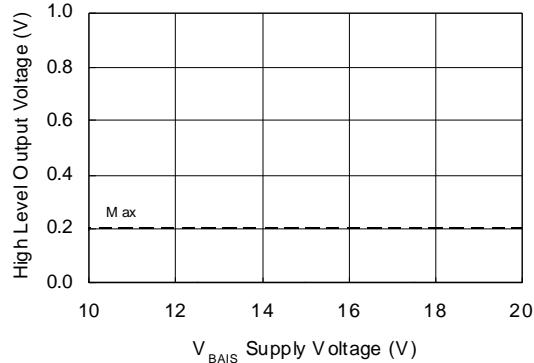
**Figure 14B. High Level Output Voltage vs. Supply Voltage (I$_O$ = 2 mA)**

**Figure 15A. Low Level Output Voltage vs. Temperature (I$_O$ = 2 mA)**

Figure 15B. Low Level Output Voltage vs. Supply Voltage (I$_O$ = 2 mA)
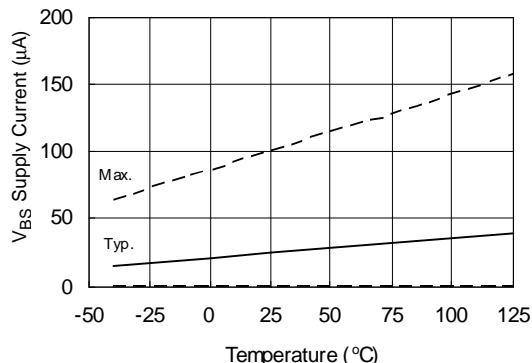

Figure 16A. V$_{BS}$ Supply Current vs. Temperature
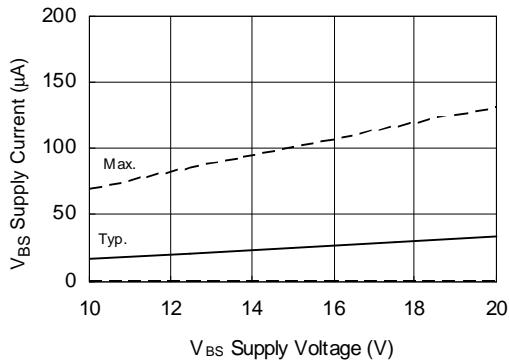
**Figure 16B. V$_{BS}$ Supply Current vs. Voltage**
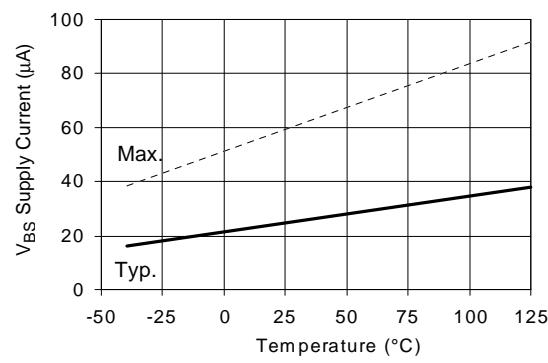
Figure 17A. V$_{BS}$ Supply Current vs. Temperature

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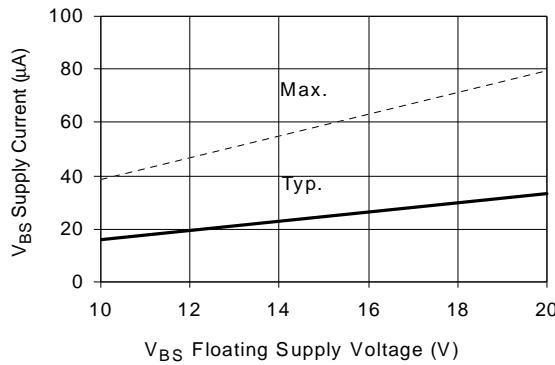
Figure 17B. V$_{BS}$ Supply Current vs. Voltage
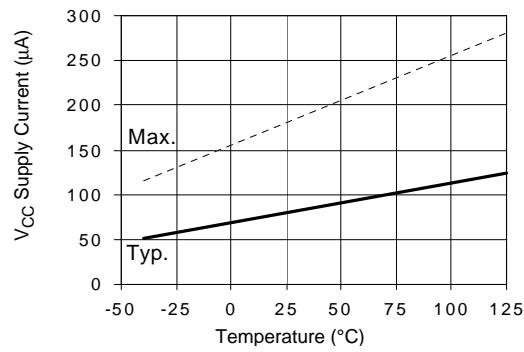

Figure 18A. V$_{CC}$ Supply Current vs. Temperature
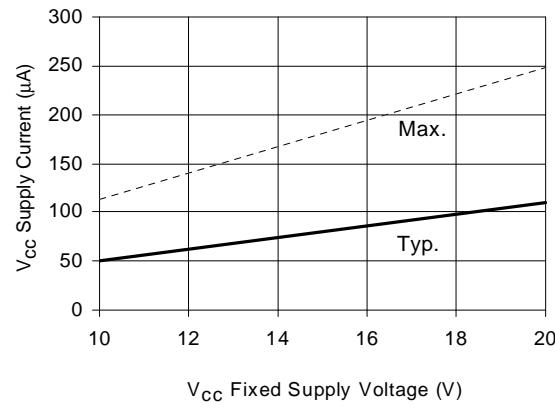
Figure 18B. V$_{CC}$ Supply Current vs. Voltage
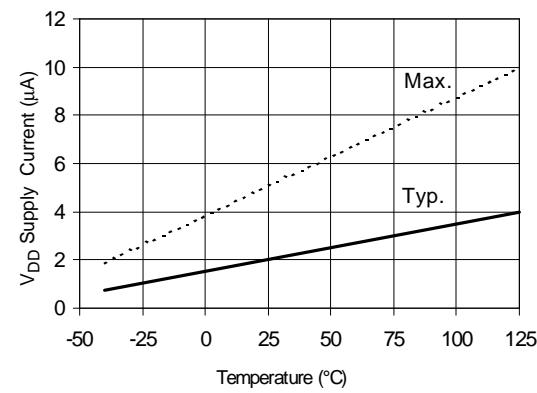
Figure 19A. V$_{DD}$ Supply Current vs. Temperature
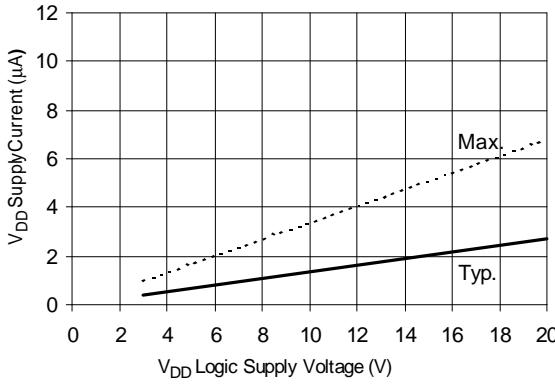
Figure 19B. V$_{DD}$ Supply Current vs. V$_{DD}$ Voltage

Figure 20A. Logic "I" Input Current vs. Temperature

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11

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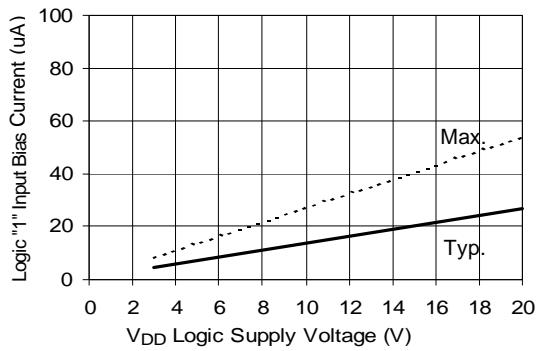
Figure 20B. Logic "1" Input Current vs. V_DD Voltage
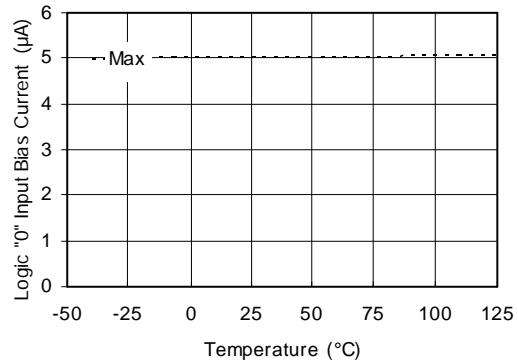
**Figure 21A. Logic "0" Input Bias Current
vs. Temperature**
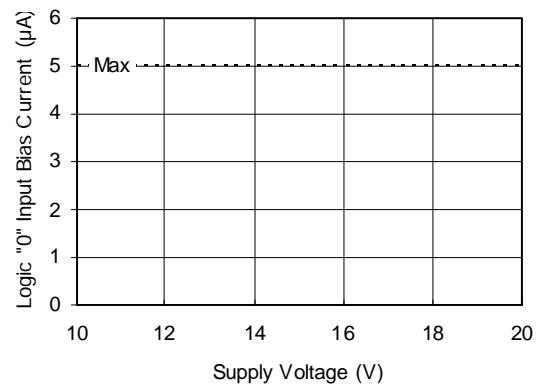
**Figure 21B. Logic "0" Input Bias Current
vs. Voltage**
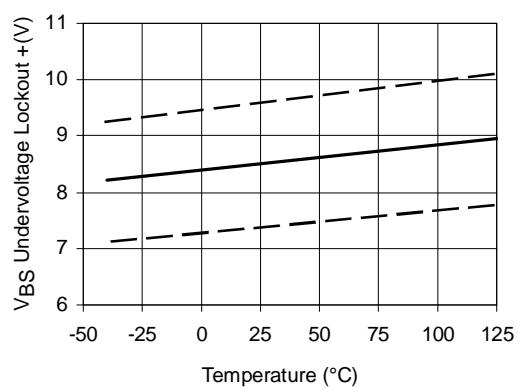
Figure 22. V_BS Undervoltage (+) vs. Temperature
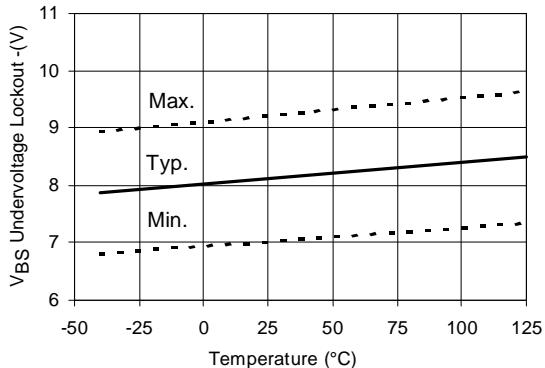
Figure 23. V_BS Undervoltage (-) vs. Temperature
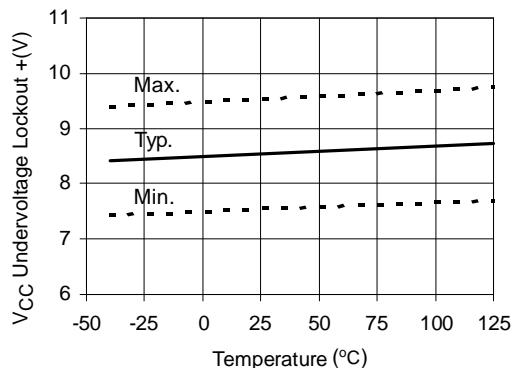
Figure 24. V_CC Undervoltage (-) vs. Temperature

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Figure 25. V$_{CC}$ Undervoltage (-) vs. Temperature
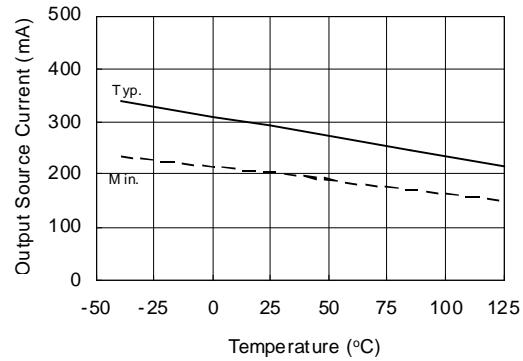
Figure 26A. Output Source Current vs. Temperature
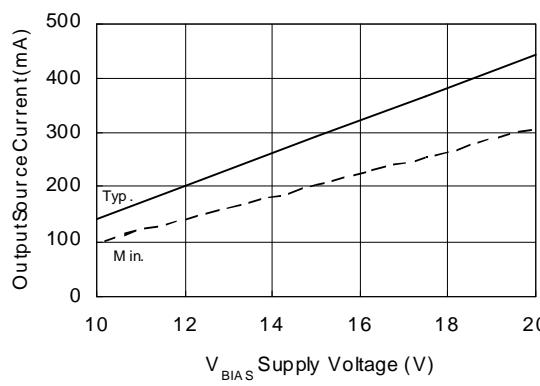
Figure 26B. Output Source Current vs. Supply Voltage
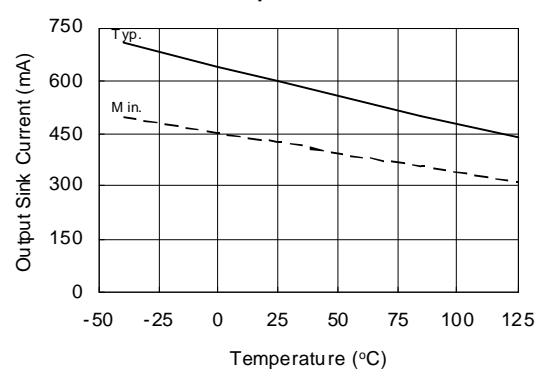
Figure 27A. Output Sink Current vs. Temperature
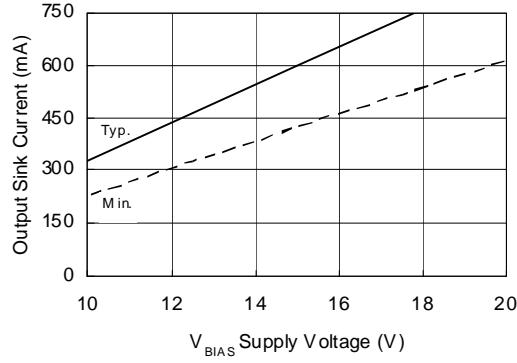
Figure 27B. Output Sink Current vs. Supply Voltage

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13

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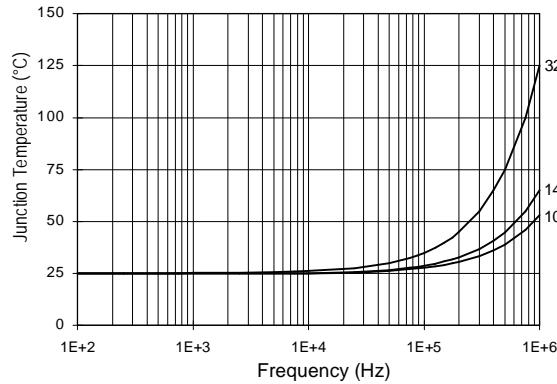
Figure 28. IRS2112 T$_J$ vs. Frequency (IRFBC20)
R$_{GATE}$ = 33 W, V$_{CC}$ = 15 V
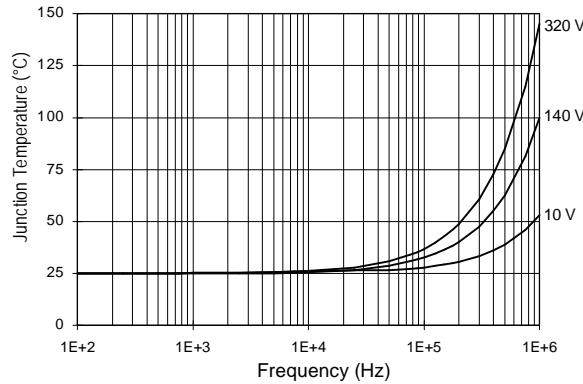
Figure 29. IRS2112 T$_J$ vs. Frequency (IRFBC30)
R$_{GATE}$ = 22 W, V$_{CC}$ = 15 V
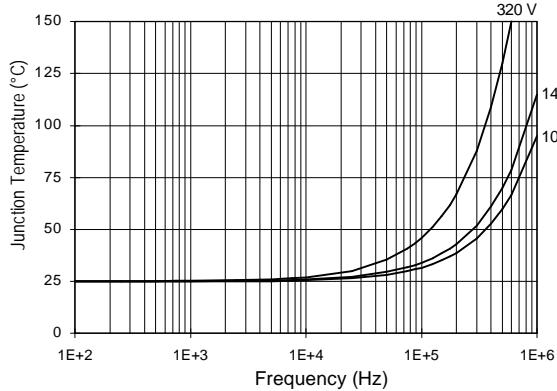
Figure 30. IRS2112 T$_J$ vs. Frequency (IRFBC40)
R$_{GATE}$ = 15 W, V$_{CC}$ = 15 V
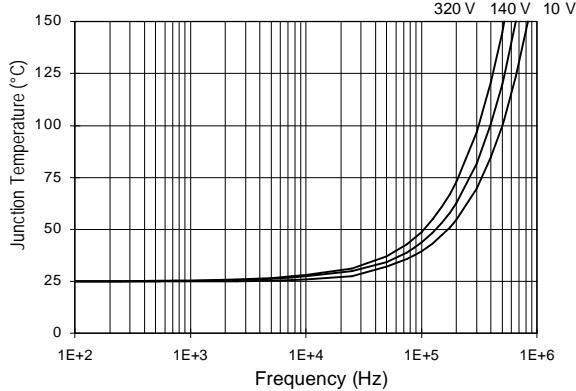
Figure 31. IRS2112 T$_J$ vs. Frequency (IRFPE50)
R$_{GATE}$ = 10 W, V$_{CC}$ = 15 V
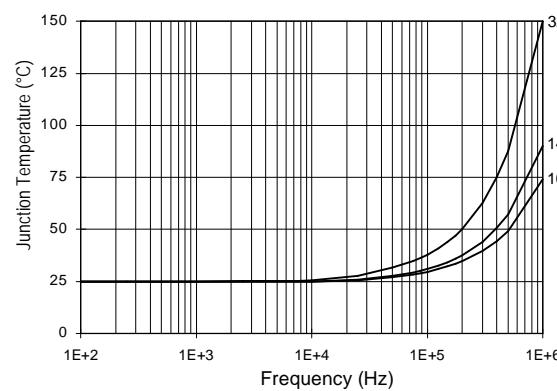
Figure 32. IRS2112S T$_J$ vs. Frequency (IRFBC20)
R$_{GATE}$ = 33 W, V$_{CC}$ = 15 V
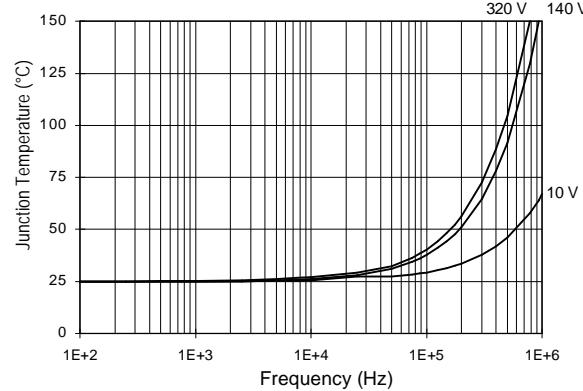
Figure 33. IRS2112S T$_J$ vs. Frequency (IRFBC30)
R$_{GATE}$ = 22 W, V$_{CC}$ = 15 V

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14

IRS2112(-1,-2,S)PbF
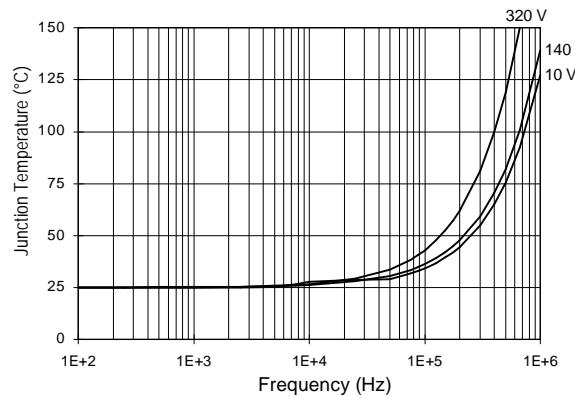
Figure 34. IRS2112S T$_J$ vs. Frequency (IRFBC40)
R$_{GATE}$ = 15 W, V$_{CC}$ = 15 V

Figure 35. IRS2112S T$_J$ vs. Frequency (IRFPE50)
R$_{GATE}$ = 10 W, V$_{CC}$ = 15 V

Figure 36.   Maximum V$_S$ Negative Offset vs.
V$_{BS}$ Supply Voltage

Figure 37.   Maximum V$_{SS}$ Positive Offset vs.
V$_{CC}$ Supply Voltage

International
IOR Rectifier

IRS2112(-1,-2,S)PbF

Case outline


```
20.19 [.795]
18.42 [.725]    -A-
                         6
14                            6

                    7.11 [.280]
                    6.10 [.240]

1                        -B-

14X 1.77 [.070]
    1.15 [.045]

0.39 [.015]
MIN.                      5.33 [.210]
-C-                       MAX

4.06 [.160]
2.93 [.115]
                    14X 0.558 [.022]
                        0.356 [.014]
2.54 [.100]
12X              ⊕ 0.25 [.010] Ⓜ C B Ⓢ A Ⓢ
```

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

```
14X 0°- 15°

7.62 [.300]
  5                  14X 0.381 [.015]
                         0.204 [.008]
```

14-Lead PDIP

01-6010
01-3002 03 (MS-001AC)


```
20.19 [.795]
18.42 [.725]    -A-
                         6
14                            6

                    7.11 [.280]
                    6.10 [.240]

1                        -B-

1.77 [.070]
1.15 [.045]
                    5.08 [.200]
0.39 [.015]
MIN                       5.33 [.210]
-C-                       MAX

4.06 [.160]
2.93 [.115]
                    13X 0.558 [.022]
                        0.356 [.014]
2.54 [.100]
10X              ⊕ 0.25 [.010] Ⓜ C B Ⓢ A Ⓢ
```

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

```
13X 0°- 15°

7.62 [.300]
  5                  13X 0.381 [.015]
                         0.204 [.008]
```

14-Lead PDIP w/o Lead 4

01-6010
01-3008 02 (MS-001AC)

```
21.33 [.840]
18.93 [.745]        -A-

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AA.
5  MEASURED WITH THE LEADS CONSTRAINED TO BE
    PERPENDICULAR TO DATUM PLANE C.
6  DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD
    PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

7.11 [.280]
6.10 [.240]
-B-

14X  1.77 [.070]
     1.15 [.045]
1.27 [.050]

0.39 [.015]
MIN
-C-
5.33 [.210]
MAX

4.06 [.160]
2.93 [.115]

2.54 [.100]
11X
14X  0.558 [.022]
     0.356 [.014]

7.62 [.300]

⊕ 0.25 [.010] Ⓜ C BⓈ AⓈ

14X 0°- 15°

7.62 [.300]
5
14X  0.381 [.015]
     0.204 [.008]
```

16 Lead PDIP w/o Leads 4 & 5

01-6015
01-3010 02


```
10.50 [.4133]
10.10 [.3977]        -A-    6

6
7.60 [.2992]
7.40 [.2914]
-B-

10.65 [.419]
10.00 [.394]

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AA.
5  DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO
    A SUBSTRATE.
6  DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD
    PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

⊕ 0.25 [.010] Ⓜ C BⓂ

0.635 [.025]

0.30 [.0118]
0.10 [.0040]

-C-

1.27 [.050]
14X
16X  0.49 [.0192]
     0.35 [.0138]

⊕ 0.25 [.010] Ⓜ C BⓈ AⓈ

0.75 [.029]
0.25 [.010]  X 45°

0° - 8°

2.65 [.1043]
2.35 [.0926]

16X  1.27 [.050]
     0.40 [.016]
16X  0.32 [.0125]
     0.23 [.0091]
5
```

16-Lead SOIC (wide body)

01 6015
01-3014 03 (MS-013AA)

IRS2112(-1,-2,S)PbF

Tape & Reel
16-Lead SOIC

LOADED TAPE FEED DIRECTION

NOTE : CONTROLLING
DIMENSION IN MM

CARRIER TAPE DIMENSION FOR 16 SOIC W

Code	Metric		Imperial	
	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	10.80	11.00	0.425	0.433
F	10.60	10.80	0.417	0.425
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062
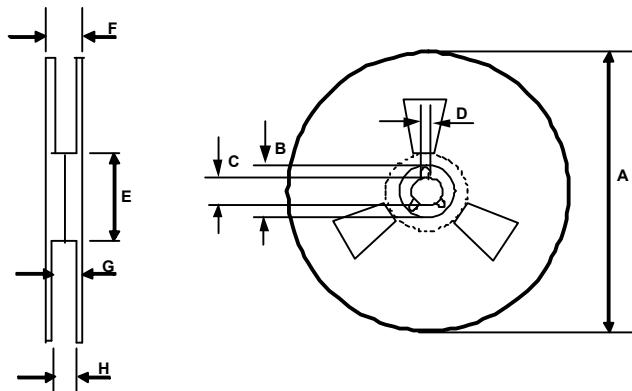
REEL DIMENSIONS FOR 16 SOIC W

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

IRS2112(-1,-2,S)PbF

LEADFREE PART MARKING INFORMATION

Part number — IRSxxxx

Date code — YWW?

IR logo — **IℛR**

Pin 1 Identifier — ●

?XXXX

Lot Code
(Prod mode - 4 digit SPN code)

?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Assembly site code
Per SCOP 200-002
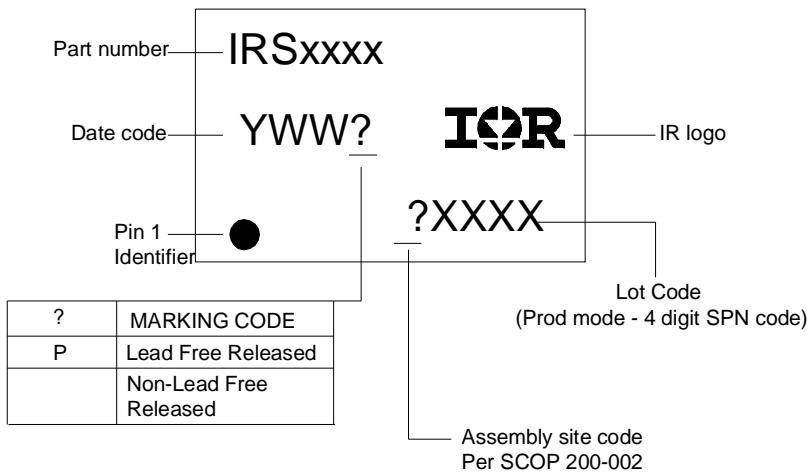
ORDER INFORMATION

14-Lead PDIP IRS2112PbF
14-Lead PDIP IRS2112-1PbF
16-Lead PDIP IRS2112-2PbF
16-Lead SOIC IRS2112SPbF
16-Lead SOIC Tape & Reel IRS2112STRPbF

International **IℛR** Rectifier

The SOIC-16 is MSL3 qualified.
This product has been designed and qualified for the industrial level.
Qualification standards can be found at www.irf.com
IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
Data and specifications subject to change without notice. 11/27/2006