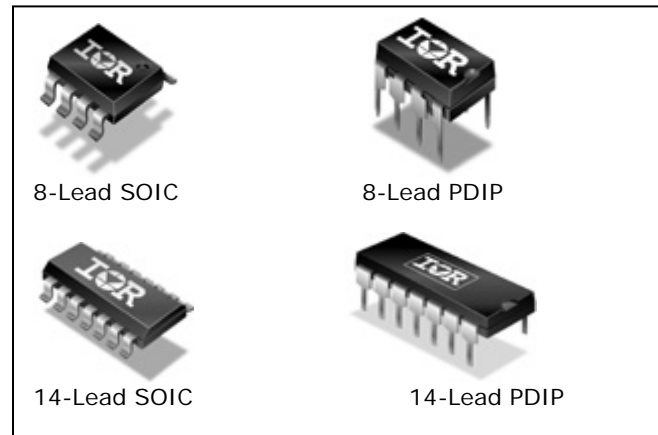


HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- Integrated bootstrap diode

Packages



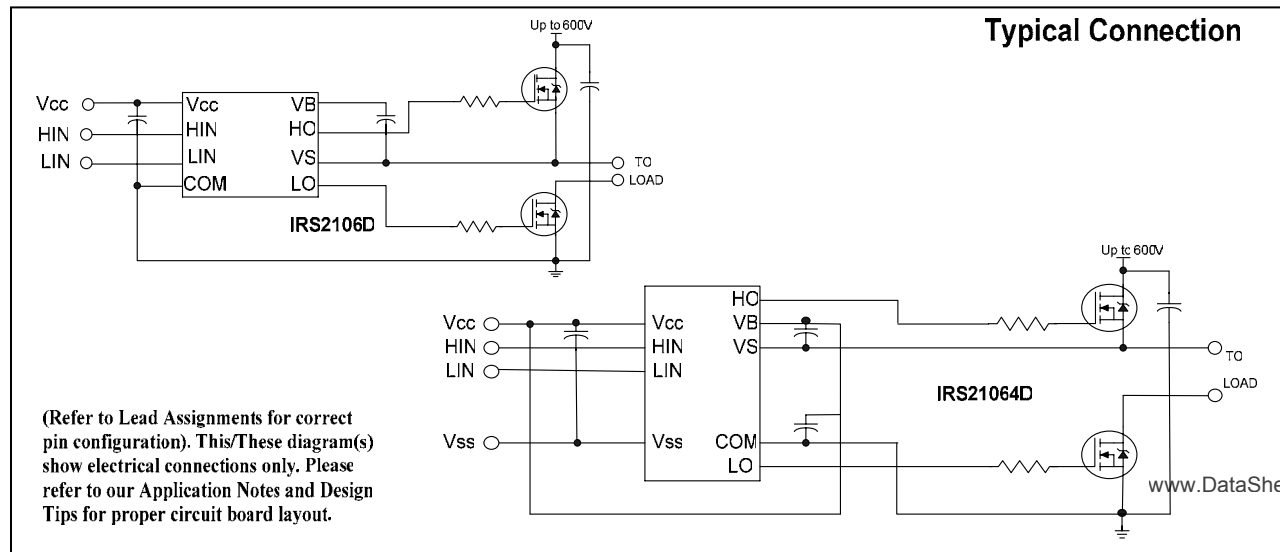
Description

The IRS2106(4)D(S) are high voltage, high speed power MOSFET an IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with Standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

IRS2106D/IRS2108D/IRS2109D/Feature Comparison

Part	Input Logic	Cross-Conduction Prevention logic	Dead-Time	Ground Pins	Ton/Toff
2106	HIN/LIN	no	none	COM	515/500
21064				VSS/COM	
2108	HIN/LIN	yes	Internal 540ns	COM	220/220
21084			Programmable 0.54- 5us	VSS/COM	
2109	IN/SD	yes	Internal 540ns	COM	750/220
21094			Programmable 0.54- 5us	VSS/COM	

Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted

Symbol	Definition	Min.	Max.	Units	
V_B	High side floating supply voltage	-0.3	620	V	
V_S	High side floating supply offset voltage	$V_B - 20$	$V_B + 0.3$		
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$		
V_{CC}	Low side and logic fixed supply voltage	-0.3	20		
V_{SS}	Logic ground (IRS21064D only)	$V_{CC} - 20$	$V_{CC} + 0.3$		
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$		
V_{IN}	Logic input voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns	
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.6	
R_{thJA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	$^\circ\text{C}/\text{W}$
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature	—	150	$^\circ\text{C}$	
T_S	Storage temperature	-50	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

and still air conditions.

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S & V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	V_{SS}	$V_{SS} + 5$	
V_{SS}	Logic ground (IRS21064D only)	-5	5	
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.
(Please refer to the Design Tip DT97 -3 for more details).

Note 2: HIN, LIN are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 \text{ pF}, T_A = 25^\circ C$

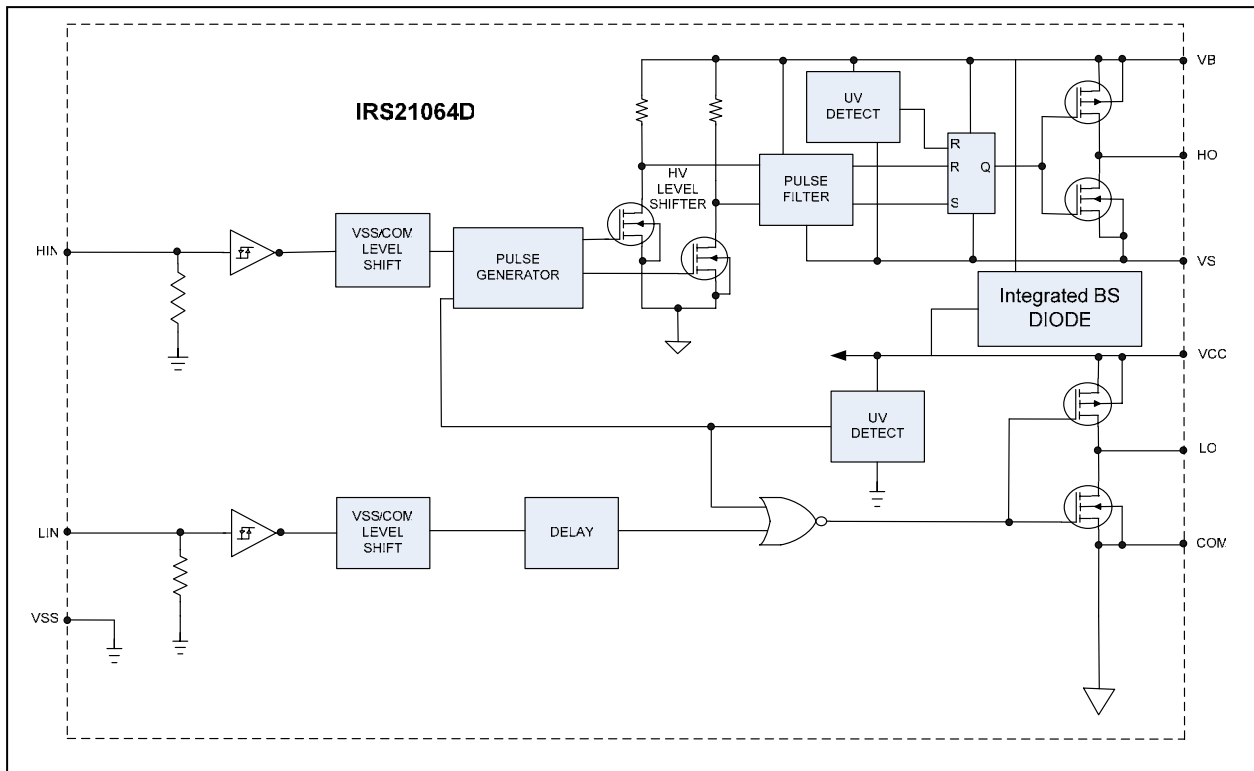
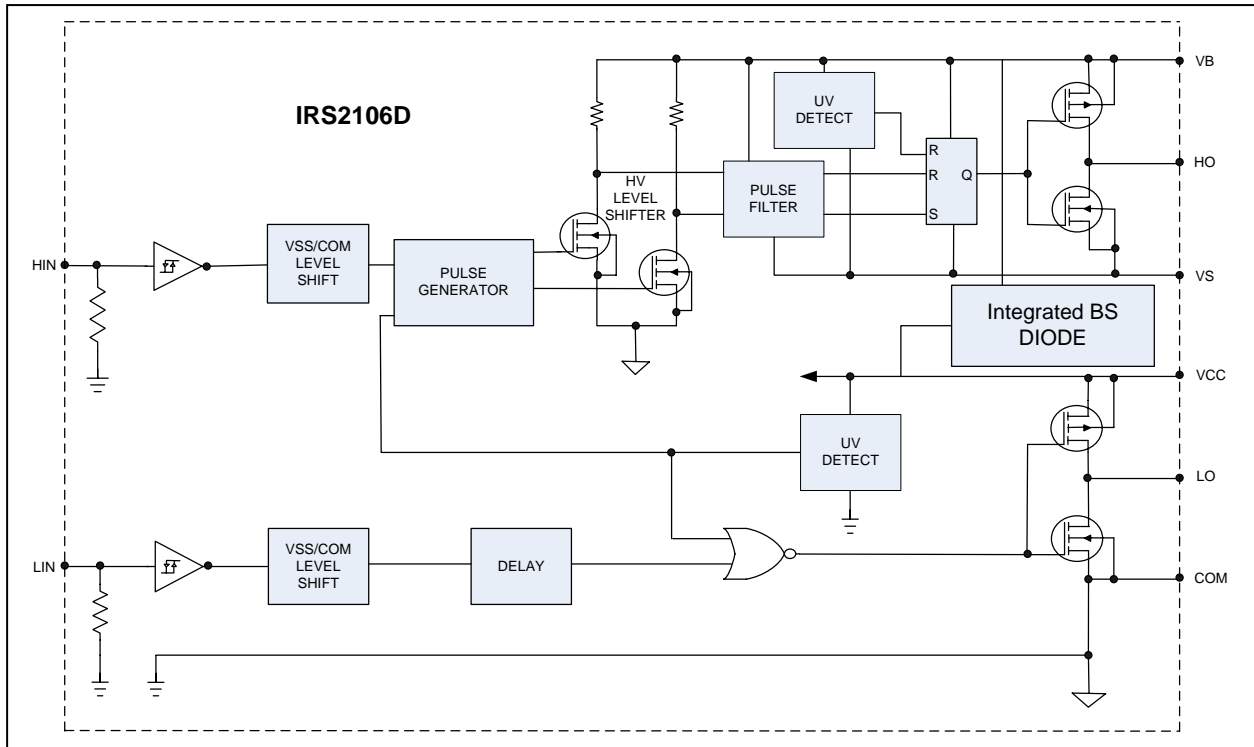
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	515	715	nsec	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	500	700		$V_S = 0V$ or $600V$
MT	Delay matching, HS & LS turn-on/off	—	—	30		
t_r	Turn-on rise time	—	150	220		$V_S = 0V$
t_f	Turn-off fall time	—	50	80		$V_S = 0V$
t_{fil}	Minimum pulse input filter time	—	300	—		

Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM$ and $T_A = 25^\circ C$ unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads. The V_O, I_O and R_{on} parameters are referenced to COM and are applicable to the respective output leads: HO and LO .

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{InTH+}	Positive input threshold voltage	—	—	2.2	V	$V_{CC} = 10V$ to $20V$
V_{InTH-}	Negative input threshold voltage	0.8	—	—		$V_{CC} = 10V$ to $20V$
V_{OH}	High level output voltage	—	0.8	1.4		$I_O = 20 \text{ mA}$
V_{OL}	Low level output voltage	—	0.3	0.6		$I_O = 20 \text{ mA}$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	—	45	70		$V_{IN} = 0V$ or $4V$
I_{QCC}	Quiescent V_{CC} supply current	500	1100	1700		$V_{IN} = 0V$ or $4V$
I_{IN+}	Logic "1" input bias current	—	5	20		$V_{IN} = 4V$
I_{IN-}	Logic "0" input bias current	—	—	2		$V_{IN} = 0V$
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going Threshold	8.0	8.9	9.8		V
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going Threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage Hysteresis	—	0.7	—		
I_{O+}	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V,$ $PW \leq 10 \text{ us}$
I_{O-}	Output low short circuit pulsed current	250	350	—		$V_O = 15V,$ $PW \leq 10 \text{ us}$
R_{bs}	Bootstrap resistance	—	200	—	Ohm	$V_{CC} = 15$

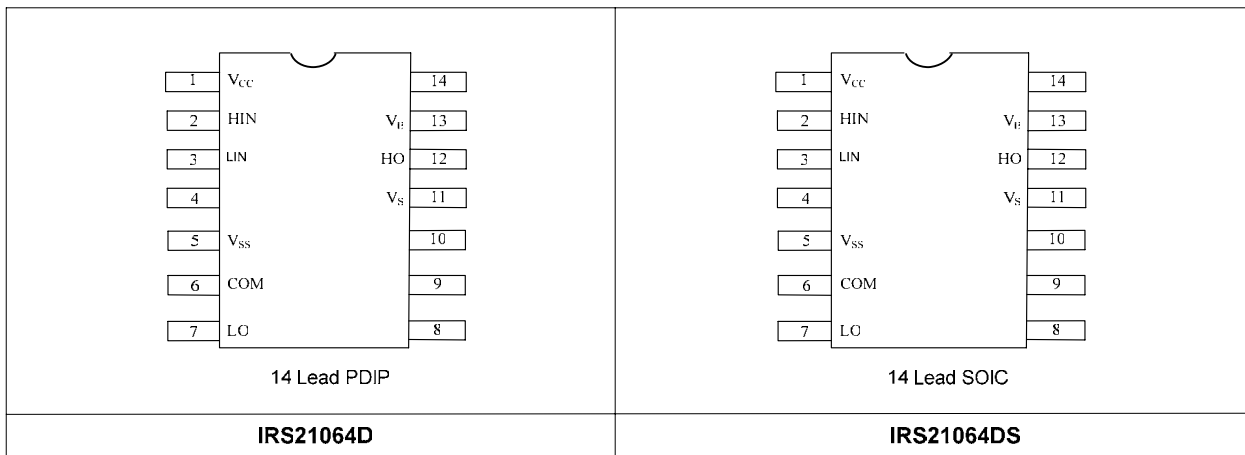
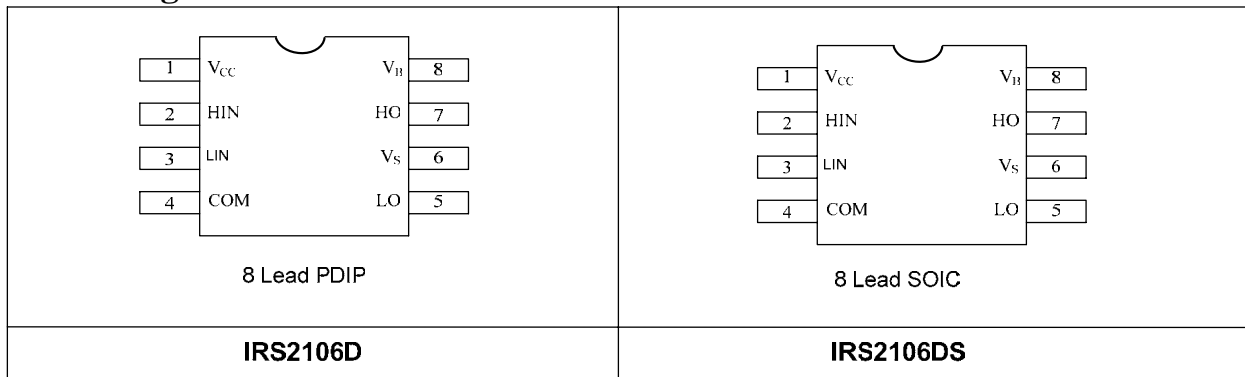
Functional Block Diagrams



Lead Definitions

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic Ground (IRS21064D only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



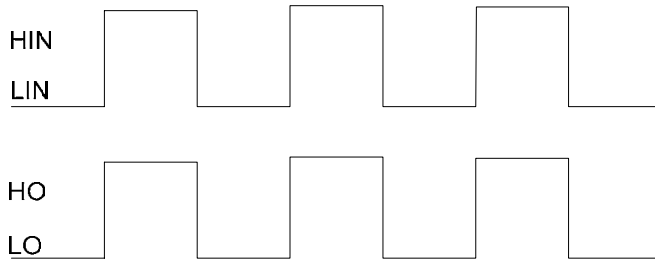


Figure 1. Input/Output Timing Diagram

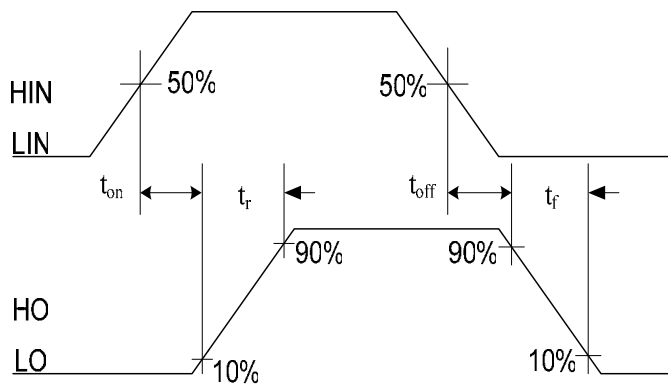


Figure 2. Switching Time Waveform Definitions

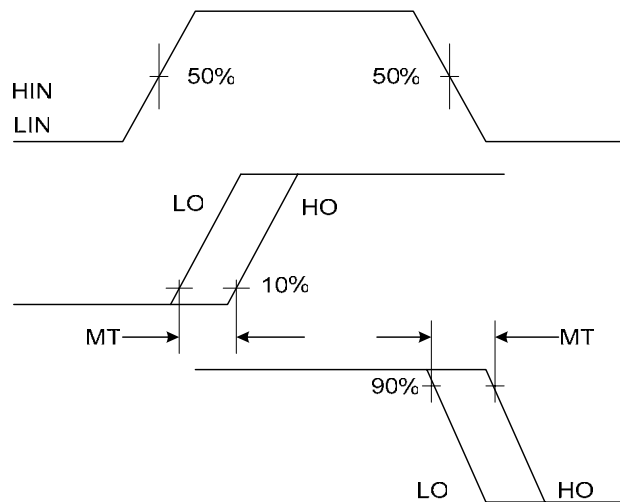


Figure 3. Delay Matching Waveform Definitions

Case Outlines

