IR3Y38M

CCD Signal Process & Digital Interface IC

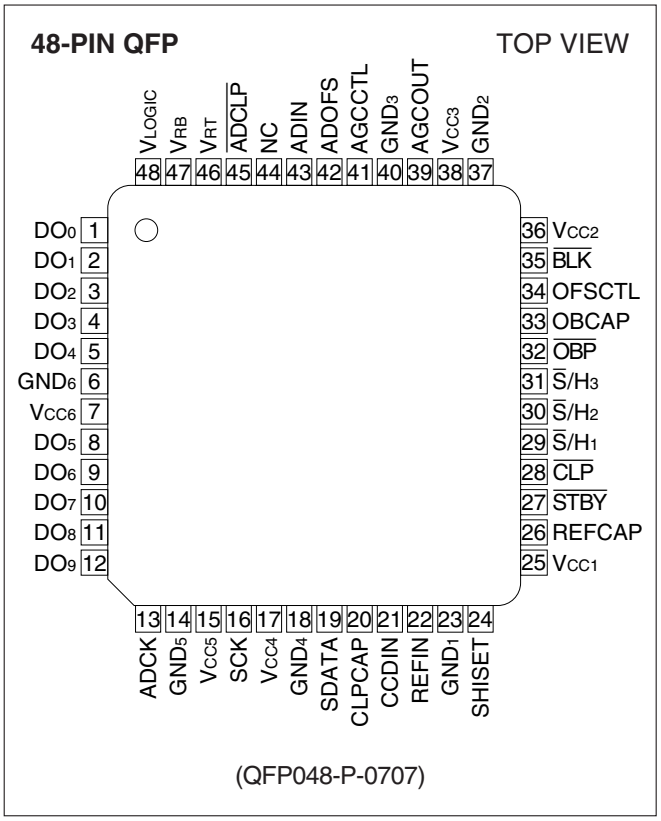
DESCRIPTION

The IR3Y38M is a bipolar single-chip signal processing IC for CCD area sensors which includes correlated double sampling circuit (CDS), clamp circuit, automatic gain control amplifier (AGC), reference voltage generator, black level detection circuit, 10-bit analog-to-digital converter (ADC), and serial interface for internal circuits.

FEATURES

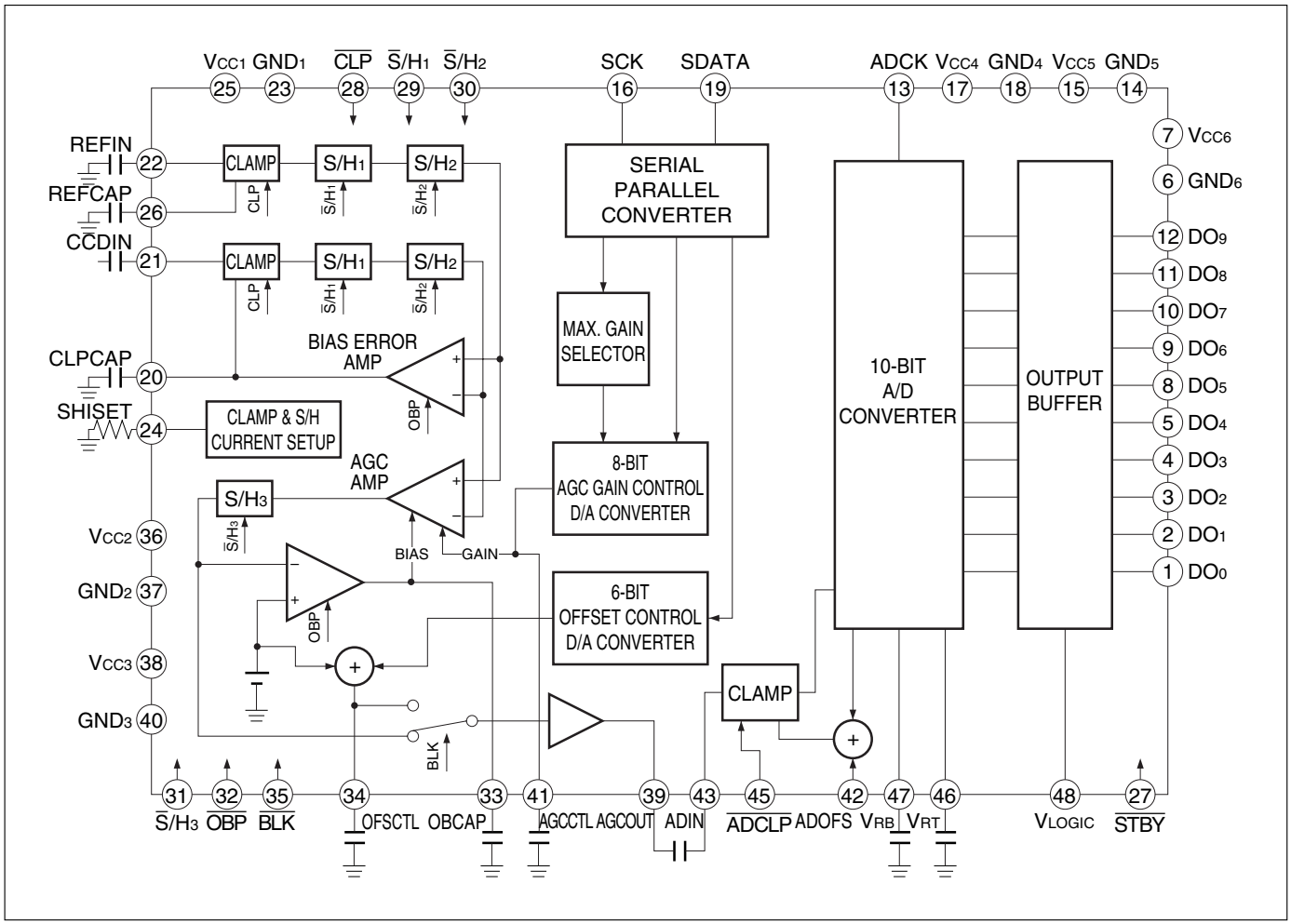
- Low power consumption : 315 mW (TYP.)
- Wide AGC range : 12 to 43.5 dB
- High speed sample-and-hold circuits : pulse width 12 ns (MIN.)
- Built-in standby mode for power saving applications
- Built-in serial interface to control the AGC gain, maximum gain and offset adjustment
- 10-bit ADC operating up to 18 MHz
- Digital interface for operating 3.3 V logic ICs
- Single +5 V power supply
- Package : 48-pin QFP (QFP048-P-0707) 0.5 mm pin-pitch

PIN CONNECTIONS



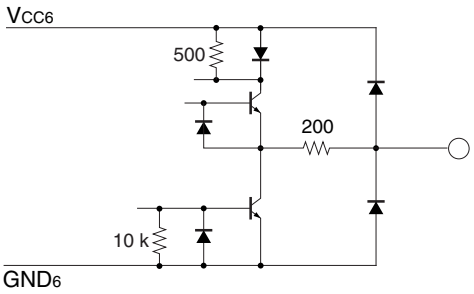
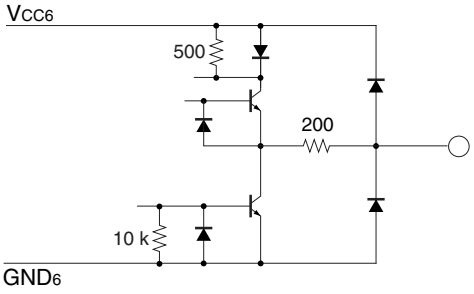
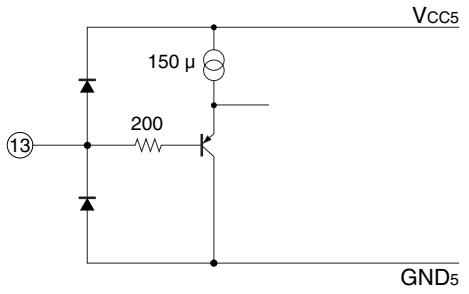
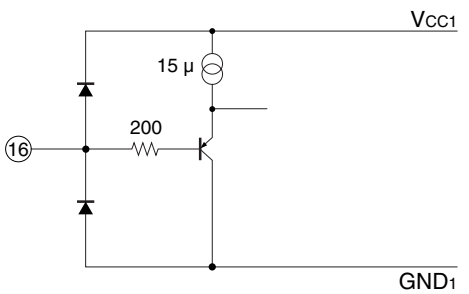
(QFP048-P-0707)

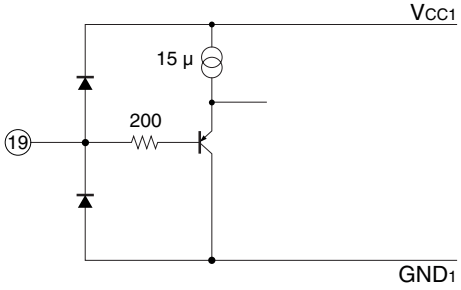
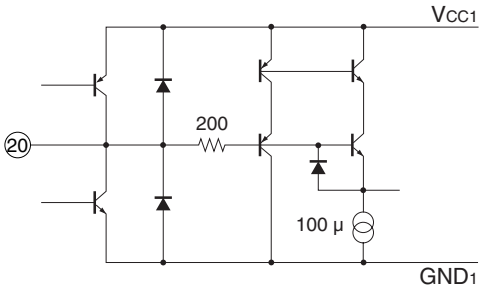
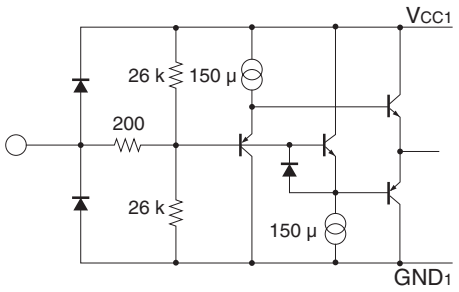
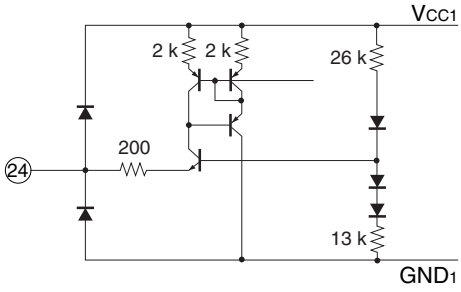
BLOCK DIAGRAM

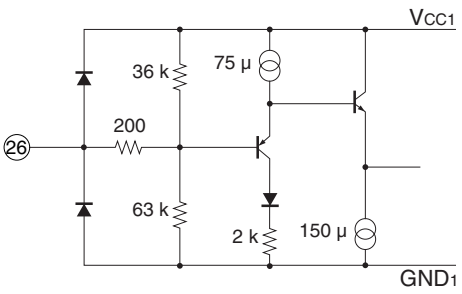
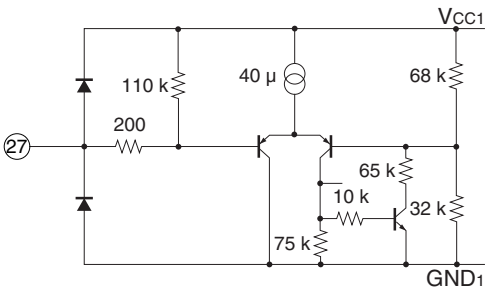
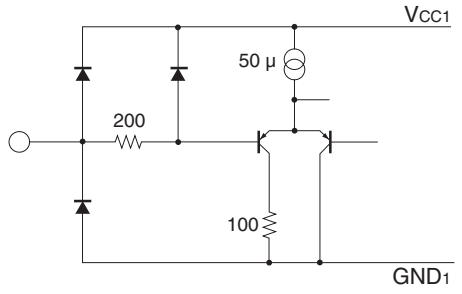
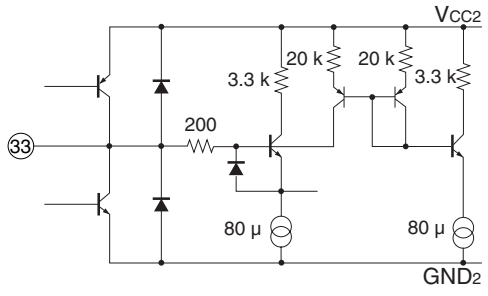


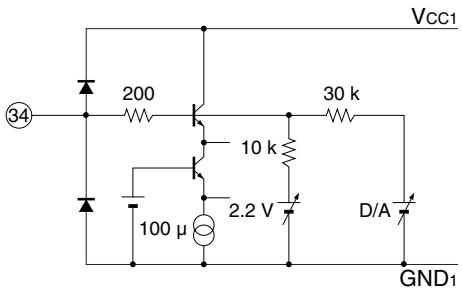
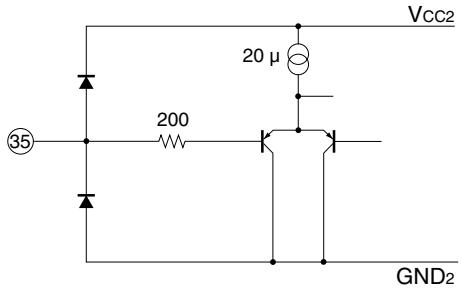
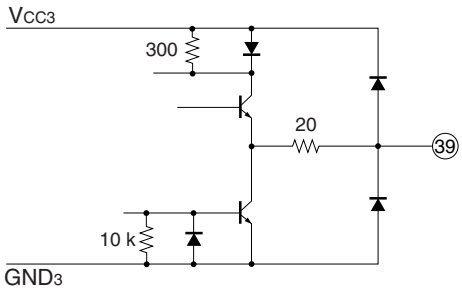
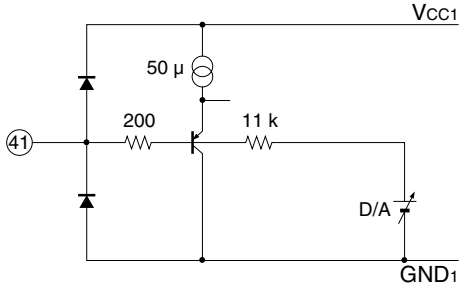
PIN DESCRIPTION

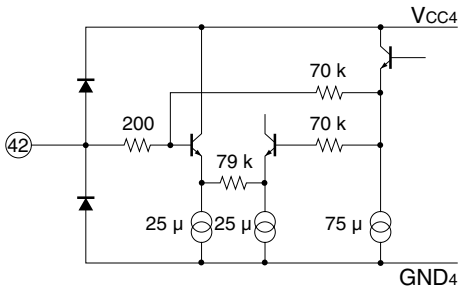
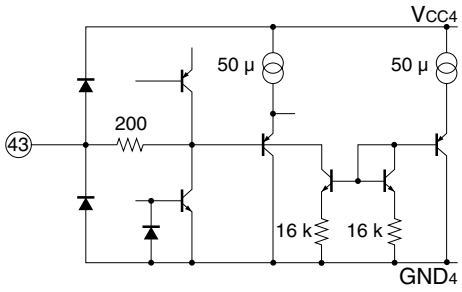
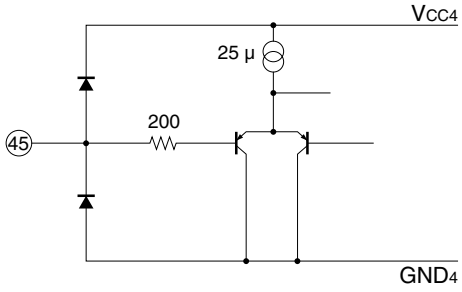
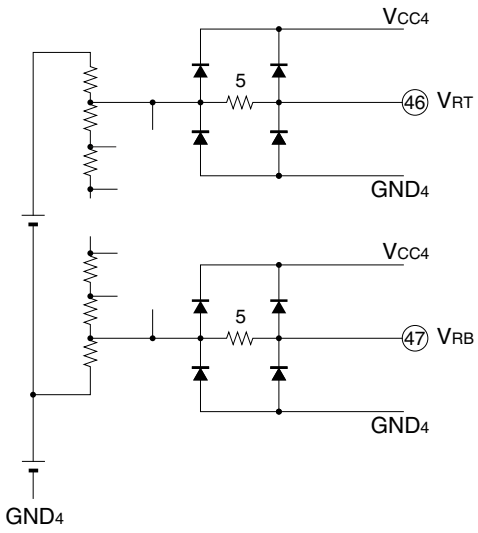
(The voltage is measured on condition that V_{CC1} to V_{CC6} = +5.0 V, V_{LOGIC} = +3.3 V.)

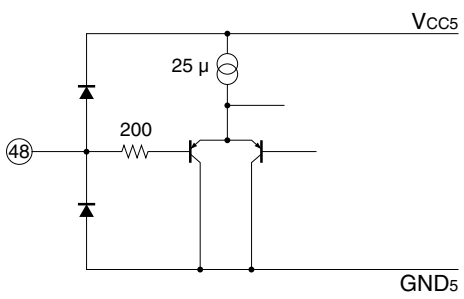
PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
1	DO_0	3.1 V / 0.2 V		Digital data output pins of the A/D converter. DO_0 is LSB. The data format is a straight binary code. V_{OL} : 0.2 V (TYP.) V_{OH} : V_{LOGIC} – 0.2 V (TYP.)
2	DO_1			
3	DO_2			
4	DO_3			
5	DO_4			
6	GND_6	0.0 V		GND pin of the output buffer of the A/D converter.
7	V_{CC6}	5.0 V		Power supply pin of the output buffer of the A/D converter.
8	DO_5	3.1 V / 0.2 V		Digital data output pins of the A/D converter. DO_9 is MSB. The data format is a straight binary code. V_{OL} : 0.2 V (TYP.) V_{OH} : V_{LOGIC} – 0.2 V (TYP.)
9	DO_6			
10	DO_7			
11	DO_8			
12	DO_9			
13	ADCK	> 2.1 V / < 0.7 V		Clock input pin of the A/D converter. The A/D conversion is executed at the rising edge of the ADCK, and the data is output at the falling edge of the ADCK. Duty : 50% fmax : 18 MHz (MIN.)
14	GND_5	0.0 V		Digital GND pin of the A/D converter.
15	V_{CC5}	5.0 V		Digital power supply pin of the A/D converter.
16	SCK	> 2.1 V / < 0.7 V		Clock input pin of the serial interface. Refer to **"TRUTH TABLE"** of pin 19.

<table>
<tr><th>PIN NO.</th><th>PIN NAME</th><th>VOLTAGE</th><th>EQUIVALENT CIRCUIT</th><th>DESCRIPTION</th></tr>
<tr><td>17</td><td>V_{CC4}</td><td>5.0 V</td><td></td><td>Analog power supply pin of the A/D converter.</td></tr>
<tr><td>18</td><td>GND_4</td><td>0.0 V</td><td></td><td>Analog GND pin of the A/D converter.</td></tr>
<tr><td>19</td><td>SDATA</td><td>> 2.1 V
< 0.7 V</td><td> 
</td><td>Data input pin of the serial interface.
TRUTH TABLE
<table>
<tr><th>SDATA</th><th>SCK</th><th>Action</th></tr>
<tr><td>DATA</td><td>↑</td><td>SHIFT</td></tr>
<tr><td>0</td><td>↓</td><td>–</td></tr>
<tr><td>1</td><td>↓</td><td>STORE</td></tr>
</table></td></tr>
<tr><td>20</td><td>CLPCAP</td><td>3.2 V</td><td> 
</td><td>Bias decoupling pin of the CDS signal clamp circuit. This pin is connected to the GND_1 via a capacitor.</td></tr>
<tr><td>21</td><td>CCDIN</td><td>2.5 V</td><td rowspan="2"> 
</td><td>Signal input pin of the CDS.
Input CCD signal to this pin via a capacitor.</td></tr>
<tr><td>22</td><td>REFIN</td><td>2.5 V</td><td>Reference input pin of the CDS.
This pin is connected to the GND_1 via a capacitor.</td></tr>
<tr><td>23</td><td>GND_1</td><td>0.0 V</td><td></td><td>GND pin of the CDS/AGC.
Pay careful attention to board layout of the GND_1 because the CDS/AGC are noise-sensitive circuitry.</td></tr>
<tr><td>24</td><td>SHISET</td><td>1.7 V</td><td> 
</td><td>Operation current setting pin of the CDS and $\overline{S}$/H_3 circuits.
This pin is connected to the GND_1 via a resistor.
The slew rates of the $\overline{S}$/Hs are in inverse proportion to the value of the resistor.</td></tr>
</table>

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
25	V_{CC1}	5.0 V		Power supply pin of the CDS/AGC.
26	REFCAP	3.2 V		Bias decoupling pin of the CDS reference clamp circuit. This pin is connected to the GND_1 via a capacitor.
27	$\overline{STBY}$	5.0 V (open) > 2.1 V < 0.7 V		Standby function control pin. All actions stop and the power consumption is decreased when low. The threshold voltage has 0.4 V hysteresis. Connect to the Vcc if not used.
28	$\overline{CLP}$	> 2.1 V < 0.7 V		Pulse input pin of the CDS feed-through level clamp. Signal is clamped when low.
29	$\overline{S}/H_1$			Pulse input pin of the $\overline{S}/H_1$. Signal is sampled when low.
30	$\overline{S}/H_2$			Pulse input pin of the $\overline{S}/H_2$. Signal is sampled when low.
31	$\overline{S}H_3$			Pulse input pin of the $\overline{S}/H_3$. Signal is sampled when low.
32	$\overline{OBP}$			Pulse input pin of the OPB clamp and bias error amplifier. Signal is clamped when low.
33	OBCAP	3.7 V		Clamp capacitor pin of the optical black clamp (OPB clamp) circuit. Connect to the GND_2 via a capacitor.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
34	OFSCTL	2.15 to 2.30 V		Decoupling capacitor pin of the blanking offset control D/A converter. Connect to the GND1 via a capacitor.
35	$\overline{BLK}$	> 2.1 V < 0.7 V		Blanking pulse input pin. The output of the AGCOUT pin is blanked when low. The blanking level can be controlled by the serial interface.
36	VCC2	5.0 V		Power supply pin of the $\overline{S}$/H3 and OPB clamp circuits.
37	GND2	0.0 V		GND pin of the $\overline{S}$/H3 and OPB clamp circuits.
38	VCC3	5.0 V		Power supply pin of the output buffer circuit connected to the AGCOUT pin.
39	AGCOUT	0.9 V ($\overline{OBP}$ = L)		Signal output pin of the AGC. Connect to the ADIN pin via a capacitor.
40	GND3	0.0 V		GND pin of the output buffer circuit connected to the AGCOUT pin.
41	AGCCTL	2.5 to 3.8 V		Decoupling capacitor pin of the AGC gain control D/A converter. Connect to the GND1 via a capacitor.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
42	ADOFS	3.3 V (open) Input range 1.6 to 5.0 V		Voltage adjustment pin of the ADC black level clamp. This pin is biased at 3.3 V from the inside of the IC. Connect to the GND4 via a capacitor if not used.
43	ADIN	1.4 V ($\overline{ADCLP}$ = L)		Signal input pin of the ADC. Connect to the AGCOUT pin via a capacitor. This capacitor is also used as the clamp capacitor of the ADC blank level clamp.
44	NC			No connection. It is recommended to connect to GND for better heat radiation and avoiding noise.
45	$\overline{ADCLP}$	> 2.1 V < 0.7 V		Pulse input pin of the ADC black level clamp. Signal is clamped when low. When the ADOFS is opened, the clamped level is set to make the ADC output 61 (decimal).
46	VRT	3.90 V		Upper reference decoupling pin of the ADC. Connect to the GND4 via a capacitor.
47	VRB	1.95 V		Lower reference decoupling pin of the ADC. Connect to the GND4 via a capacitor.

PIN NO.	PIN NAME	VOLTAGE	EQUIVALENT CIRCUIT	DESCRIPTION
48	V_{LOGIC}	3.3 V		ADC output voltage setting pin. The high level voltage of the DO_0 to DO_9 pins is set to V_{LOGIC} – 0.2 V. It is recommended to connect to the power supply of the following logic ICs.

FUNCTIONAL DESCRIPTION

CDS Circuit

The clamp circuit clamps the feed-through level of the CCD signal with the $\overline{CLP}$ pulse. Then the $\overline{S}/H_1$ circuit samples the signal period of the one with the $\overline{S}/H_1$ pulse and holds on. Thus the video signal is obtained. But this signal has a level drop caused by the reset pulse of the CCD signal, and for removing it, the $\overline{S}/H_2$ circuit samples this signal again with the $\overline{S}/H_2$ pulse.

For reducing the effect of the sampling pulse or other noise sources, the CDS circuit is formed with a differential structure.

Bias Error Amplifier Circuit

For stabilizing the bias level of the CDS circuit and reducing the offset of the AGC circuit, the bias error amplifier acts with the $\overline{OBP}$ pulse during the OPB period.

AGC Amplifier Circuit

The AGC amplifier amplifies the video signal obtained by the CDS circuit. The gain of the AGC is controlled by the value of the AGCGAIN serial register. And the maximum gain of the AGC is controlled by the value of the GAINSEL serial register.

OPB Clamp Circuit

For clamping the level of the amplified signal to the black level, the OPB clamp circuit acts with the $\overline{OBP}$ pulse during the OPB period.

Blanking Circuit

The output signal is fixed to the blanking level with the $\overline{BLK}$ pulse. The blanking level is the sum of the black level and the offset value decided by the value of the OFFSET serial register.

A/D Converter Circuit

The $\overline{S}/H_3$ circuit samples the amplified signal with the $\overline{S}/H_3$ pulse and the A/D converter converts the sampled signal to 10-bit straight binary digital data.

The clamp circuit placed in front of the A/D converter clamps the signal level beside the lower limit of the convertible input range with the $\overline{ADCLP}$ pulse. The clamped level is controllable by the voltage of the ADOFS pin.

The A/D conversion is executed at the rising edge of the ADCK clock, and the data is output at the falling edge.

The high level voltage of the outputs is controlled by the voltage of the V_{LOGIC} pin.

Standby Function

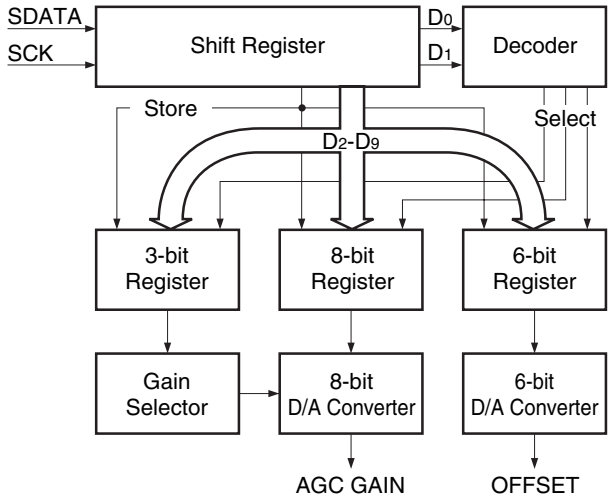
By making the $\overline{STBY}$ pin low, all actions of this IC stop and power consumption is decreased.

The outputs of the A/D converter (DO_0 to DO_9) turn to high impedance when on standby.

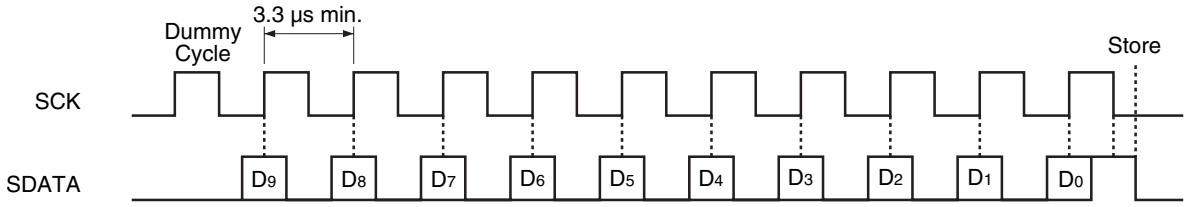
Serial Interface Circuit

The IR3Y38M has a serial interface to control the gain of the AGC amplifier and the offset of the blanking level. This interface is constituted by a shift register for serial-parallel conversion, data registers and D/A converters.

The data input to SDATA is fetched and shifted at the rising edge of the SCK. While transmitting data, the SDATA must be low when the SCK falls. When the SDATA is high and the SCK falls, the data on the shift register is stored at the selected data register at the following falling edge of the SDATA. The stored data register is selected by the data of the D_0 and D_1 bits.

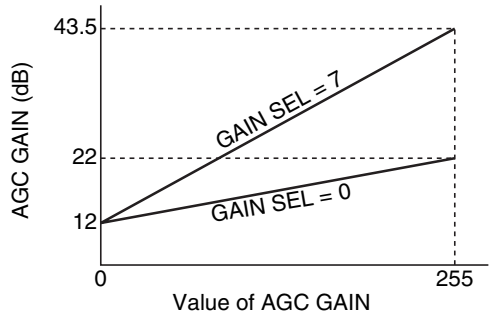


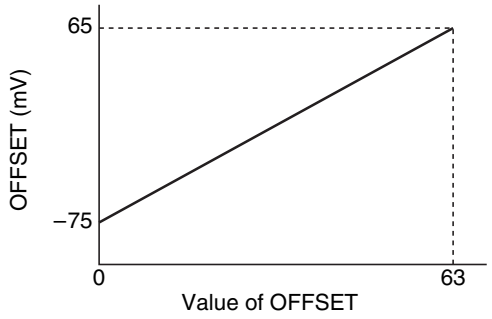
GAIN SEL	MAXIMUM GAIN (dB)
0	22
1	25
2	28
3	31.5
4	34.5
5	38
6	41
7	43.5



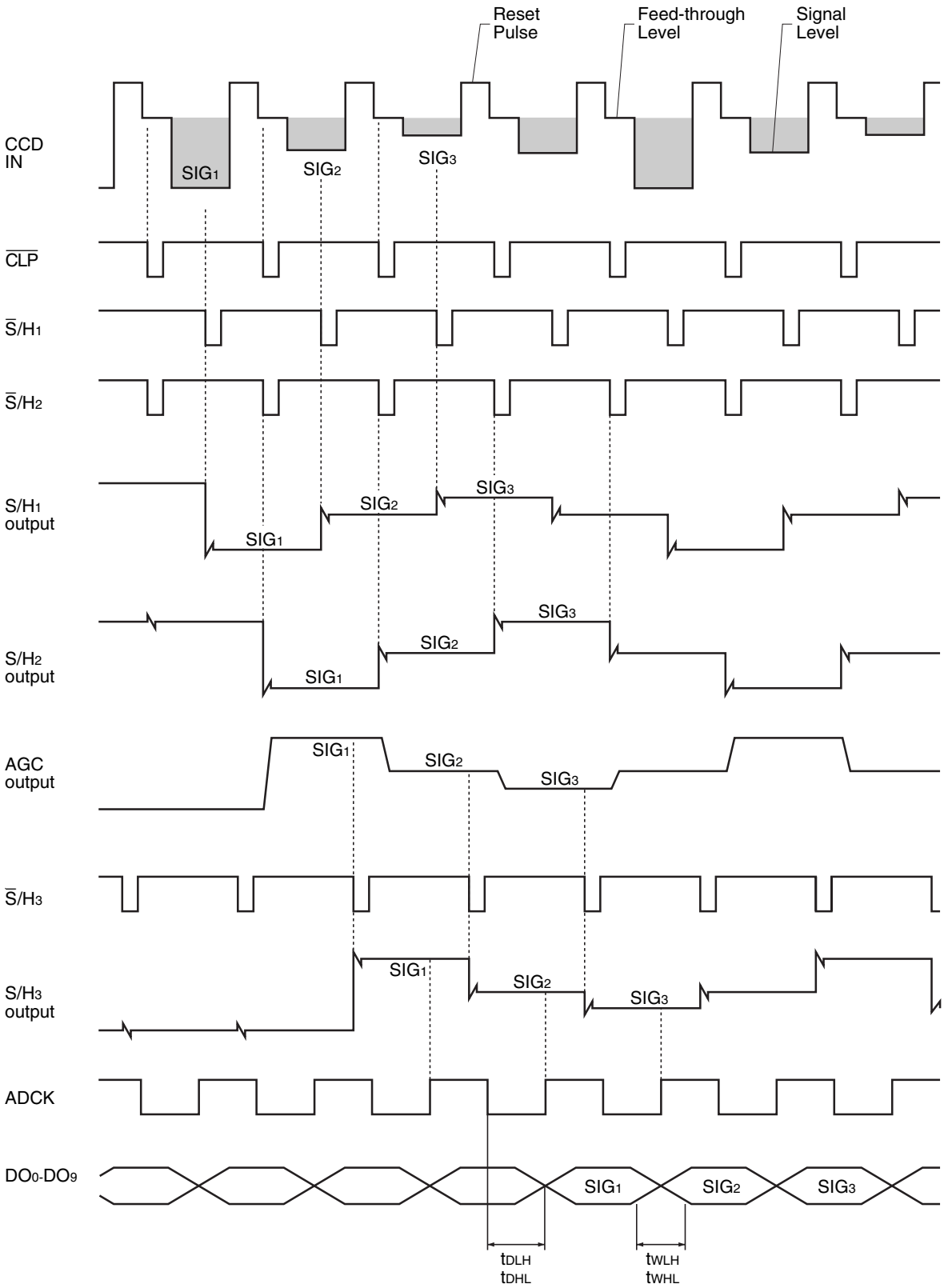
DATA REGISTER	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GAIN SEL						d0	d1	d2	0	0
AGC GAIN	d0	d1	d2	d3	d4	d5	d6	d7	0	1
OFFSET			d0	d1	d2	d3	d4	d5	1	0
(Don't care)									1	1

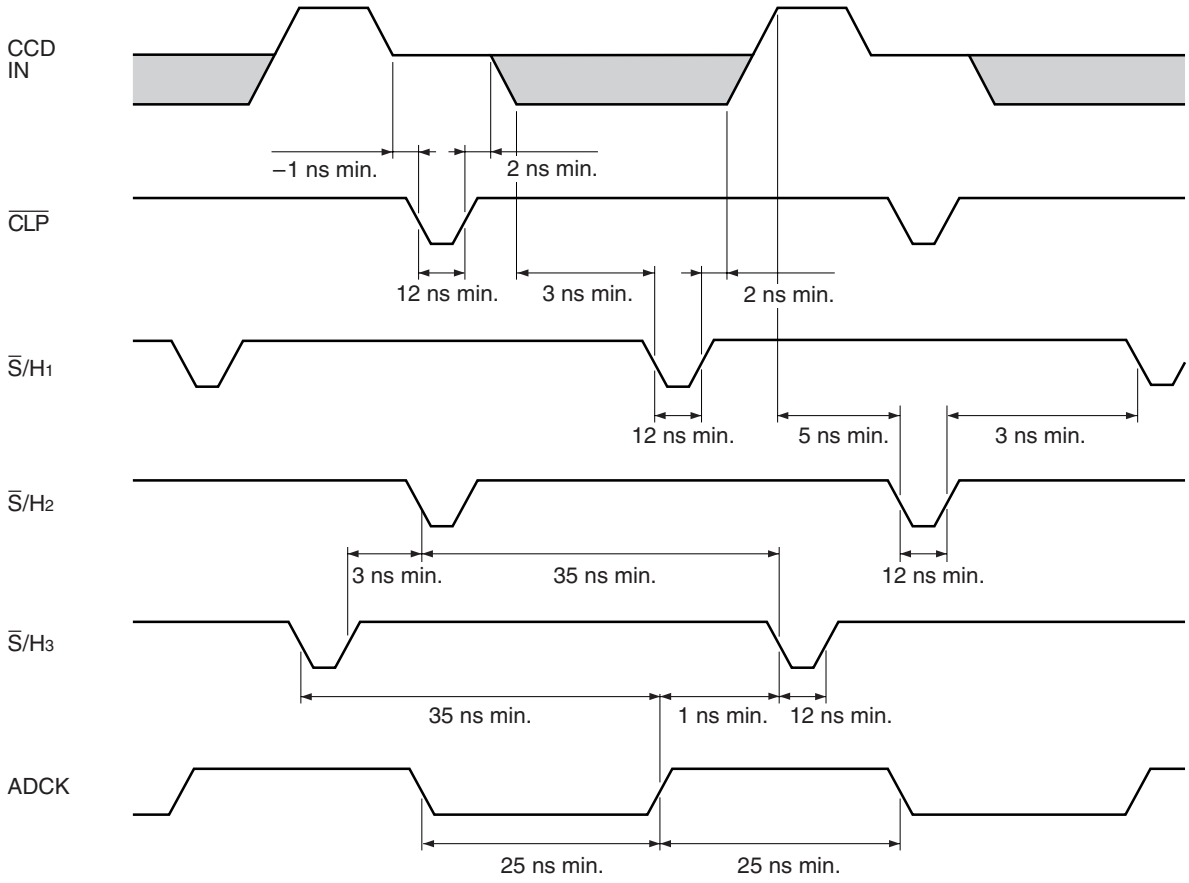
LSB MSB

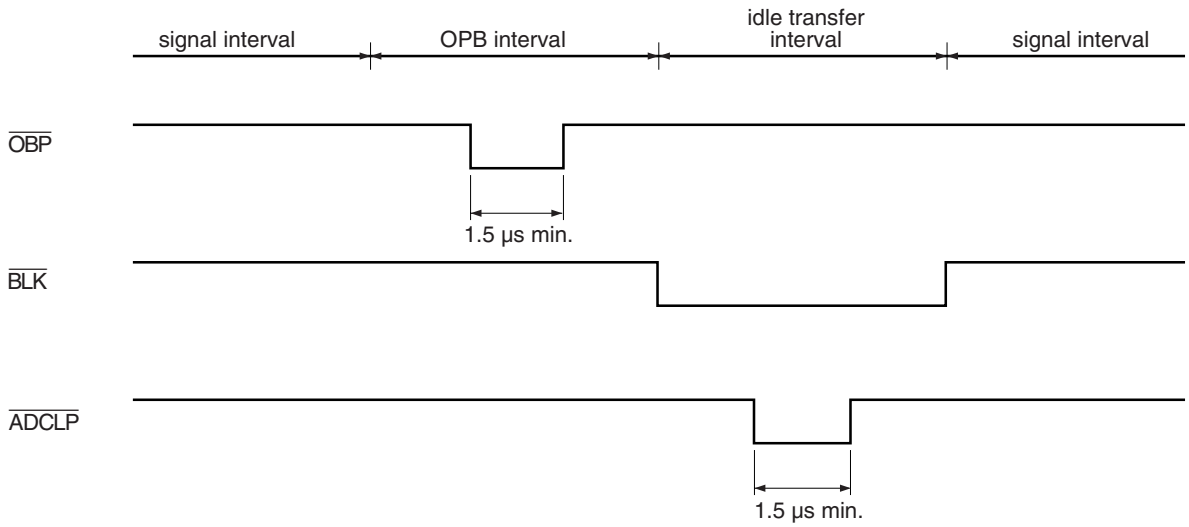




TIMING CHART







PRECAUTIONS

Each V_{CC1} to V_{CC6} pin corresponds to the each GND_1 to GND_6 pin. Connect a ceramic capacitor as near the IC as possible between each corresponding V_{CC} pin and GND pin.

The GND_1 pin is the ground of the CDS/ADC circuit handling a weak signal. Pay careful attention to the board layout of the GND_1 pattern in order to avoid the potential fluctuation of the GND_1 caused by the current of the other GND pins. Especially pay attention to the current of the GND_6 pin's flowing spiky current.

All the GND pins must be at the same potential and not open. And keep the potential difference of each V_{CC} pin within 0.3 V.

The high level voltage of the outputs of the A/D converter is controllable by the voltage of the V_{LOGIC} pin, but take care that the high level voltage does not fall below about 1.5 V, in spite of making the V_{LOGIC} pin 0 V. This may cause the latch up of the following logic ICs if the power supply of this IC rises up faster than the power supply of the following logic. To avoid this problem, it is recommended to make the $\overline{STBY}$ pin low until the voltage of the logic power supply becomes stable. Take care too that the high level voltage does not rise above about V_{CC} – 1.0 V, in spite of making the V_{LOGIC} pin the V_{CC} potential.

Restore the value of the serial register when setting up the power supply or making the $\overline{STBY}$ pin high because the value will have been removed in that case.

ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, T_A = +25 ˚C)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply voltage	V_{CC1}-V_{CC6}		7	V
Input voltage	V_{IN}		–0.3 to V_{CC} + 0.3	V
Power consumption	P_D	$T_A \leq$ +25 ˚C	570	mW
P_D derating ratio		$T_A >$ +25 ˚C	4.5	mW/˚C
Operating temperature	T_{OPR}		–30 to +70	˚C
Storage temperature	T_{STG}		–55 to +150	˚C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT
Supply voltage	V_{CC1}-V_{CC6}		4.75 to 5.25	V
Standard CCD input signal level	V_{CCD}	CCDIN	200	mVp-p
Input "Low" voltage	V_{IL}	$\overline{ADCK}$, SCK, SDATA, $\overline{STBY}$, $\overline{CLP}$, $\overline{S}/H_1$, $\overline{S}/H_2$, $\overline{S}/H_3$, $\overline{OBP}$, $\overline{BLK}$, $\overline{ADCLP}$	0 to 0.7	V
Input "High" voltage	V_{IH}		2.1 to V_{CC}	V
S/H pulse width	$t_{WS/H}$	$\overline{CLP}$, $\overline{S}/H_1$, $\overline{S}/H_2$, $\overline{S}/H_3$	≥ 12	ns
Clamp pulse width	t_{WC}	$\overline{OBP}$, $\overline{ADCLP}$	≥ 1.5	µs
A/D converter clock frequency	f_{ADCK}	ADCK	≤ 18	MHz
Serial interface clock frequency	f_{SCK}	SCK	≤ 300	kHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Unless otherwise specified, T_A = +25 ˚C, V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = V_{CC5} = V_{CC6} = 5.0 V, V_{LOGIC} = 3.3 V, ADCK = 0 V, SCK = 0 V, SDATA = 0 V, $\overline{STBY}$ = 3.3 V, $\overline{CLP}$ = 0 V, $\overline{S}/H_1$ = 0 V, $\overline{S}/H_2$ = 0 V, $\overline{S}/H_3$ = 0 V, $\overline{BLK}$ = 3.3 V, $\overline{OBP}$ = 0 V, SW42 = OFF, SW43 = (a), $\overline{ADCLP}$ = 3.3 V)
The current direction flowing into the pin is positive direction.

• General

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply current (1)	I_{CC1}	Measure pin 25 (V_{CC1})	–	27	34	mA
Supply current (2)	I_{CC2}	Measure pin 36 (V_{CC2}).	–	2.3	2.8	mA
Supply current (3)	I_{CC3}	Measure pin 38 (V_{CC3}).	–	0.7	1.0	mA
Supply current (4)	I_{CC4}	Measure pin 17 (V_{CC4}).	–	13	20	mA
Supply current (5)	I_{CC5}	Measure pin 15 (V_{CC5}).	–	16	21	mA
Supply current (6)	I_{CC6}	Measure pin 7 (V_{CC6}).	–	5.0	6.5	mA
Total supply current	I_{CC}	Total of I_{CC1} to I_{CC6}	–	63	77	mA
Standby supply current	I_{STBY}	$\overline{STBY}$ = 0 V, Total of I_{CC1} to I_{CC6}.	–	4.5	6.5	mA
Input "Low" current (1)	I_{IL1}	Apply to pin 28 ($\overline{CLP}$), pin 29 ($\overline{S}/H_1$), pin 30 ($\overline{S}/H_2$), pin 31 ($\overline{S}/H_3$), and pin 32 ($\overline{OBP}$). V_{IL} = 0 V	–3.5	–2.0	–	µA
Input "High" current (1)	I_{IH1}	Apply to pin 28 ($\overline{CLP}$), pin 29 ($\overline{S}/H_1$), pin 30 ($\overline{S}/H_2$), pin 31 ($\overline{S}/H_3$), and pin 32 ($\overline{OBP}$). V_{IH} = 3.3 V	–	0	0.1	µA
Input "Low" current (2)	I_{IL2}	Apply to pin 16 (SCK) and pin 19 (SDATA). V_{IL} = 0 V	–0.3	–0.2	–	µA
Input "High" current (2)	I_{IH2}	Apply to pin 16 (SCK) and pin 19 (SDATA). V_{IH} = 3.3 V	–	0	0.1	µA
Input "Low" current (3)	I_{IL3}	Apply to pin 35 ($\overline{BLK}$) and pin 45 ($\overline{ADCLP}$). V_{IL} = 0 V	–0.5	–0.3	0	µA
Input "High" current (3)	I_{IH3}	Apply to pin 35 ($\overline{BLK}$) and pin 45 ($\overline{ADCLP}$). V_{IH} = 3.3 V	–	0	0.1	µA
Input "Low" current (4)	I_{IL4}	Apply to pin 13 (ADCK). V_{IL} = 0 V	–3.5	–2.0	–	µA
Input "High" current (4)	I_{IH4}	Apply to pin 13 (ADCK). V_{IH} = 3.3 V	–	0	0.1	µA
$\overline{STBY}$ voltage	V_{27}	Open pin 27 ($\overline{STBY}$).	4.5	5.0	–	V
$\overline{STBY}$ impedance	Z_{27}		70	110	140	kΩ

• **CDS & AGC Circuits**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLPCAP voltage	V_{20}		2.9	3.2	3.6	V
CCDIN voltage	V_{21}		2.3	2.5	2.8	V
REFIN voltage	V_{22}		2.3	2.5	2.8	V
SHISET voltage	V_{24}		1.5	1.7	1.9	V
REFCAP voltage	V_{26}		2.9	3.2	3.6	V
OBCAP voltage	V_{33}		3.3	3.7	4.0	V
AGCOUT voltage	V_{39}		0.7	0.9	1.1	V
CCDIN impedance	Z_{21}		9	13	18	kΩ
REFIN impedance	Z_{22}		9	13	18	kΩ
REFCAP impedance	Z_{26}		15	23	32	kΩ
OFSCTL impedance	Z_{34}		6	9	12	kΩ
AGCCTL impedance	Z_{41}		7	11	15	kΩ
CLPCAP charge current	I_{L20}	CLPCAP = 2.8 V, OBP = 0 V Measure the current of CLPCAP.	–	−135	−110	µA
CLPCAP discharge current	I_{H20}	CLPCAP = 3.6 V, OBP = 0 V Measure the current of CLPCAP.	110	135	–	µA
CLPCAP leakage current	I_{Z20}	CLPCAP = 3.2 V, OBP = 3.3 V Measure the current of CLPCAP.	−0.5	0	0.5	µA
OBCAP charge current	I_{L33}	OBCAP = 3.3 V, OBP = 0 V Measure the current of OBCAP.	–	−90	−65	µA
OBCAP discharge current	I_{H33}	OBCAP = 4.1 V, OBP = 0 V Measure the current of OBCAP.	65	90	–	µA
OBCAP leakage current	I_{Z33}	OBCAP = 3.7 V, OBP = 3.3 V Measure the current of OBCAP.	−0.5	0	0.5	µA

• **A/D Converter Circuit**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADOFS voltage	V_{42}		3.0	3.3	3.6	V
ADIN voltage	V_{43}	ADCLP = 0 V	1.2	1.4	1.6	V
V_{RT} voltage	V_{46}		3.7	3.9	4.1	V
V_{RB} voltage	V_{47}		1.8	1.95	2.2	V
ADOFS impedance	Z_{42}		50	70	90	kΩ
ADIN charge current	I_{L43}	ADIN = 1.0 V, ADCLP = 0 V Measure the current of ADIN.	–	–45	–30	µA
ADIN discharge current	I_{H43}	ADIN = 1.8 V, ADCLP = 0 V Measure the current of ADIN.	30	45	–	µA
ADIN leakage current	I_{Z43}	ADIN = 1.4 V, ADCLP = 3.3 V Measure the current of ADIN.	–0.3	0	0.3	µA
Output "Low" voltage	V_{OL}	SW43 = (b), ADCIN = 0.8 V Change the level of ADCK to L→H→L, then measure the voltages of DO_0 to DO_9 pins.	–	0.2	0.4	V
Output "High" voltage	V_{OH}	SW43 = (b), ADCIN = 3.5 V Change the level of ADCK to L→H→L, then measure the voltages of DO_0 to DO_9 pins.	2.9	3.1	–	V

AC Characteristics

(Unless otherwise specified, T_A = +25 °C, V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = V_{CC5} = V_{CC6} = 5.0 V, V_{LOGIC} = 3.3 V, ADCK = 0 V, SCK = 0 V, SDATA = 0 V, $\overline{STBY}$ = 3.3 V, $\overline{CLP}$ = 3.3 V, $\overline{S}/H_1$ = 0 V, $\overline{S}/H_2$ = 0 V, $\overline{S}/H_3$ = 0 V, $\overline{BLK}$ = 3.3 V, $\overline{OBP}$ = 3.3 V, SW42 = OFF, SW43 = (a), $\overline{ADCLP}$ = 3.3 V, (OFFSET) = 32)
The value of the serial register is written with decimal.

• CDS & AGC Circuits

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC minimum gain	G_{AN}	(GAIN SEL) = 0, (AGC GAIN) = 0 $\overline{CLP}$ = SG2, $\overline{OBP}$ = SG3 Input the attenuated SG1 (f = 2 MHz, V = 1.6 Vp-p) to the SIN and seek the attenuation amount to make the amplitude of AGCOUT 1.6 Vp-p.	11	12	13	dB
AGC maximum gain (0)	G_{AX0}	(GAIN SEL) = 0, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of G_{AN}.	20.5	22	24.5	dB
AGC maximum gain (1)	G_{AX1}	(GAIN SEL) = 1, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of G_{AN}.	23	25	28	dB
AGC maximum gain (2)	G_{AX2}	(GAIN SEL) = 2, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of G_{AN}.	26	28	31	dB
AGC maximum gain (3)	G_{AX3}	(GAIN SEL) = 3, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of G_{AN}.	28.5	31.5	35	dB
AGC maximum gain (4)	G_{AX4}	(GAIN SEL) = 4, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of G_{AN}.	31	34.5	38	dB
AGC maximum gain (5)	G_{AX5}	(GAIN SEL) = 5, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of G_{AN}.	34	38	42	dB
AGC maximum gain (6)	G_{AX6}	(GAIN SEL) = 6, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of G_{AN}.	36.5	41	44.5	dB
AGC maximum gain (7)	G_{AX7}	(GAIN SEL) = 7, (AGC GAIN) = 255 Measure the gain using the same procedure as for the measurement of G_{AN}.	38.5	43.5	47.5	dB
AGC gain variable width	G_{AR}	$G_{AR} = G_{AX7} - G_{AN}$	26.5	31.5	35.5	dB

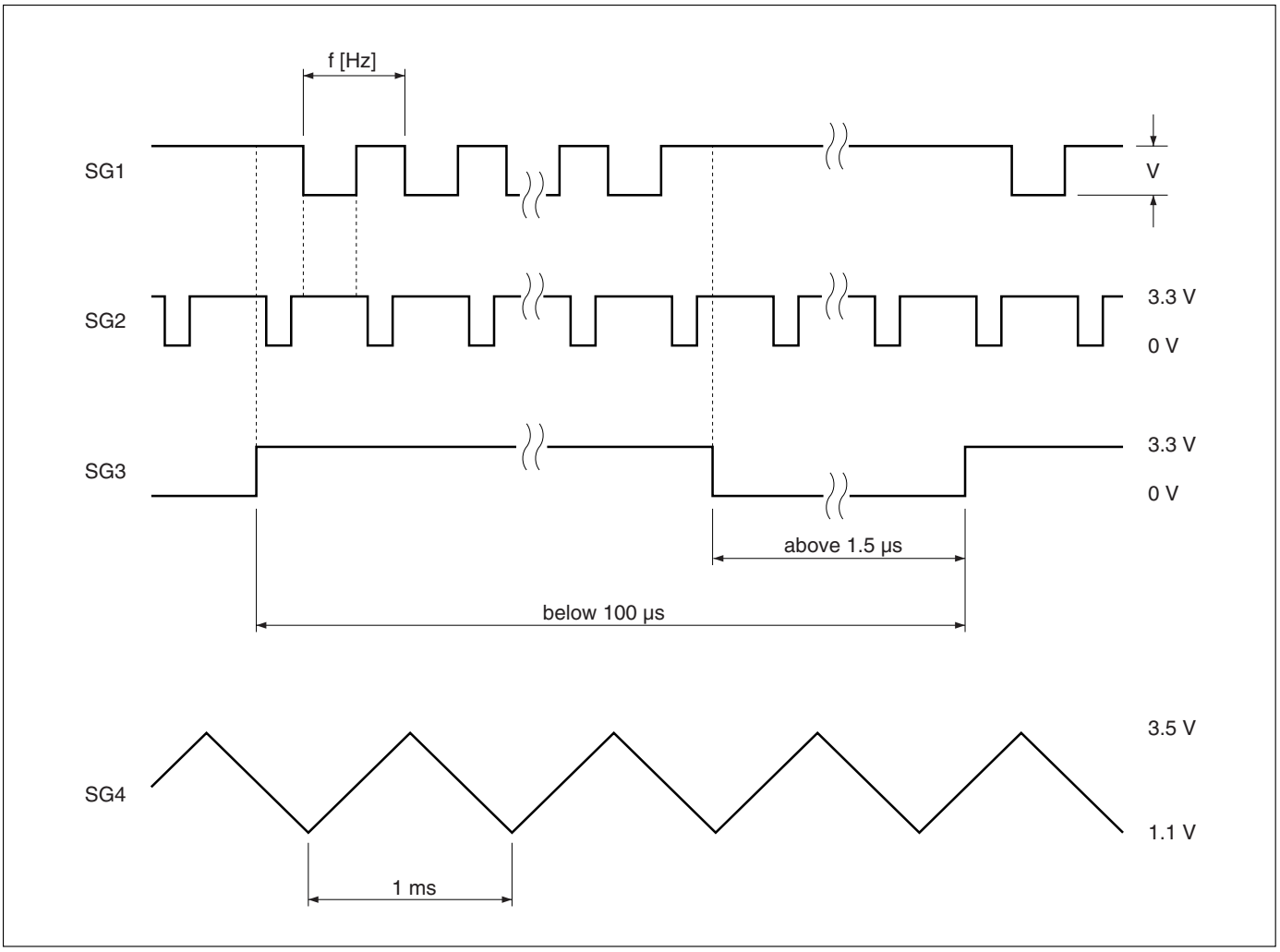
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Bandwidth (1) (Minimum gain)	f_{TN}	(GAIN SEL) = 0, (AGC GAIN) = 0 $\overline{CLP}$ = SG2, $\overline{OBP}$ = SG3 Input the SG1 (f = 2 MHz, V = 0.2 Vp-p) to the SIN and measure the amplitude of the AGCOUT. Increase the frequency and measure the frequency when the amplitude attenuates to −3 dB.	24	35	–	MHz
Bandwidth (2) (Maximum gain)	f_{TX}	(GAIN SEL) = 7, (AGC GAIN) = 255 $\overline{CLP}$ = SG2, $\overline{OBP}$ = SG3 Input the SG1 (f = 2 MHz, V = 8 mVp-p) to the SIN and measure the amplitude of the AGCOUT. Increase the frequency and measure the frequency when the amplitude attenuates to −3 dB.	13	20	–	MHz
OFFSET adjustment limit (1) (OFFSET = 0)	V_{BON}	(GAIN SEL) = 0, (AGC GAIN) = 0 SIN = GND_1, (OFFSET) = 0, $\overline{CLP}$ = 0 V, $\overline{OBP}$ = 0 V Measure the voltage of the AGCOUT at BLK = 3.3 V and define it V_{BO11}. Measure the one similarly at BLK = 0 V and define it V_{BO12}. $V_{BON} = V_{BO12} - V_{BO11}$	–	−75	−60	mV
OFFSET adjustment limit (2) (OFFSET = 63)	V_{BOX}	(GAIN SEL) = 0, (AGC GAIN) = 0 SIN = GND_1, (OFFSET) = 63, $\overline{CLP}$ = 0 V, $\overline{OBP}$ = 0 V Measure the V_{BO21} and V_{BO22} similarly to above-mentioned method. $V_{BON} = V_{BO22} - V_{BO21}$	50	65	–	mV
Output dynamic range (1) (Minimum gain)	V_{DYN}	(GAIN SEL) = 0, (AGC GAIN) = 0 $\overline{CLP}$ = SG2, $\overline{OBP}$ = SG3 Input the SG1 (f = 2 MHz, V = 0.9 Vp-p) to the SIN and measure the amplitude of the AGCOUT.	2.0	2.2	–	Vp-p
Output dynamic range (2) (Maximum gain)	V_{DYX}	(GAIN SEL) = 7, (AGC GAIN) = 255 $\overline{CLP}$ = SG2, $\overline{OBP}$ = SG3 Input the SG1 (f = 2 MHz, V = 50 mVp-p) to the SIN and measure the amplitude of the AGCOUT.	2.0	2.2	–	Vp-p

• **A/D Converter Circuit**

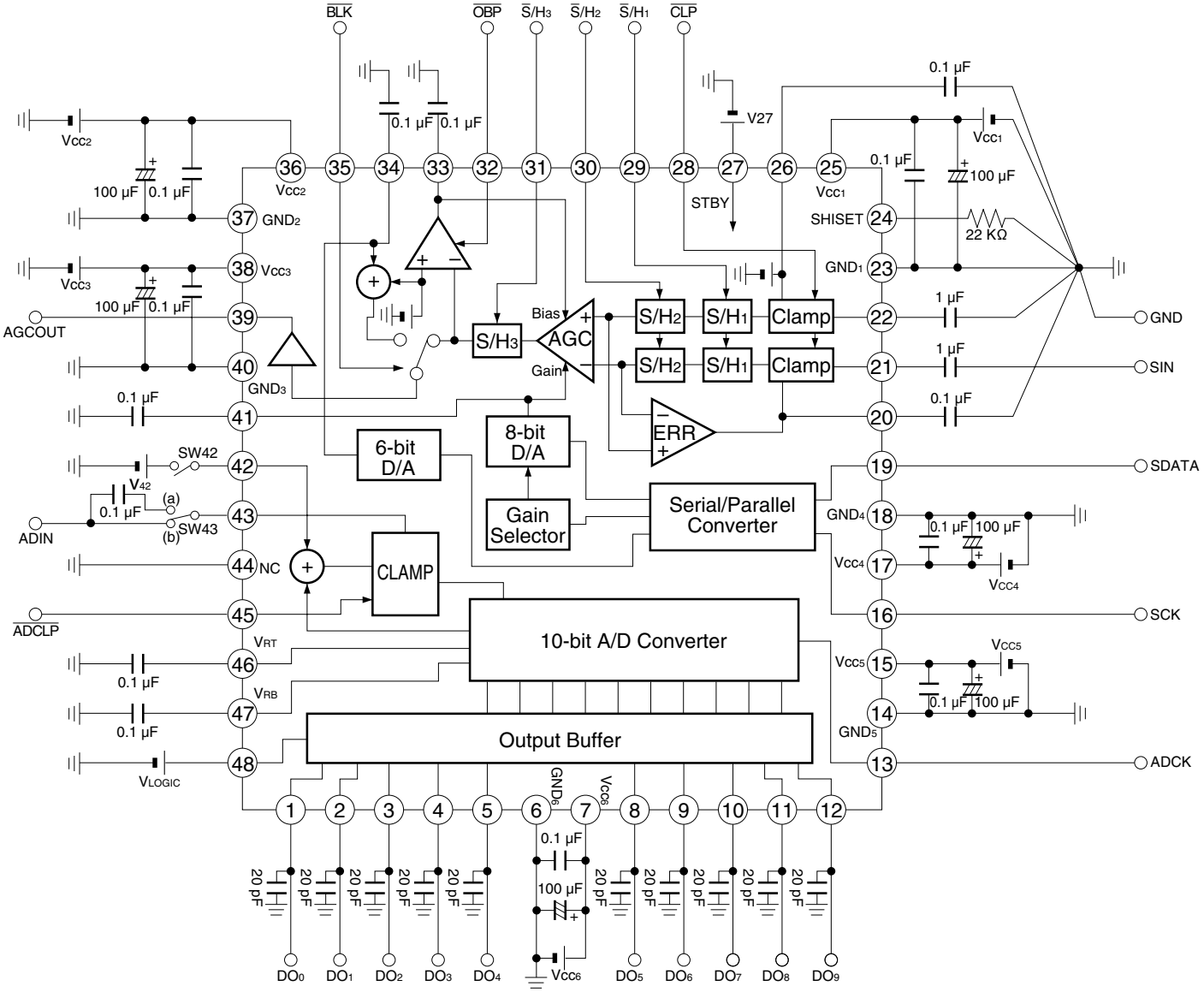
(Unless otherwise specified, T_A = +25 ˚C, V_{CC1} = V_{CC2} = V_{CC3} = V_{CC4} = V_{CC5} = V_{CC6} = 5.0 V, V_{LOGIC} = 3.3 V, ADCK = 18 MHz square wave, $\overline{SCK}$= 0 V, $\overline{SDATA}$ = 0 V, $\overline{STBY}$ = 3.3 V, $\overline{CLP}$ = 3.3 V, $\overline{S}/H_1$ = 0 V, $\overline{S}/H_2$ = 0 V, $\overline{S}/H_3$ = 0 V, $\overline{BLK}$ = 3.3 V, $\overline{OBP}$ = 3.3 V, SW42 = OFF, SW43 = (b), $\overline{ADCLP}$ = 3.3 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Clamp value	D_{CLP}	SW43 = (a) $\overline{ADCLP}$ = 0 V ADCIN = GND_4 Read the output value of DO_0 to DO_9.	56	61	66	–
Clamp value adjustment limit (1)	D_{CLPN}	SW42 = ON, V_{42} = 5.0 V, $\overline{ADCLP}$ = 0 V, ADCIN = GND_4 Read the output value of DO_0 to DO_9.	31	36	41	–
Clamp value adjustment limit (2)	D_{CLPX}	SW42 = ON, V_{42} = 1.6 V, $\overline{ADCLP}$ = 0 V, ADCIN = GND_4 Read the output value of DO_0 to DO_9.	81	86	91	–
Differential linearity error	DLE	ADCIN = SG4 Read the output value of DO_0 to DO_9 at about 10^6 times and make it a histogram. Normalize the histogram and obtain the DLE. Integrate the histogram and obtain the ILE.	–	±0.5	±0.9	LSB
Integral linearity error	ILE		–	±3	±7	LSB
Propagation delay (L→H)	t_{DLH}	ADCIN = SG4, C_L = 20 pF Measure the delay time from the falling edge (50%) of the ADCK to the rising edge (50%) of the DO_0 to DO_9.	15	26	38	ns
Propagation delay (H→L)	t_{DHL}	ADCIN = SG4, C_L = 20 pF Measure the delay time from the falling edge (50%) of the ADCK to the falling edge (50%) of the DO_0 to DO_9.	15	26	38	ns
Output rise time	t_{WLH}	ADCIN = SG4, C_L = 20 pF Measure the rise time (10%→90%) of the DO_0 to DO_9.	10	17	25	ns
Output fall time	t_{WHL}	ADCIN = SG4, C_L = 20 pF Measure the fall time (90%→10%) of the DO_0 to DO_9.	10	17	25	ns

Measurement Waveforms



Test Circuit



PACKAGE

(Unit : mm)

48 QFP (QFP048-P-0707)