

STRUCTURE				
PRODUCT	NAME			

Silicon Monolithic Integrated Circuit System Power Supply with WDT

TYPE

BD4911FM

FEATURES

•Very low current consumption

•Built in multiple microcontroller outputs, RESET with a microcontroller delay, BATTERY/ACCESSORY voltage detection, MUTE function, WDT function.

OABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage1	VIN1	-0.3~36	V
Supply Voltage2	VIN2	-0.3~36	v
Power Dissipation	Pd	2200(*1)	mW
Operating Temperature Range	Topr	-40~+85)C
Storage Temperature Range	Tstg	-55~+150	Ĉ
Peak Supply Voltage1	VIN1 Peak	50(*2)	V
Peak Supply Voltage2	VIN2 Peak	50(*2)	V
Surge Supply Current1	ACC(S+)	+3(*2)	mA
Surge Supply Current2	IACC (S-)	-12(*3)	mA
Max. Junction Temperature	Tjmax	150	C

(*1) When mounted on a PCB (70mm \times 70mm \times 1.6mm glass epoxy)

(*2) tr≥1msec, Bias voltage/current is less than 200msec

(*3) tr≧1msec, Bias voltage/current is less than 60msec

ORECOMMENDED OPERATING RANGES (Ta=25°C)

Parameter	Symbol	Limits				compat	
raidiletei	Symbol	Min.	Тур.	Max.	Unit	comment	
Recommended Power	VIN1	Vo1+1.2	13.2	16.0	V	When using built-in transistor.	
Supply Voltage Rangel	VINI	Vo1+0.5	13.2	16.0	v	When using external boost	
		+eternal TrVBE				transistor.	
Recommended Power Supply Voltage Range2	VIN2	4.5	13.2	16.0	v		
Recommended Power Supply Voltage Range3	Vo1	1.2	-	5.2	v	RESET, DET1	
Recommended Power Supply Voltage Range4	Vo1	2.5	_	5.2	v	BuDET, ACCDET, MUTE,WDT	
Recommended Power Supply Voltage Range5	Vo2	1.2	_	3.4	v	DET2	

※ Electrical characteristics are not guaranteed (especially when operating on reduced voltage).

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*This product is not designed for normal operation within a radio active environment.

*Status of this document

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OELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, VIN1=VIN2=13.2V)

CELECTRICAL CHARACTERISTICS		inise spe	_	10-230,	v : ivi = V I	IIL-13.24/
Parameter	Symbol	Min.	Limits Typ.	Wax.	Unit	Condition
[Overall]						
VIN1 Supply Current	IVIN1	65	95	125	μA	ACC=OV, WDINH=H
VIN2 Supply Current	IVIN2	5	10	20	μA	ACC=OV, WDINH=H
Total Supply Current	IVINA	65	100	135	μA	ACC=0V, WDINH=H
	IVINB	65	130	195	μA	ACC=13.2V
Overvoltage Detection Voltage	VOVP	28	31	34	v	All regulator output off
Overvoltage Detection	VOVPHY	0.5	1	1.5	v	
Hysteresis Width	4041111	0.5	-	1.5	v	All regulator output reset
[Main Regulator (REG1) Sub-Regu	lator (REG2)]					
V01-1 Output Voltage	V01-1	4.8	5.0	5.2	v	VIN1=6.2~16V, Io1=0~150mA, SEL>1.5V
V01-1 Line Regulation	∆V01-11	-	1	30	mV	VIN1=6.2~16V, SEL>1.5V
V01-1 Load Regulation	∆V01-1L	_	7	50	mV	lo1=0~150mA, SEL>1.5V
V01-2,V02 Output Voltage	V01-2,2	3.168	3.3	3.432	~	VIN1,2=4.5~16V, 101,2=0~150mA,SEL<1.0V
V01-2,V02 Line Regulation	∆V01-2,2I	-	1	30	mV	VIN1, 2=4.5~16V, SEL<1.0V
V01-2,V02 Load Regulation	△V01-2,2L	-	7	30	mV	101,2=0~150mA,SEL<1.0V
Minimum V01,2 Output	V01,2-L	2.5	-	_	v	VIN1, 2=3.0V, 101, 2=0mA
Short Protection Start Current	101,2max	150	400	600	mA	
Ripple Rejection	RRV01,2	45	55	-	dB	fin=120Hz,-10dBV, Io1,2=150mA
V01 Sink Current	1 V 01 in	35	90	145	μA	Vo1=5V, VIN1=ACC=OPEN, WDINH=SEL=5V
[External Boost Transistor Curre	ent-Limiting Ci	rcuit (OCP)]			
OCP Input Current	IOCP	0	0.1	1.0	μA	VOCP=VIN1=16V
OCP Detection Voltage	V0CP1	360	400	440	mV	Voltage differential with VIN1
00P Detection Voltage	V0CP2	20	20	50		
(during output ground fault)	VUCP2	20	32	50	mV	Vo1=OV, voltage differential with VIN1
(Elevated Output Detection Circu	[Elevated Output Detection Circuit (COMP)]					
Elevated Output Detection Voltage1	V0VER1	5.30	5.49	5.68	v	SEL>1.5V
Elevated Output Detection Voltage2	V0VER2	3.5	3.62	3.75	v	SEL<1.0V
Elevated Output Detection Output	VCOMP	1	0.1	0.4	v	V01>5.68V, Io=100 µ A
Output Off Delay Time	TmVoff	1	-	50	μS	Vol:3.1 \rightarrow 4.8V(tr=0.01V/ μ S) VIN1=4.8V, Ro=1k Ω
Regulator Voltage Selection Cir	rcuit (SEL)]					
SEL Threshold	VTHSEL	1.20	1.25	1.30	V	
SEL Input Current	ISEL	1	2	4	μA	VSEL=5V
[V01,2 Reduced-Voltage Detection	n Circuit (DET1	,2)]				
V01-1 Detection Voltage	VTLP1-1	4.00	4.15	4.30	v	Vol falling, SEL>1.5V
V01-1 Reset Voltage	VTHP1-1	4.10	4.35	4.60	v	Vol rising, SEL>1.5V
V01-1 Hysteresis Width	VHSP1-1	0.1	0.2	0.3	v	SEL>1.5V
V01-2,V02 Detection Voltage	VTLP1-2,2	2.85	2.95	3.05	V	Vol,2 falling, SEL<1.0V
V01-2,V02 Reset Voltage	VTHP1-2,2	2.92	3.09	3.26	v	Vol,2 rising, SEL<1.0V
V01-2,V02 Hysteresis Width	VHSP1-2,2	0.07	0.14	0.21	v	SEL<1.0V
DET1,2 Output On Resistance	RDET1,2	-	270	600	Ω	IDET1.2=1mA
DET1,2 Output Saturation Voltage	VDET1,2L	-	0.1	0.4	v	IDET1, 2=2 µ A, Vo1=1.2V
[Power-On Reset Timer (CTP, RESET	T)]				•	
CTP Charge Resistance1	RCTP1	0.6	0.9	1.2	MΩ	When RESET is low (while charging).
CTP Charge Resistance2	RCTP2	5.5	8.5	11.5	kΩ	When RESET is high (after charging is complete).
Power-On Reset Time	TPR	60	100	140	mS	CTP=0.1 µF
Reset-On Delay Time	TDR	10	50	100	μS	CTP=0.1 µF
RESET Output On Resistance	RRST	-	-	100	Ω	IRST=1mA

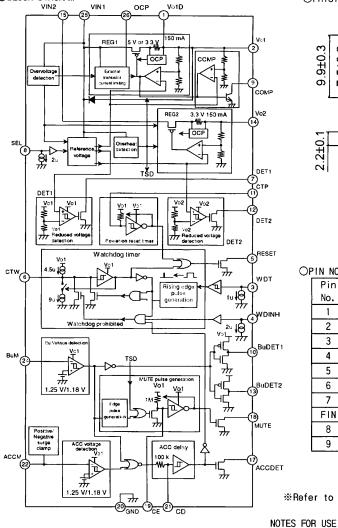
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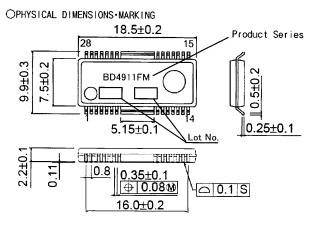
OELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, VIN1=VIN2=13.2V)

DELECTRICAL CHARACTERISTICS (130 Spect	Limits	0, 1111-1	112-10.2		
Parameter	Symbol	Min. Typ.		Max.	Unit	Condition	
[Watchdog Timer (WDT,WDINH,CTW)]							
Runaway Operation Detection Time1	TWD1	420	700	980	mS	CT=1 μF, V01=5V	Time from final WDT signal
Runaway Operation Detection Time2	TWD2	277.2	462.0	646.8	mS	CT=1 µF, V01=3. 3V	Input to RESET inversion
Runaway Operation Reset Time1	TWR1	204	340	476	mS	CT=1 µF, V01=5V	I
Runaway Operation Reset Time2	TWR2	156	260	364	mS	CT=1 µF, V01=3.3V	
CTW Charge Current (Source)	I HCTW	3.3	4.7	6.1	μA		
CTW discharge Current (Sink)	ILCTW	3.4	4.8	6.2	μA	·····	
	RCTWon1		16	50	Ω	When WDT signal input	is active.
CTW Rapid Discharge Resistance	RCTWon2		0.5	2.5	kΩ	ACC:L,WDINH:H	
WDT Input Current	IWDT	0.5	1.0	2.0	μA	VWDT=5V.SEL>1.5V	<u>.</u>
WDT Edge Pulse Width	TPULSE	100	190	300	μS		
WDINH Input Voltage H	VIH	0.8XVo1	_	_	v		
WDINH Input Voltage L	VIL		_	0.3XVo1	v		
WDINH Input Current	IWDINH	1	2	4	μA	VWDINH=5V, SEL<1.0V	· ··· ·· ·
[Bu Voltage Detection Circuit (Bu	M, BuDET)]		1		<u> </u>	I.,	
BuM Detection Voltage (rising)					<u> </u>		
BuDET:H→L.AccDET:H→L	VTHB	1.214	1.252	1.290	v	IC without heat sink	
BuM Detection Voltage (falling)							
BuDET:L→H,AccDET:L→H	VTLB	1.148	1.184	1.220	V V	IC without heat sink	
BuDET1,2 High Output Voltage	VBDTH1.2	Vo-0.4	Vo-0.2	_	v	lout=-5mA	· · · · ·
BuDET1,2 Low Output Voltage	VBDTL1,2	-	0.15	0.40	v	lout=5mA	
	I BM1	0	4	110	nA	BuM=1V	
BuM Input Current	IBM2	0	20	110	nA	BuM=2V	- · · · ·
[NUTE One-Shot Pulse Generation C	ircuit (MUTE, C	E)]	I	·	1		
MUTE Pulse width	Tm	0.6	1.0	1.4	S	CE=1 µF, SEL<1.0V, SEL>	1.5V
	Td1	0	5	10	μS	CE=1 μF, SEL>1.5V	
MUTE Pulse On Delay Time	Td2	0	8	16	μS	CE=1 μF, SEL<1.0V	
CE Charge Resistance1	RTM1	0.7	1.0	1.3	MΩ	When MUTE is on (resi	stance while charging).
			11.5			When MUTE is off (res	sistance when stabilized
CE Charge Resistance2	RTM2	8.0		15.0	kΩ	after charging).	
CE Rapid Discharge Resistance	RCEon	-	4	20	Ω	Must satisfy Td.	
CE Output Saturation Voltage	VCEL		0.1	0.3	v	CE output on, ICE=0 µ	Α
MUTE Output Saturation Voltage	VMUTEL	_	0.2	0.4	v	IMUTE=5mA	
[ACC Voltage Detection & Delay Ci	rcuit (ACCM, CD	, ACCDET)]		1			
ACCM Detection Voltage (rising)	VTHA	1.214	1.252	1.290	V	IC without heat sink.	BuM=H
ACCM Detection Voltage (falling)	VTLA	1.148	1.184	1.220	v	IC without heat sink,	BuM=H
ACCM Positive Clamp Voltage		8	11	14	v	IACCM=+5mA	
	VHACC						
ACCM Negative Clamp Voltage	VHACC VLACC	-0.30	-0.15	0	V	IACCM=-12mA	
ACCM Negative Clamp Voltage ACCM Input Current1				0	۷ µA	IACCM=-12mA ACCM=0V	
	VLACC	-0.30	-0.15		1		
ACCM Input Current1	VLACC IACC1	-0.30 -5	-0.15 -1	0	μA	ACCM=0V	
ACCM Input Current1 ACCM Input Current2	VLACC IACC1 IACC2	-0.30 -5 0	-0.15 -1 10	0	μA nA	ACCM=0V ACCM=2V	
ACCW Input Current1 ACCW Input Current2 CD Delay Time	VLACC IACC1 IACC2 TdLH, L	-0.30 -5 0 6	-0.15 -1 10 10	0 110 14	μA nA mS	ACCM=0V ACCM=2V	
ACCW Input Current1 ACCW Input Current2 CD Delay Time CD Charge/Discharge Resistance	VLACC IACC1 IACC2 TdLH, L ICDH, L VADTL	-0.30 -5 0 6 60 -	-0.15 -1 10 10 90	0 110 14 120	μA nA mS kΩ	ACCM=0V ACCM=2V CD=0.1 μF	
ACCW Input Current1 ACCM Input Current2 CD Delay Time CD Charge/Discharge Resistance ACCDET Output Saturation Voltage [Delay Time Setting Pin (CTP, CTW	VLACC IACC1 IACC2 TdLH, L ICDH, L VADTL	-0.30 -5 0 6 60 -	-0.15 -1 10 10 90	0 110 14 120	μA nA mS kΩ	ACCM=0V ACCM=2V CD=0.1 μF	
ACCW Input Current1 ACCW Input Current2 CD Delay Time CD Charge/Discharge Resistance ACCDET Output Saturation Voltage	VLACC IACC1 IACC2 TdLH,L ICDH,L VADTL V, WDT, CE, CD)	-0.30 -5 0 6 60 	-0.15 -1 10 10 90 0.2	0 110 14 120 0.4	μΑ nA mS kΩ V	ACCM=0V ACCM=2V CD=0.1 μF IADT=5mA	
ACCW Input Current1 ACCM Input Current2 CD Delay Time CD Charge/Discharge Resistance ACCDET Output Saturation Voltage [Delay Time Setting Pin (CTP, CTW	VLACC IACC1 IACC2 TdLH,L ICDH,L VADTL VADTL VTH1	-0.30 -5 0 6 60 -	-0.15 -1 10 10 90 0.2 3.33	0 110 14 120 0.4 3.66	μA nA mS kΩ V	ACCM=OV ACCM=2V CD=0.1 μF IADT=5mA SEL>1.5V	

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OBLOCK DIAGRAM





HSOP-M28 (Unit:mm)

OPIN NO. . PIN NAME

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	Vo1D	10	BuDET1	20	GND
2	Vo1	11	СТР	21	CD
3	WDT	12	DET2	FIN	FIN
4	WDINH	13	BuDET2	22	ACCM
5	RESET	14	Vo2	23	N.C.
6	CTW	15	V1N2	24	BuM
7	DET1	16	N.C.	25	N.C.
FIN	FIN	17	ACCDET	26	0CP
8	SEL	18	MUTE	27	N.C.
9	COMP	19	CE	28	VIN1

*Refer to the Technical Note about the details of the application.

1. Overvoltage protection circuit

Overvoltage protection is designed to turn off all output voltages when the voltage differential between the VIN1 and GND pins exceeds approximately 31V (at room temperature). Use caution when determining the power supply voltage range to use. 2. Bypass capacitor between the VIN1,2 and GND pins

- It is recommended to insert bypass capacitor with above 0.47 μ F between the VIN and GND pins.
- 3. Output capacitors

Capacitors for stopping oscillation must be placed between the Vol,2 pin and the GND pin.

It is recommended to use a ceramic capacitor with above $10\,\mu$ F (B characteristics). When using an external boost transistor, the ceramic capacitor described above should be connected in series with a 1Ω resistor.

4. When abruptly fluctuated input voltage

Abrupt VIN1,2 voltage can be made to occur OVERSHOOT. Output capacitor should be determined after sufficient testing of the actual application.

[Recommendation] When using a built-in Tr

When Vo1 output 5V : When VIN1=4.8 \rightarrow 16V, MAX0.6V/ μ s and using ceramic capacitor with above 50 μ F (B characteristics), output voltage can hold less than 6.5V.

When Vol output 3.3V : When VIN1=3.2 \rightarrow 16V, MAX0.6V/ μ s and using ceramic capacitor with above 70 μ F (B characteristics), output voltage can hold less than 4.6V.

5. Pull up resistor for RESET, DET1, DET2, ACCDET, MUTE, COMP pin

Connect the pull up resistor for RESET, DET1, DET2, ACCDET, MUTE, COMP pin to less than Vo1 voltage. 6. VIN1,2 plus surge

In case of the over 50V surge at VIN1,2, use the Power Zenner Diode between VIN1,2 and GND.

7. BuM, ACCM pin

External resistor for BuM and ACCM pin have to be high accuracy : temperature characteristics etc. In case of changing the value of external resistor, be careful to threshold voltage.

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