

# Product Preview

## 256K x 16 Bit 3.3 V Asynchronous Fast Static RAM

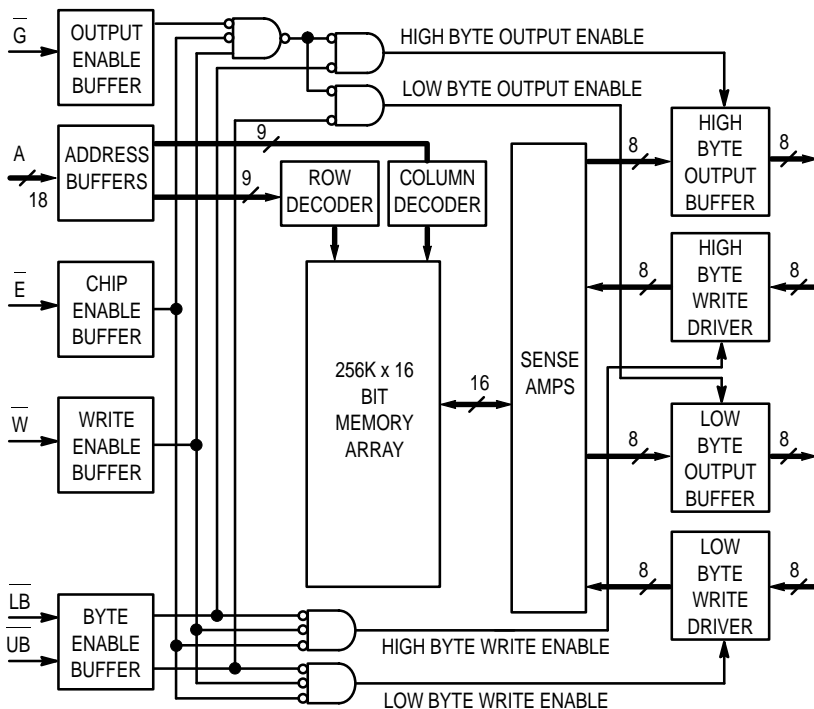
The MCM6343 is a 4,194,304-bit static random access memory organized as 262,144 words of 16 bits. Static design eliminates the need for external clocks or timing strobes.

The MCM6343 is equipped with chip enable ( $\bar{E}$ ), write enable ( $\bar{W}$ ), and output enable ( $\bar{G}$ ) pins, allowing for greater system flexibility and eliminating bus contention problems. Separate byte enable controls (LB and UB) allow individual bytes to be written and read. LB controls the lower bits DQ0 to DQ7, while UB controls the upper bits DQ8 to DQ15.

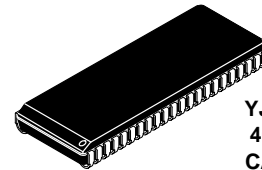
The MCM6343 is available in a 400 mil, 44-lead small-outline SOJ package and a 44-lead TSOP Type II package.

- Single 3.3 V  $\pm$  0.3 V Power Supply
- Fast Access Time: 12/15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Data Byte Control
- Fully Static Operation
- Power Operation: 250/240/230 mA Maximum, Active AC
- Commercial and Standard Industrial Temperature Option: - 40 to + 85°C

### BLOCK DIAGRAM



## MCM6343



**YJ PACKAGE**  
400 MIL SOJ  
CASE 919-01



**TS PACKAGE**  
TSOP TYPE II  
CASE 924A-02

### PIN ASSIGNMENT

A	1	44	A
A	2	43	A
A	3	42	A
A	4	41	G
A	5	40	UB
E	6	39	LB
DQ0	7	38	DQ15
DQ1	8	37	DQ14
DQ2	9	36	DQ13
DQ3	10	35	DQ12
VDD	11	34	VSS
VSS	12	33	VDD
DQ4	13	32	DQ11
DQ5	14	31	DQ10
DQ6	15	30	DQ9
DQ7	16	29	DQ8
W	17	28	NC
A	18	27	A
A	19	26	A
A	20	25	A
A	21	24	A
A	22	23	A

### PIN NAMES

A0 – A17	.....	Address Input
E	.....	Chip Enable
W	.....	Write Enable
G	.....	Output Enable
UB	.....	Upper Byte
LB	.....	Lower Byte
DQ0 – DQ15	.....	Data Input/Output
VDD	.....	+ 3.3 V Power Supply
VSS	.....	Ground
NC	.....	No Connection

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REV 2  
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**TRUTH TABLE** (X = Don't Care)

E	G	W	LB	UB	Mode	V <sub>DD</sub> Current	DQ0 – DQ7	DQ8 – DQ15
H	X	X	X	X	Not Selected	I <sub>SB1</sub> , I <sub>SB2</sub>	High-Z	High-Z
L	H	H	X	X	Output Disabled	I <sub>DDA</sub>	High-Z	High-Z
L	X	X	H	H	Output Disabled	I <sub>DDA</sub>	High-Z	High-Z
L	L	H	L	H	Low Byte Read	I <sub>DDA</sub>	D <sub>out</sub>	High-Z
L	L	H	H	L	High Byte Read	I <sub>DDA</sub>	High-Z	D <sub>out</sub>
L	L	H	L	L	Word Read	I <sub>DDA</sub>	D <sub>out</sub>	D <sub>out</sub>
L	X	L	L	H	Low Byte Write	I <sub>DDA</sub>	D <sub>in</sub>	High-Z
L	X	L	H	L	High Byte Write	I <sub>DDA</sub>	High-Z	D <sub>in</sub>
L	X	L	L	L	Word Write	I <sub>DDA</sub>	D <sub>in</sub>	D <sub>in</sub>

**ABSOLUTE MAXIMUM RATINGS** (See Notes)

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>DD</sub>	- 0.5 to + 4.6	V
Voltage on Any Pin	V <sub>in</sub>	- 0.5 to V <sub>DD</sub> + 0.5	V
Output Current per Pin	I <sub>out</sub>	± 20	mA
Package Power Dissipation	P <sub>D</sub>	TBD	W
Temperature Under Bias	T <sub>bias</sub>	- 10 to + 85	°C
Commercial Industrial		- 45 to + 90	
Operating Temperature	T <sub>A</sub>	0 to + 70	°C
Commercial Industrial		- 45 to + 85	
Storage Temperature	T <sub>stg</sub>	- 55 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. All voltages are referenced to V<sub>SS</sub>.
3. Power dissipation capability will be dependent upon package characteristics and use environment.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $T_A = 0 \text{ to } 70^\circ\text{C}$ , Unless Otherwise Noted)

( $T_A = -40 \text{ to } +85^\circ\text{C}$  for Industrial Temperature Offering)

### RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	$V_{DD}$	3.0	3.3	3.6	V
Input High Voltage	$V_{IH}$	2.2	—	$V_{DD} + 0.3^{**}$	V
Input Low Voltage	$V_{IL}$	$-0.5^*$	—	0.8	V

\*  $V_{IL}(\text{min}) = -0.5 \text{ V dc}$ ;  $V_{IL}(\text{min}) = -2.0 \text{ V ac}$  (pulse width  $\leq 20 \text{ ns}$ ) for  $I \leq 20.0 \text{ mA}$ .

\*\*  $V_{IH}(\text{max}) = V_{DD} + 0.3 \text{ V dc}$ ;  $V_{IH}(\text{max}) = V_{DD} + 2.0 \text{ V ac}$  (pulse width  $\leq 20 \text{ ns}$ ) for  $I \leq 20.0 \text{ mA}$ .

### DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0 \text{ to } V_{DD}$ )	$I_{lkg}(I)$	—	$\pm 1.0$	$\mu\text{A}$
Output Leakage Current ( $E = V_{IH}$ , $V_{out} = 0 \text{ to } V_{DD}$ )	$I_{lkg}(O)$	—	$\pm 1.0$	$\mu\text{A}$
Output Low Voltage ( $I_{OL} = +4.0 \text{ mA}$ ) ( $I_{OL} = +100 \mu\text{A}$ )	$V_{OL}$	—	0.4 $V_{SS} + 0.2$	V
Output High Voltage ( $I_{OH} = -4.0 \text{ mA}$ ) ( $I_{OH} = -100 \mu\text{A}$ )	$V_{OH}$	2.4 $V_{DD} - 0.2$	—	V

### POWER SUPPLY CURRENTS

Parameter	Symbol	0 to 70°C	-40 to +85°C	Unit
AC Active Supply Current ( $I_{out} = 0 \text{ mA}$ , $V_{CC} = \text{max}$ ) MCM6343-12: $t_{AVAV} = 12 \text{ ns}$ MCM6343-15: $t_{AVAV} = 15 \text{ ns}$	$I_{CC}$	240 230	240	mA
AC Standby Current ( $V_{CC} = \text{max}$ , $E = V_{IH}$ , No other restrictions on other inputs) MCM6343-12: $t_{AVAV} = 12 \text{ ns}$ MCM6343-15: $t_{AVAV} = 15 \text{ ns}$	$I_{SB1}$	50 45	55 50	mA
CMOS Standby Current ( $E \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \leq V_{SS} + 0.2 \text{ V}$ or $\geq V_{CC} - 0.2 \text{ V}$ ) ( $V_{CC} = \text{max}$ , $f = 0 \text{ MHz}$ )	$I_{SB2}$	5	5	mA

**CAPACITANCE** ( $f = 1.0 \text{ MHz}$ ,  $dV = 3.0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	$C_{in}$	—	6	pF
Control Input Capacitance	$C_{in}$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $T_A = 0\text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

( $T_A = -40\text{ to } +85^\circ\text{C}$  for Industrial Temperature Offering)

Logic Input Timing Measurement Reference Level ..... 1.50 V  
 Logic Input Pulse Levels ..... 0 to 3.0 V  
 Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... 1.50 V  
 Output Load ..... See Figure 1

### READ CYCLE TIMING (See Notes 1, 2, and 3)

Parameter	Symbol	MCM6343-12		MCM6343-15		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	$t_{AVAV}$	12	—	15	—	ns	4
Address Access Time	$t_{AVQV}$	—	12	—	15	ns	
Enable Access Time	$t_{ELQV}$	—	12	—	15	ns	5
Output Enable Access Time	$t_{GLQV}$	—	6	—	7	ns	
Output Hold from Address Change	$t_{AXQX}$	3	—	3	—	ns	
Enable Low to Output Active	$t_{ELQX}$	3	—	3	—	ns	6, 7, 8
Output Enable Low to Output Active	$t_{GLQX}$	0	—	0	—	ns	6, 7, 8
Enable High to Output High-Z	$t_{EHQZ}$	0	6	0	7	ns	6, 7, 8
Output Enable High to Output High-Z	$t_{GHQZ}$	0	6	0	7	ns	6, 7, 8
Byte Enable Access Time	$t_{BLQV}$	—	6	—	7	ns	
Byte Enable Low to Output Active	$t_{BLQX}$	0	—	0	—	ns	6, 7, 8
Byte High to Output High-Z	$t_{BHQZ}$	0	6	0	7	ns	6, 7, 8

#### NOTES:

1. W is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. Device is continuously selected ( $E \leq V_{IL}$ ,  $G \leq V_{IL}$ ).
4. All read cycle timings are referenced from the last valid address to the first transitioning address.
5. Addresses valid prior to or coincident with E going low.
6. At any given voltage and temperature,  $t_{EHQZ}\text{ max} < t_{ELQX}\text{ min}$ , and  $t_{GHQZ}\text{ max} < t_{GLQX}\text{ min}$ , both for a given device and from device to device.
7. This parameter is sampled and not 100% tested.
8. Transition is measured  $\pm 200\text{ mV}$  from steady-state voltage.

### TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

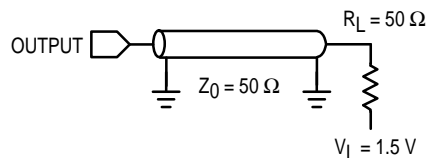
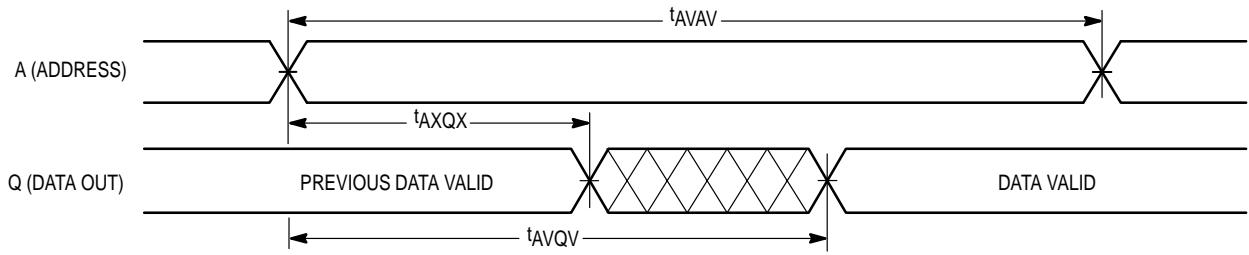
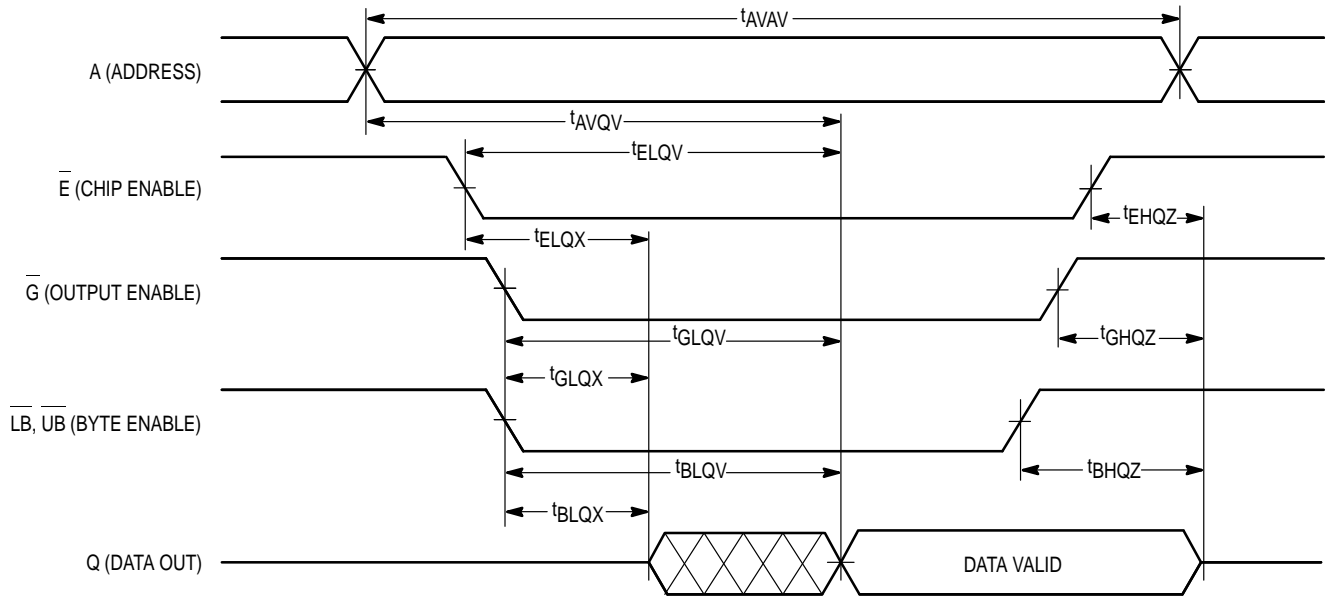


Figure 1. AC Test Load

**READ CYCLE 1 (See Note 8)**



**READ CYCLE 2 (See Note 4)**

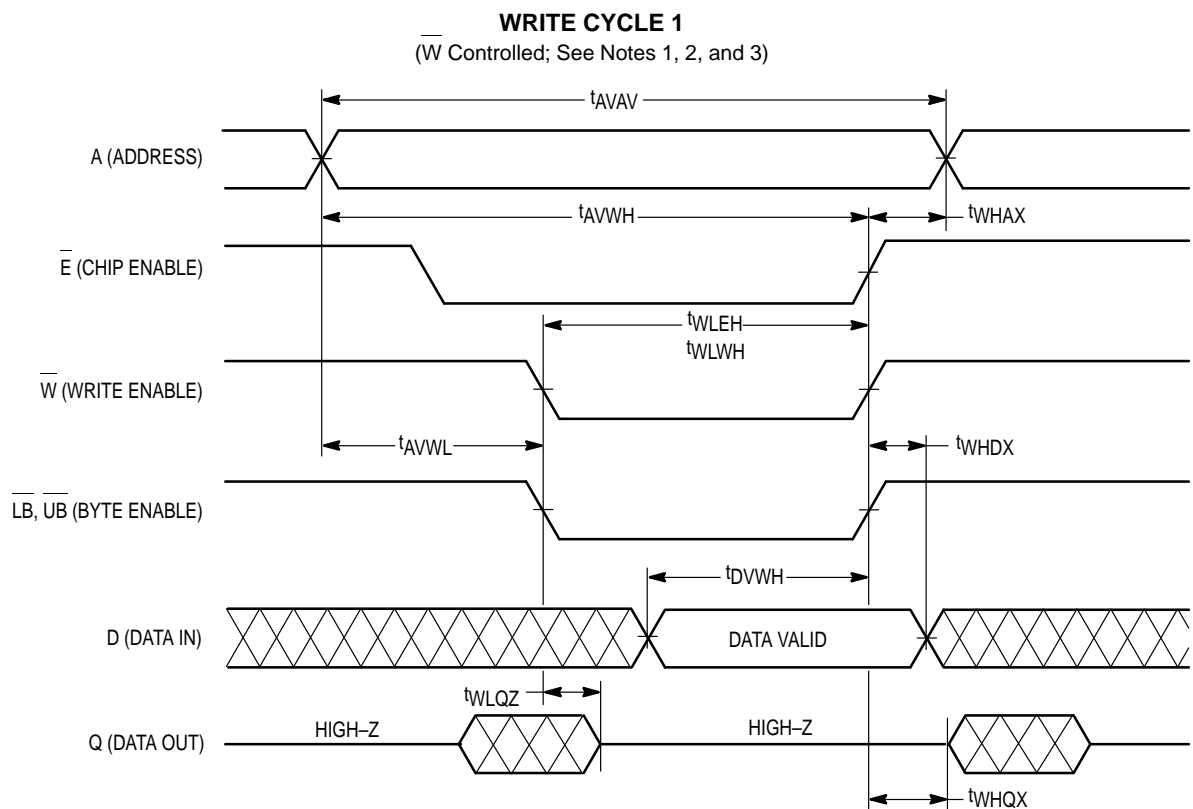


**WRITE CYCLE 1** ( $\bar{W}$  Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6343-12		MCM6343-15		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	12	—	15	—	ns	4
Address Setup Time	$t_{AVWL}$	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	10	—	12	—	ns	
Address Valid to End of Write (G High)	$t_{AVWH}$	9	—	10	—	ns	
Write Pulse Width	$t_{WLWH}$ $t_{WLEH}$	10	—	12	—	ns	
Write Pulse Width (G High)	$t_{WLWH}$ $t_{WLEH}$	9	—	10	—	ns	
Data Valid to End of Write	$t_{DVWH}$	6	—	7	—	ns	
Data Hold Time	$t_{WHDX}$	0	—	0	—	ns	
Write Low to Data High-Z	$t_{WLQZ}$	0	6	0	7	ns	5, 6, 7
Write High to Output Active	$t_{WHQX}$	3	—	3	—	ns	5, 6, 7
Write Recovery Time	$t_{WHAX}$	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If  $\bar{G}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. This parameter is sampled and not 100% tested.
6. Transition is measured  $\pm 200$  mV from steady-state voltage.
7. At any given voltage and temperature,  $t_{WLQZ} \text{ max} < t_{WHQX} \text{ min}$  both for a given device and from device to device.

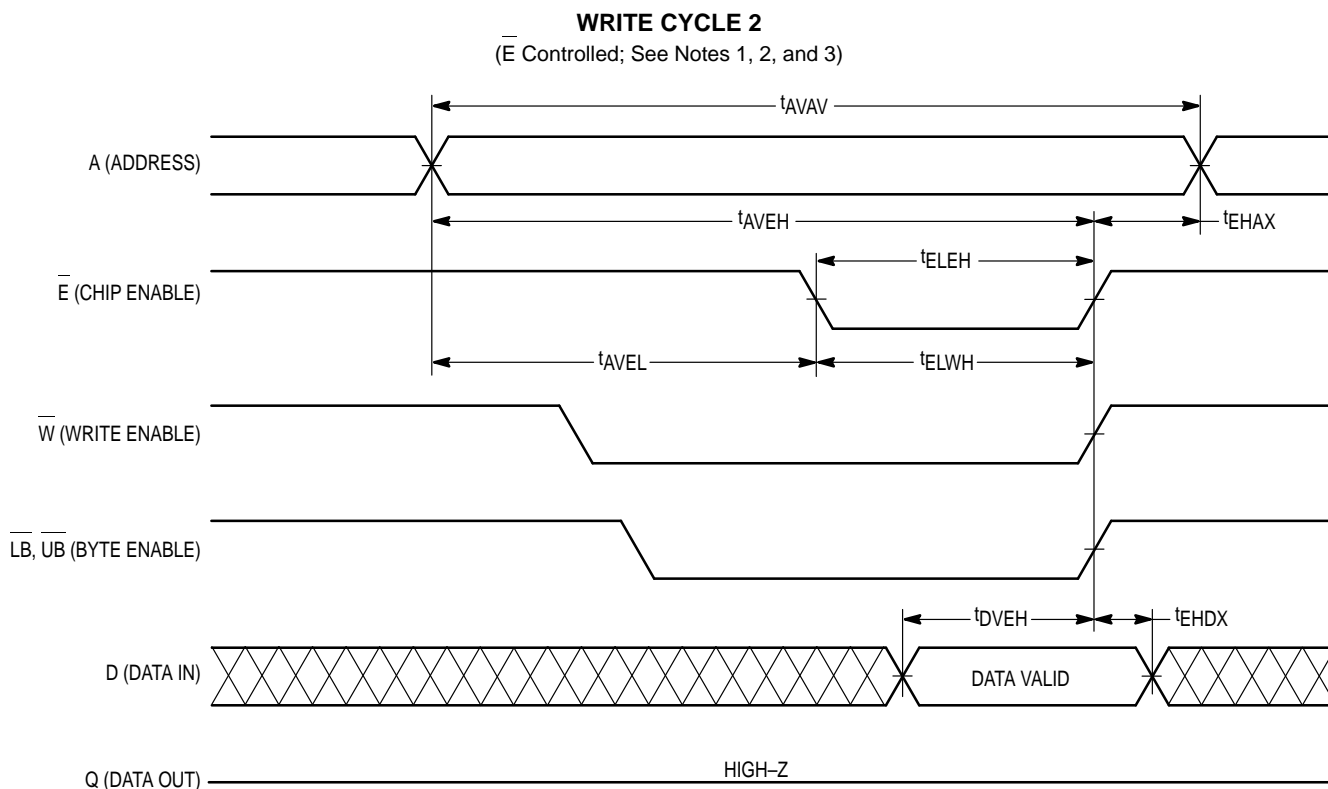


**WRITE CYCLE 2** ( $\bar{E}$  Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6343-12		MCM6343-15		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	12	—	15	—	ns	4
Address Setup Time	$t_{AVEL}$	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVEH}$	10	—	12	—	ns	
Address Valid to End of Write (G High)	$t_{AVEH}$	9	—	10	—	ns	
Enable to End of Write	$t_{ELEH}$ , $t_{ELWH}$	10	—	12	—	ns	5, 6
Enable to End of Write (G High)	$t_{ELEH}$ , $t_{ELWH}$	9	—	10	—	ns	5, 6
Data Valid to End of Write	$t_{DVEH}$	6	—	7	—	ns	
Data Hold Time	$t_{EHDX}$	0	—	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If G goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high-impedance condition.
6. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high-impedance condition.

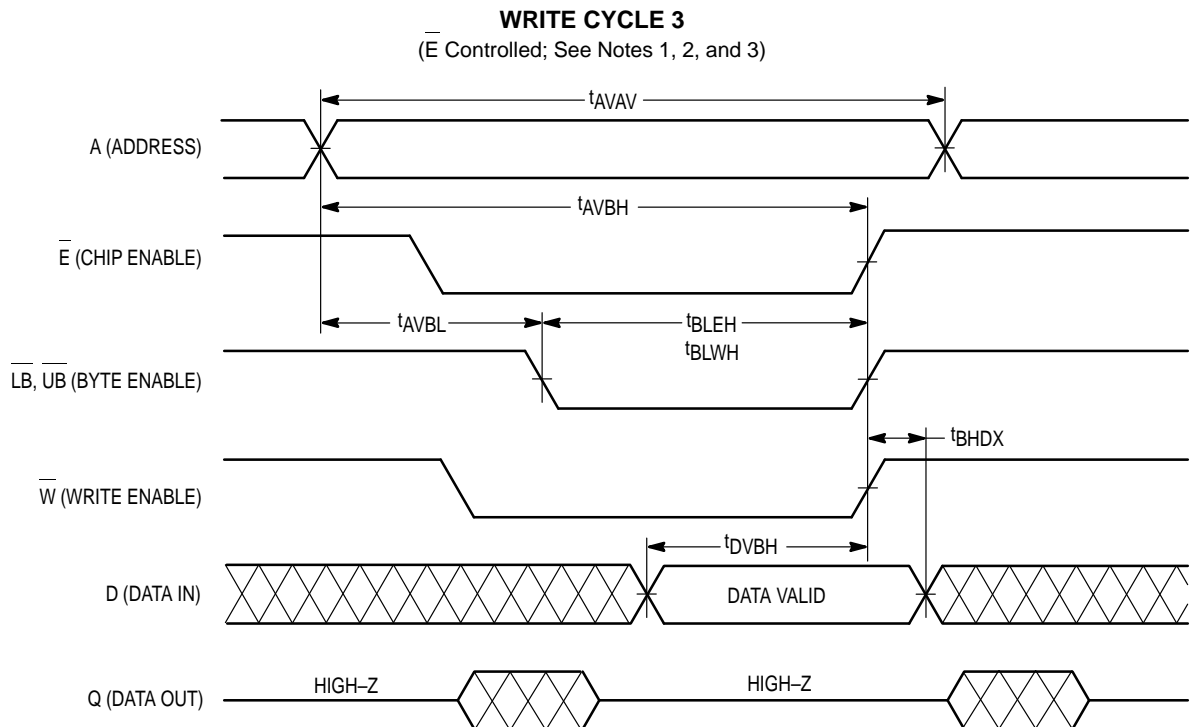


**WRITE CYCLE 3** ( $\bar{E}$  Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	MCM6343-12		MCM6343-15		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	12	—	15	—	ns	4
Address Setup Time	$t_{AVBL}$	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVBH}$	10	—	12	—	ns	
Address Valid to End of Write (G High)	$t_{AVBH}$	9	—	10	—	ns	
Byte Pulse Width	$t_{BLWH}$ $t_{BLEH}$	10	—	12	—	ns	
Byte Pulse Width (G High)	$t_{BLWH}$ $t_{BLEH}$	9	—	10	—	ns	
Data Valid to End of Write	$t_{DVBH}$	6	—	7	—	ns	
Data Hold Time	$t_{BHDX}$	0	—	0	—	ns	

NOTES:

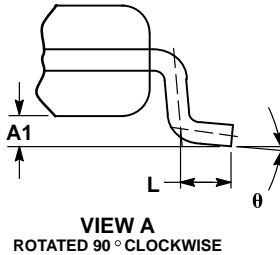
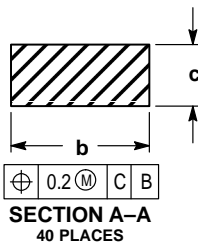
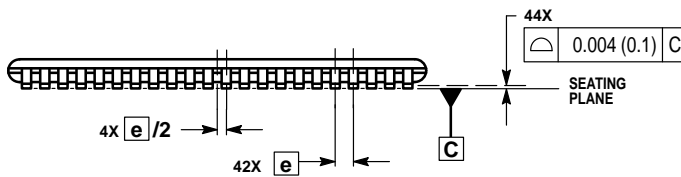
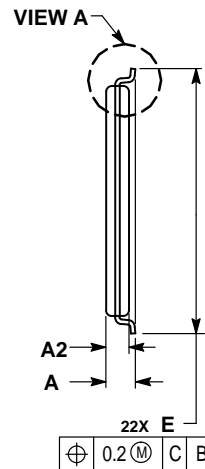
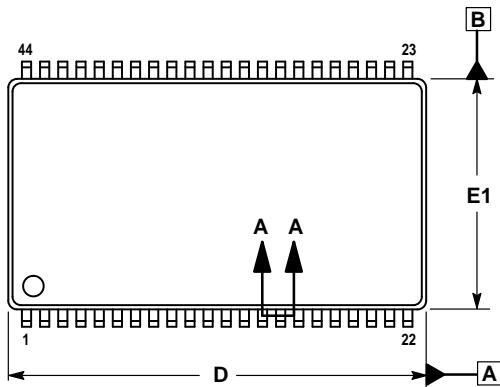
1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If G goes low coincident with or after W goes low, the output will remain in a high-impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.







**TS PACKAGE  
44-LEAD  
TSOP TYPE II  
CASE 924A-02**



**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.58.

MILLIMETERS		
DIM	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.95	1.05
b	0.30	0.45
c	0.12	0.21
D	18.28	18.54
e	0.80 BSC	
E	11.56	11.96
E1	10.03	10.29
L	0.40	0.60
θ	0°	5°

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