MPNC22D-38KX3 PC-2100 CL2.5 184pin DDR Registered DIMM

64M´72 DDR SDRAM DIMM with PLL & Register based on 32Mx8 DDR SDRAM

DESCRIPTION

The Kingmax MPNC22D-38KX3 is 64M bit × 72 Double Data Rate SDRAM high density memory module. The MPNC22D-38KX3 consists of eighteen CMOS 32M × 8 bit with 4 banks Double Data Rate SDRAMs in 60-balls TinyBGA package, two 14-bit Drive ICs for input control signal, one PLL in 48-pin TSSOP package for clock and one 2K EEPROM in 8-Pin TSSOP package for Serial Presence Detect, mounted on a 184-Pin glass-epoxy substrate. 0.2uF&2.2nF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM.

The MPNC22D-38KX3 is a Dual In-line Memory Module and intended for mounting into 184-Pin edge connector socket.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- Performance range - 133MHz (7.5ns @ CL=2.5)
- Power supply : V_{DD}: 2.5V ± 0.2V, V_{DDQ}: 2.5V ± 0.2V
- Double-data-rate architecture; two data transfers per clock cycle
- Bi-directional data strobe (DQS)
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1100 mil, double sided component

PIN CONFIGURATIONS (Front side/Back side)

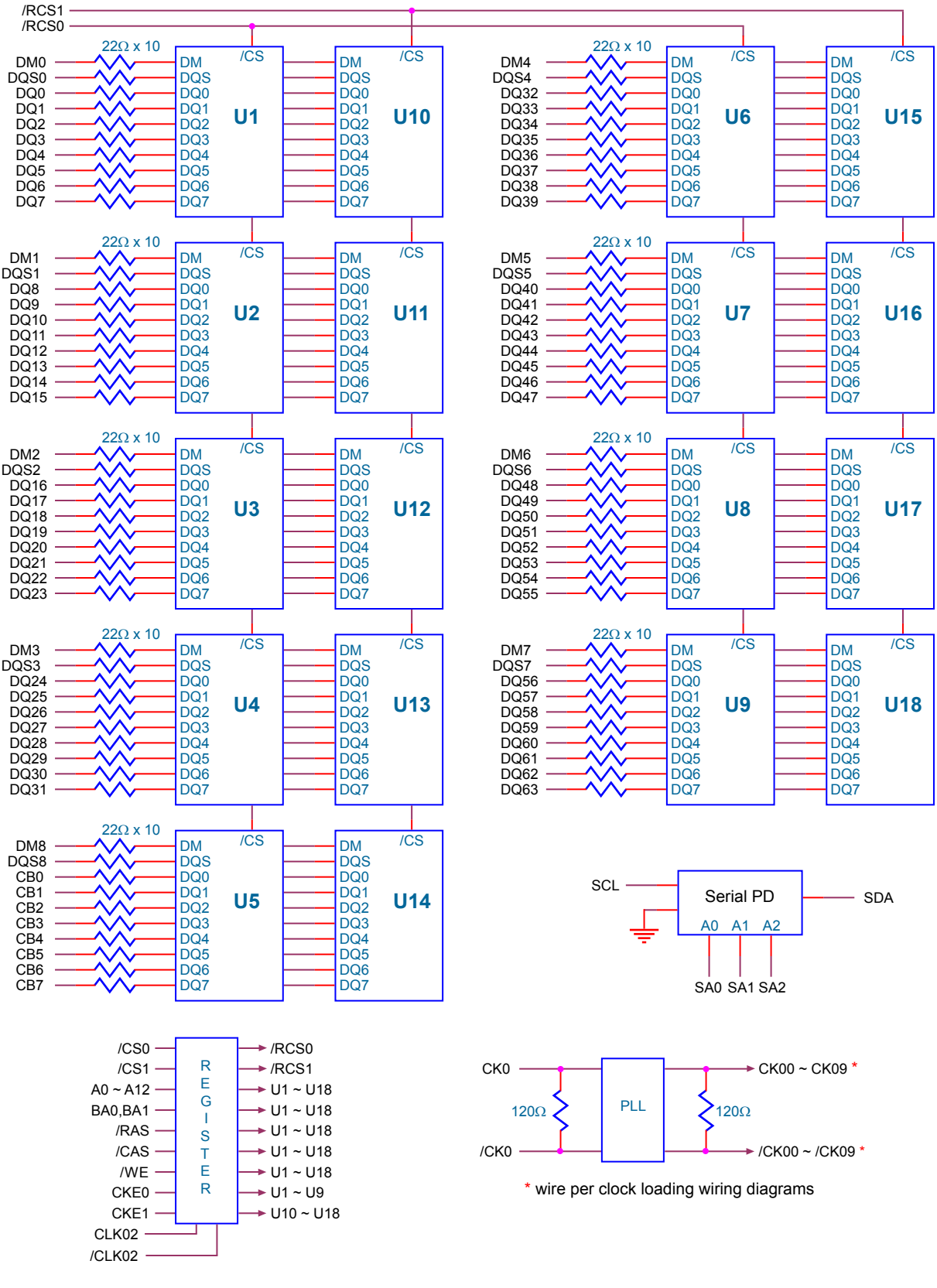
Pin	Front	Pin	Front	Pin	Back	Pin	Back
1	VREF	47	DQS8	93	Vss	139	Vss
2	DQ0	48	A0	94	DQ4	140	DM8
3	Vss	49	CB2	95	DQ5	141	A10
4	DQ1	50	Vss	96	VDDQ	142	CB6
5	DQS0	51	CB3	97	DM0	143	VDDQ
6	DQ2	52	BA1	98	DM6	144	CB7
7	VDD	53	DQ32	99	DQ7	145	Vss
8	DQ3	54	VDDQ	100	Vss	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	/RESET	56	DQS4	102	NC	148	VDD
11	Vss	57	DQ34	103	* A13	149	DM4
12	DQ8	58	Vss	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	Vss
15	VDDQ	61	DQ40	107	DM1	153	DQ44
16	* CK1	62	VDDQ	108	VDD	154	/RAS
17	* /CK1	63	/WE	109	DQ14	155	DQ45
18	Vss	64	DQ41	110	DQ15	156	VDDQ
19	DQ10	65	/CAS	111	CKE1	157	/CS0
20	DQ11	66	Vss	112	VDDQ	158	/CS1
21	CKE0	67	DQS5	113	* BA2	159	DM5
22	VDDQ	68	DQ42	114	DQ20	160	Vss
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	VDD	116	Vss	162	DQ47
25	DQS2	71	* /CS2	117	DQ21	163	* /CS3
26	Vss	72	DO48	118	A11	164	VDDO
27	A9	73	DQ49	119	DM2	165	DQ52
28	DQ18	74	Vss	120	VDD	166	DQ53
29	A7	75	* /CK2	121	DQ22	167	NC
30	VDDQ	76	* CK2	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DM6
32	A5	78	DQS6	124	Vss	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	Vss	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	Vss	127	DQ29	173	NC
36	DQS3	82	VDDID	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DM3	175	DQ61
38	VDD	84	DQ57	130	A3	176	Vss
39	DQ26	85	VDD	131	DQ30	177	DM7
40	DQ27	86	DQS7	132	Vss	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	Vss	88	DQ59	134	CB4	180	VDDQ
43	A1	89	Vss	135	CB5	181	SA0
44	CB0	90	NC	136	VDDQ	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	/CK0	184	VDDSPD

* These pins are not used in this module.

PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 , BA1	Bank select address
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/Data-out)
DQS0 ~ DQS8	Data strobe input/output
DM0 ~ DM8	Data-in mask
CLK0 , /CLK0	Clock input
CKE0 , CKE1	Clock enable input
/CS0 , /CS1	Chip select input
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write enable
VDD	Power supply (2.5V)
VDDQ	Power supply for DQS (2.5V)
Vss	Ground
REGE	Register enable
VREF	Power supply for reference
VDDSPD	Serial EEPROM power supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ SA2	Address in EEPROM
VDDID	VDD identification flag
/RESET	Reset enable
NC	No connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD} , V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	27	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RANTINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD}	2.3	2.7	V	
I/O Supply Voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	0.49 x V_{DDQ}	0.51x V_{DDQ}	V	1
I/O Termination voltage (System)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	4
Input voltage level, CK and /CK inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input differential voltage, CK and /CK inputs	V_{ID}(DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and /CK inputs	V_{IX}(DC)	1.15	1.35	V	5
Input leakage current	I_I	-5	5	µA	
Output leakage current	I_{OZ}	-90	90	µA	
Output high current; V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output low current; V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	

Note : 1. Includes ±25mV margin for DC offset on V_{REF}, and a combined total of ±50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled to V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of 3nH.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on /CK
4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.
5. The value of V_{IX} is expected to equal 0.5×V_{DDQ} of the transmitting device and must track variations in the dc level of the same.
6. These characteristics obey the SSTL-2 class II standards.

I_{DD} SPECIFICATIONS AND CONDITIONS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C) (Note: 1, 2, 3, 4)

Parameter / Conditions	Symbol	Value	Unit
Operating current - One bank Active-Precharge; tRC=tRC(min); DQ,DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	I_{DD0}	TBD	mA
Operating current - One bank operation; tRC = tRC(min); One bank open, BL = 4, Reads, I_{OUT} = 0mA; Address and control inputs changing once per clock cycle	I_{DD1}	TBD	mA
Precharge power-down standby current; All banks idle; power-down mode; CKE V_{IL}(max); V_{IN} = V_{REF} for DQ,DQS and DM	I_{DD2P}	54	mA
Precharge Floating standby current; /CS V_{IH}(min); All banks idle; CKE V_{IH}(min); V_{IN} = V_{REF} for DQ,DQS and DM; Address and other control inputs changing once per clock cycle	I_{DD2F}	630	mA
Precharge Quiet standby current; /CS VIH(min); All banks idle; CKE V_{IH}(min); Address and other control inputs stable with keeping V_{IH}(min) or V_{IL}(max); V_{IN} = V_{REF} for DQ ,DQS and DM	I_{DD2Q}	TBD	mA
Active power-down standby current; One bank active; Power-down mode; CKE V_{IL}(max); V_{IN} = V_{REF} for DQ,DQS and DM	I_{DD3P}	TBD	mA
Active standby current; /CS V_{IH}(min); CKE V_{IH}(min); One bank active; active-precharge; tRC=tRAS(max); DQ, DQS and DM inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{DD3N}	630	mA
Operating current - burst read; Burst length = 2; reads; Continuous burst; One bank active; 50% of data changing at every burst; Address and control inputs changing once per clock cycle; Iout = 0mA	I_{DD4R}	TBD	mA
Operating current - burst write; Burst length = 2; writes; Continuous burst; One bank active; 50% of data changing at every burst; Address and control inputs changing once per clock cycle; DQ, DM and DQS inputs changing twice per clock cycle	I_{DD4W}	TBD	mA
Auto refresh current; tRC = tRFC(min) – 10×tCK; distributed refresh	I_{DD5}	TBD	mA
Self refresh current; CKE 0.2V; External clock tCK = 133Mhz	I_{DD6}	TBD	mA
Operating current - Four bank operation; Four bank interleaving with BL=4; tRC = tRC(min), Burst Mode, Address and control inputs are not changing; Iout = 0mA	I_{DD7}	4200	mA

Note: Module I_{DD} was calculated on the basis of component I_{DD} and can be differently measured according to DQ loading cap.

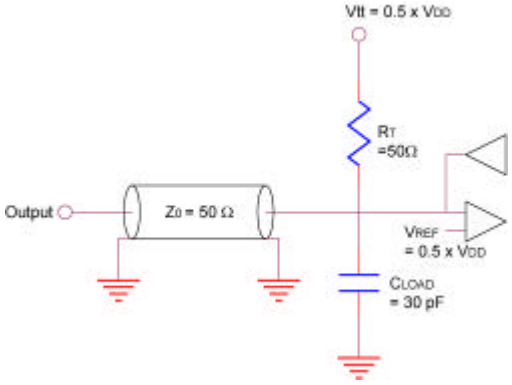
AC OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage, DQ, DQS and DM signals	V_{IH}(AC)	V_{REF} + 0.31		V	3
Input low voltage, DQ, DQS and DM signals	V_{IL}(AC)		V_{REF} - 0.31	V	3
Input differential voltage, CK and /CK inputs	V_{ID}(AC)	0.7	V_{DDQ} + 0.6	V	1
Input crossing point voltage, CK and /CK inputs	V_{IX}(AC)	0.5×V_{DDQ} - 0.2	0.5×V_{DDQ} + 0.2	V	2

Note : 1. V_{ID} is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of V_{IX} is expected to equal 0.5×V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are refer to a V_{REF} envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (V_{DD} = 2.5V, V_{DDQ} = 2.5V, T_A = 0 to 70°C)

Parameter	Value	Unit
Input reference voltage for Clock	0.5 × V_{DD}	V
Input signal maximum peak swing	1.5	V
Input Levels (V_{IH}/V_{IL})	(V_{REF}+0.31) / (V_{REF}-0.31)	V
Input timing measurement reference level	V_{REF}	V
Output timing measurement reference level	V_{TT}	V
Output load condition	See Load Circuit	



Output Load Circuit (SSTL_2)

CAPACITANCE (V_{DD} = 2.5V, V_{DDQ} = 2.5V, T_A = 25°C, f = 1MHz)

Pin	Symbol	Max	Unit
A0 ~ A12, BA0 ~ BA1, /RAS, /CAS, /WE	C_{IN1}	12	pF
CKE0 , CKE1	C_{IN2}	12	pF
/CS0 , /CS1	C_{IN3}	11	pF
CLK0 , /CLK0	C_{IN4}	12	pF
DM0 ~ DM8	C_{IN5}	16	pF
DQ0 ~ DQ63	C_{OUT1}	16	pF
CB0 ~ CB7	C_{OUT2}	16	pF

AC TIMMING PARAMETERS AND SPECIFICATIONS
(These AC characteristics were tested on the component)

Parameter		Symbol	Min	Max	Unit	Note
Row cycle time		tRC	65	-	ns	
Refresh row cycle time		tRFC	75	-	ns	
Row active time		tRAS	40	120K	ns	
/RAS to /CAS delay		tRCD	20		ns	
Row precharge time		tRP	20		ns	5
Row active to Row active delay		tRRD	15		ns	5
Write recovery time		tWR	15		ns	
Last data in to Read command		tCDLR	1		tCK	
Column address to Column address delay		tCCD	1		tCK	
Clock cycle time	CL = 2.5	tCK	7.5	12	ns	5
	CL = 2.0		10	13		
Clock high level width		tCH	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	tCK	
DQS-out access time from CK, /CK		tDQSCK	-0.75	+0.75	ns	
Output data access time from CK, /CK		tAC	-0.75	+0.75	ns	
Data strobe edge to output data edge		tDQSQ	-	0.5	ns	
Read Preamble		tRPRE	0.9	1.1	tCK	
Read Post amble		tRPST	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		ns	2
DQS-in hold time		tWPREH	0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		tCK	
DQS-in high level width		tDQSH	0.35		tCK	
DQS-in low level width		tDQSL	0.35		tCK	
DQS-in cycle time		tDSC	0.9	1.1	tCK	
Address and Control Input setup time (fast)		tIS	0.9		ns	6
Address and Control Input hold time (fast)		tIH	0.9		ns	6
Address and Control Input setup time (slow)		tIS	1.0		ns	6
Address and Control Input hold time (slow)		tIH	1.0		ns	6
Data-out high impedance time from CK, /CK		tHZ	-0.75	+0.75	ps	
Data-out low impedance time from CK, /CK		tLZ	-0.75	+0.75	ps	
Input Slew Rate (for input only pins)		tSL(I)	0.5		V/ns	6
Input Slew Rate (for I/O pins)		tSL(IO)	0.5		V/ns	7
Output Slew Rate (x8)		tSL(O)	1.0	4.5	V/ns	10

AC TIMMING PARAMETERS AND SPECIFICATIONS (continues)

Parameter	Symbol	Min	Max	Unit	Note
Output Slew Rate Matching Ratio (rise to fall)	tSLMR	0.67	1.5		
Mode register set cycle time	tMRD	15		ns	
DQ & DM setup time to DQS	tDS	0.5		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.5		ns	7,8,9
Control & Address input pulse width	tIPW	2.2		ns	
DQ & DM input pulse width	tDIPW	1.75		ns	
Power down exit time	tPDEX	7.5		ns	
Exit self refresh to non-read command	tXSNR	75		ns	4
Exit self refresh to read command	tXSRD	200		tCK	
Refresh interval time	tREFI	7.8		us	1
Output DQS valid window	tQH	tHPmin - tQHS		ns	5
Clock half period	tHP	tCLmin or tCHmin		ns	
Data hold skew factor	tQHS		0.75	ns	
DQS write post amble time	tWPST	0.4	0.6	tCK	3

Note : 1. Maximum burst refresh cycle : 8

2. The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with tRCD satisfied after this command.
5. For registered DINNs, tCL and tCH are ≥ 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to cross talk (tJIT(crosstalk)) on the DIMM.
6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate (V/ns)	ΔtIS (ps)	ΔtIH (ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase tIS /tIH in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate (V/ns)	ΔtIS (ps)	ΔTih (ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase tDS /tDH in the case where the I/O slew rate is below0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level (mV)	ΔtIS (ps)	ΔtIH (ps)
±280	+50	+50

This derating table is used to increase tDS /tDH in the case where the input level is flat below VREF ± 310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate (ns/V)	ΔtIS (ps)	ΔtIH (ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is collated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5 V/ns and slew rate 2 = 4 V/ns then the Delta Rise/Fall Rate = -0.05 ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guaranteed by design.

COMMAND TRUTH TABLE

(V = Valid, X = Don't Care, H = Logic High, L = Logic Low)

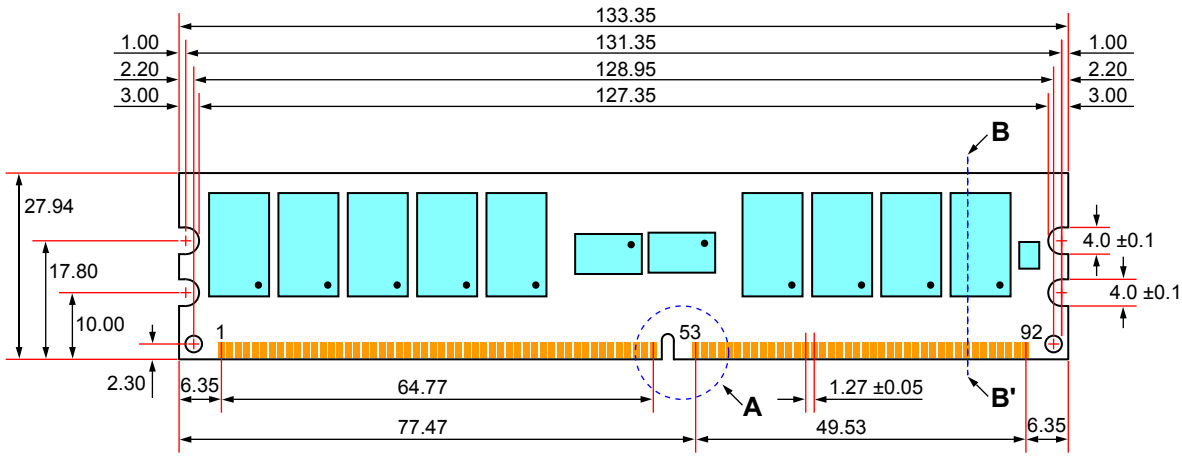
Command			CKE_{n-1}	CKE_n	/CS	/RAS	/CAS	/WE	$BA_{0,1}$	A_{10}/AP	A12,A_{11} A_9~A_0	Note
Register	Extended MRS		H	X	L	L	L	L	OP code			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP code			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Address			H	X	L	L	H	H	V	Row address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column address (A_0~A_9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column address (A_0~A_9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

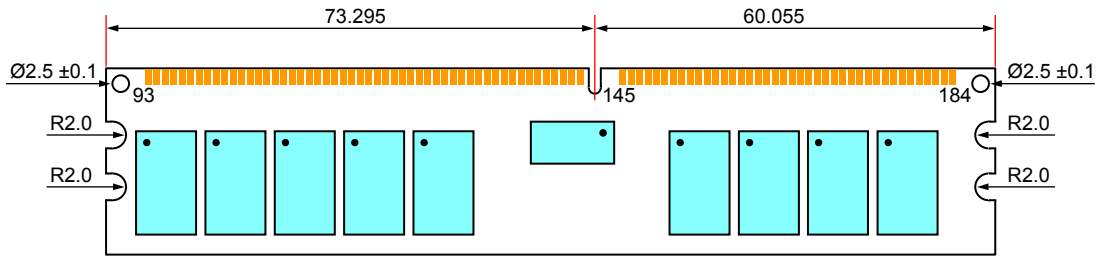
Note : 1. OP Code : Operand Code. A_0 ~ A_{12} & BA_0 ~ BA_1 : Program keys. (@EMRS/MRS)

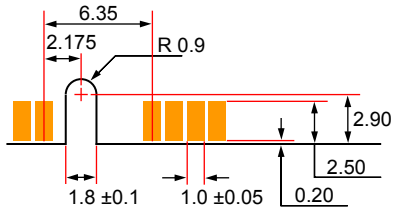
2. EMRS/ MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatically precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation (NOP)" in DDR SDRAM.

PACKAGE DIMENSIONS

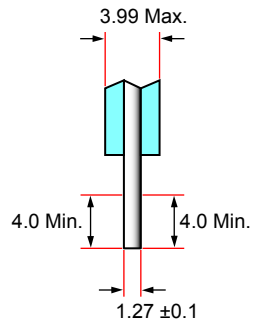
Units: Millimeter







Detail A



Section B-B'

Tolerance : ±0.15 unless otherwise specified

The used device is 32Mx8 DDR SDRAM TinyBGA