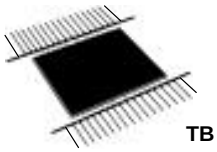
MCM101524

Product Preview

1M x 4 Bit Fast Static Random Access Memory with ECL I/O



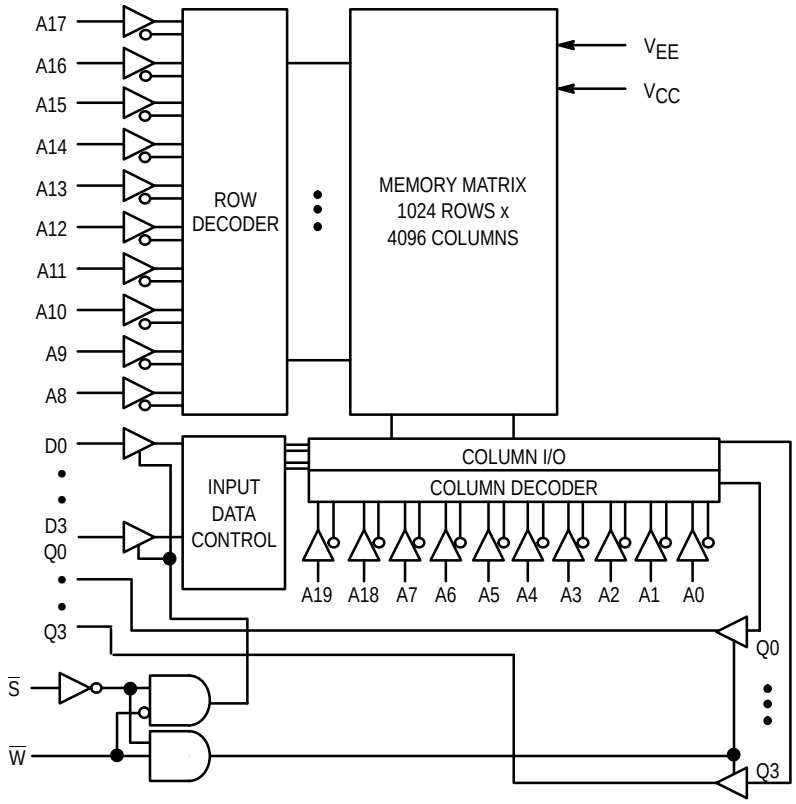
TB PACKAGE
400 MIL TAB
CASE 984A–01

The MCM101524 is a 4,194,304 bit static random access memory organized as 1,048,576 words of 4 bits. This circuit is fabricated using high performance silicon–gate BiCMOS technology. Asynchronous design eliminates the need for external clocks or timing strobes.

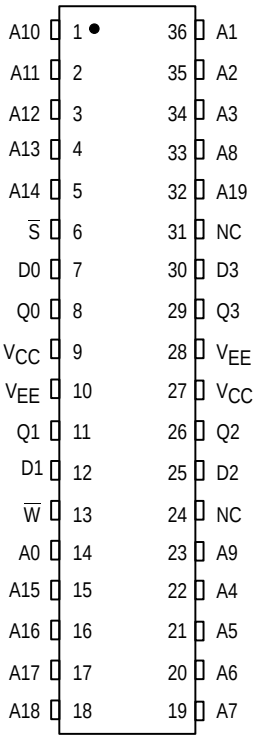
The MCM101524 is available in a 400 mil, 36 lead TAB.

- Fast Access Times: 12, 15 ns
- Equal Address and Chip Select Access Times
- Power Operation: – 195 mA Maximum, Active AC

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0 – A19 . . . . . Address Inputs	W . . . . . Write Enable
S . . . . . Chip Select	D0 – D3 . . . . . Data Input
Q0 – Q3 . . . . . Data Output	NC . . . . . No Connection
V_{EE} . . . . . Power Supply	V_{CC} . . . . . Ground

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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TRUTH TABLE (X = Don't Care)

$\overline{S}$	$\overline{W}$	Operation	Data	Output	Current
H	X	Not Enabled	X	L	—
L	H	Read	X	Q	I_{EE}
L	L	Write	X	L	I_{EE}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential (to Ground)	V_{EE}	– 7.0 to + 0.5	V
Voltage Relative to V_{CC} for Any Pin Except V_{EE}	V_{in}, V_{out}	V_{EE} – 0.5 to + 0.5	V
Output Current (per I/O)	I_{out}	– 50	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 30 to + 85	°C
Operating Temperature	T_J	0 to + 60	°C
Storage Temperature — Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = – 5.2 V ± 5%, T_J = 0 to + 60°C, Unless Otherwise Noted)

DC OPERATING CONDITIONS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{EE}	– 5.46	– 5.2	– 4.94	V
Input High Voltage	V_{IH}	– 1165	—	– 880	mV
Input Low Voltage	V_{IL}	– 1810	—	– 1475	mV
Output High Voltage	V_{OH}	– 1025	—	– 880	mV
Output Low Voltage	V_{OL}	– 1810	—	– 1620	mV
Input Low Current	I_{IL}	– 50	—	—	µA
Input High Current	I_{IH}	—	—	220	µA
Chip Select Input Low Current	$I_{IL(CS)}$	0.5	—	170	µA
Operating Power Supply Current: ^tAVAV = 20 ns (All Outputs Open)*	I_{EE}	—	—	– 195	mA
Quiescent Power Supply Current: f_o = 0 MHz (Outputs Open)	I_{EEQ}	—	—	– 150	mA
Voltage Compensation (V_{OH})	$\Delta V_{OH}/\Delta V_{EE}$	± 35 mV/V @ – 4.94 to – 5.46 V			
Voltage Compensation (V_{OL})	$\Delta V_{OL}/\Delta V_{EE}$	± 60 mV/V @ – 4.94 to – 5.46 V			

* Address Increment

RISE/FALL TIME CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise Time	t_r	20% to 80%	0.5	1.0	1.5	ns
Output Fall Time	t_f	20% to 80%	0.5	1.0	1.5	ns

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	Address and Data $\overline{S}$, $\overline{W}$	C_{in} C_{ck}	3.5 4	7 7	pF
Output Capacitance	Q	C_{out}	4	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{EE} = – 5.2 V ± 5%, V_{CC} = 0 V, T_J = 0 to +60°C, Unless Otherwise Noted)

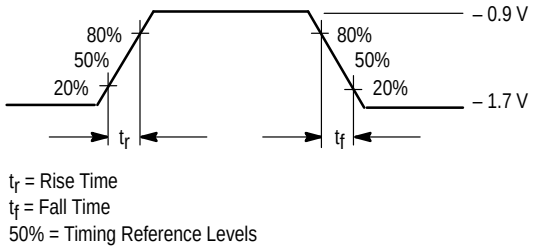
Input Pulse Levels . . . . . – 1.7 V to – 0.9 V (See Figure 1)
Input Rise/Fall Time . . . . . 1 ns
Input Timing Measurement Reference Level 50%
Output Timing Measurement Reference Level . . V_{OH} = – 1165 mV
V_{OL} = – 1475 mV
Output Load (AC Test Circuit) . . . . . See Figure 2

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	MCM101524–12		MCM101524–15		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	12	—	15	—	ns	2, 3
Address Access Time	t_{AVQV}	—	12	—	15	ns	
Chip Select Access Time	t_{SLQV}	—	12	—	15	ns	6
Select High to Output Low	t_{SHQL}	0	8	0	9	ns	
Output Hold from Address Change	t_{AXQX}	4	—	4	—	ns	
Power Up Time	t_{SLIEEH}	0	—	0	—	ns	4
Power Down Time	t_{SHIEEL}	—	12	—	15	ns	4

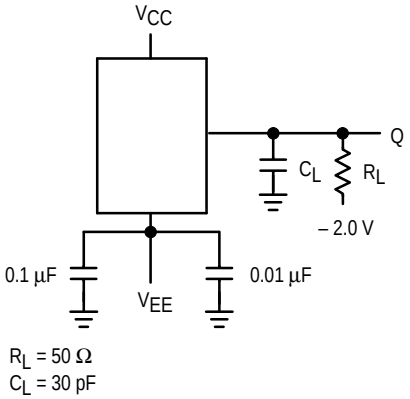
NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.
5. Device is continuously selected ($\overline{S} \le V_{IL}$).
6. Addresses valid prior to or coincident with $\overline{S}$ going low.

AC TEST CONDITIONS



t_r = Rise Time
t_f = Fall Time
50% = Timing Reference Levels

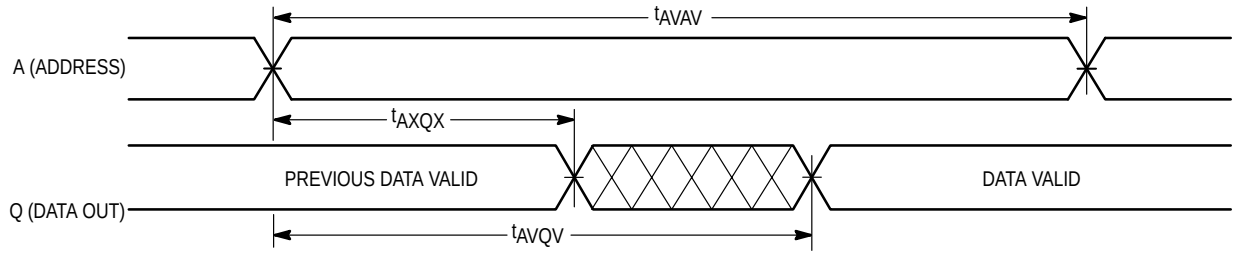
Figure 1. Input Levels



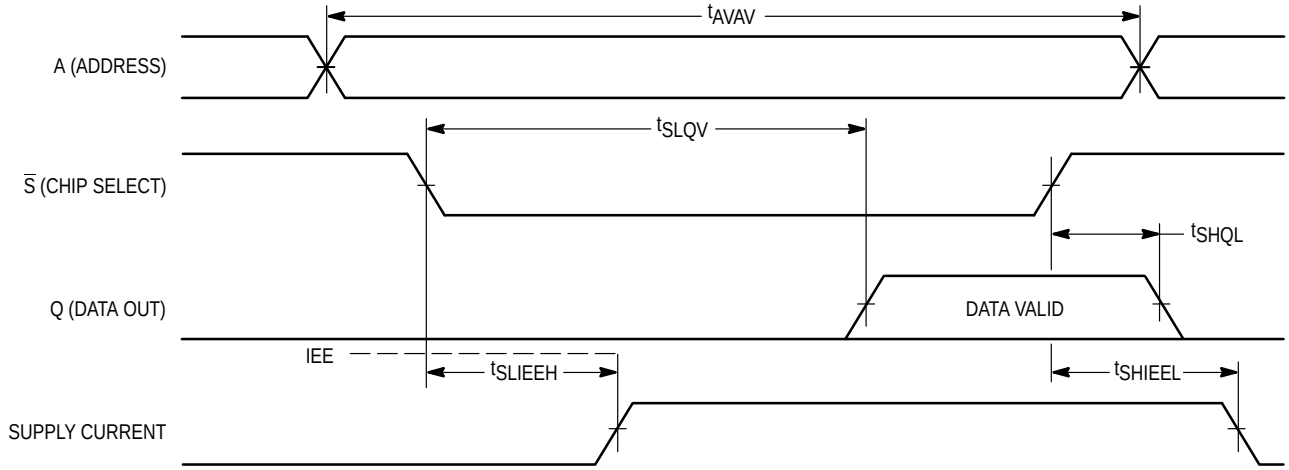
R_L = 50 Ω
C_L = 30 pF

Figure 2. AC Test Circuit

READ CYCLE 1 (See Notes 1, 2, and 5)



READ CYCLE 2 (See Note 6)

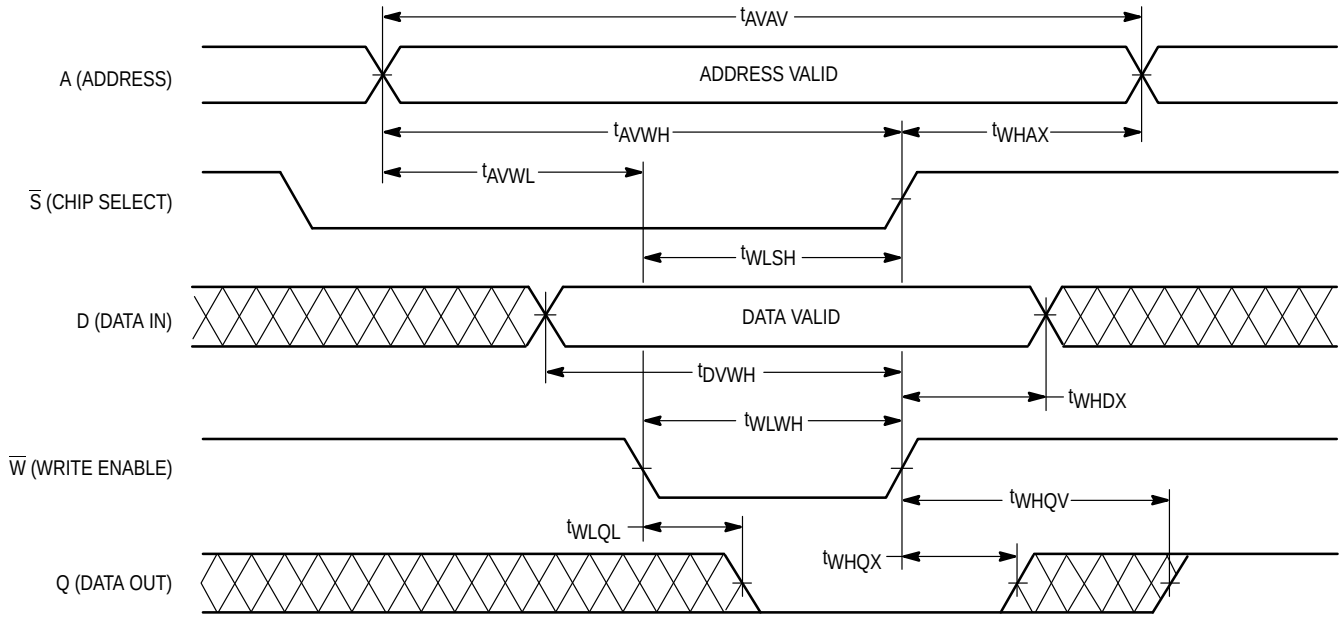


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM101524–12		MCM101524–15		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	1	—	1	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLSH}	8	—	9	—	ns	
Data Valid to End of Write	t_{DVWH}	8	—	9	—	ns	
Data Hold Time	t_{WHDX}	1	—	1	—	ns	
Write High to Output Active	t_{WHQX}	4	—	4	—	ns	4
Write High to Output Valid	t_{WHQV}	—	13	—	16	ns	
Write Recovery Time	t_{WHAX}	1	—	1	—	ns	
Write Low to Output Low	t_{WLQL}	0	8	0	9	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. This parameter is sampled and not 100% tested.

WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

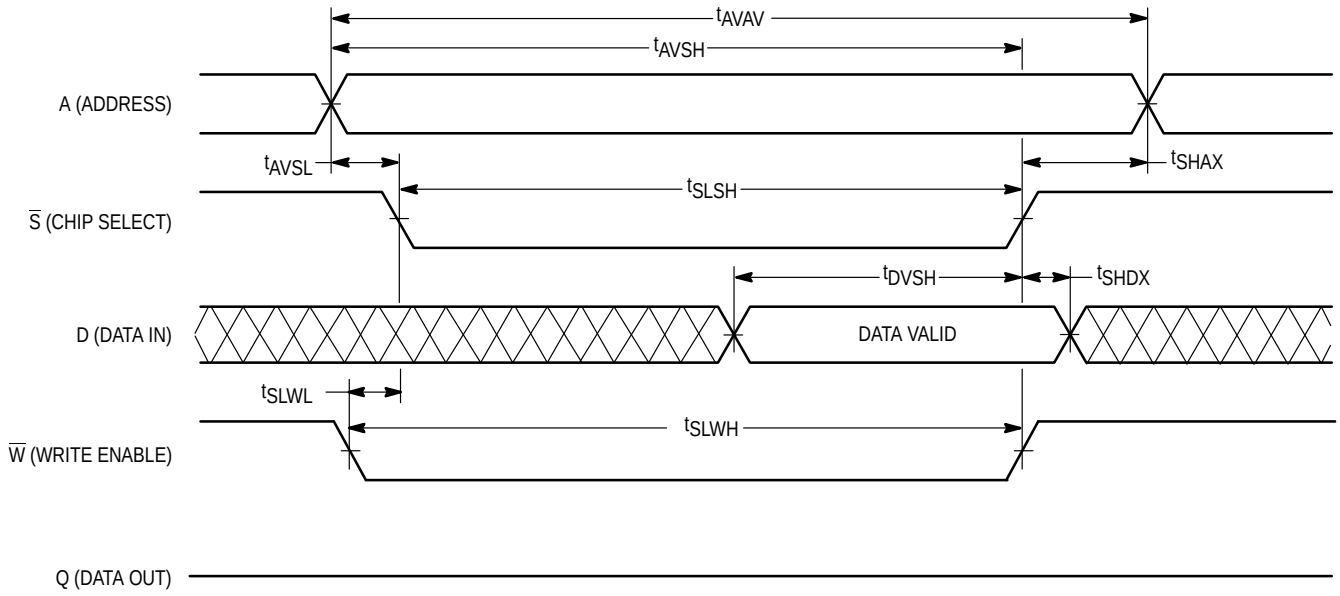


WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)

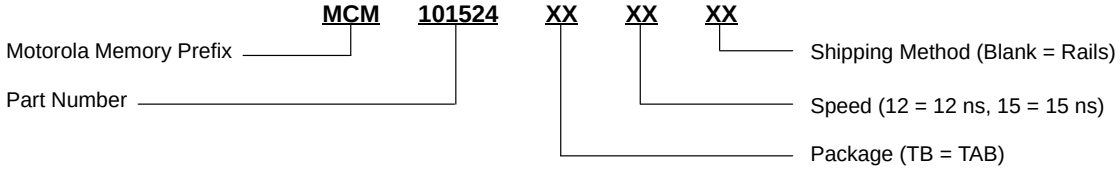
Parameter	Symbol	MCM101524–12		MCM101524–15		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	12	—	15	—	ns	3
Address Setup Time	t_{AVSL}	1	—	1	—	ns	
Address Valid to End of Write	t_{AVSH}	9	—	10	—	ns	
Write Pulse Width ($\overline{S}$) / ($\overline{W}$)	t_{SLSH} / t_{SLWH}	8	—	9	—	ns	
Data Valid to End of Write	t_{DVSH}	8	—	9	—	ns	
Chip Select Set–Up Time	t_{SLWL}	0	—	0	—	ns	
Data Hold Time	t_{SHDX}	1	—	1	—	ns	
Write Recovery Time	t_{SHAX}	1	—	1	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.

WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2)



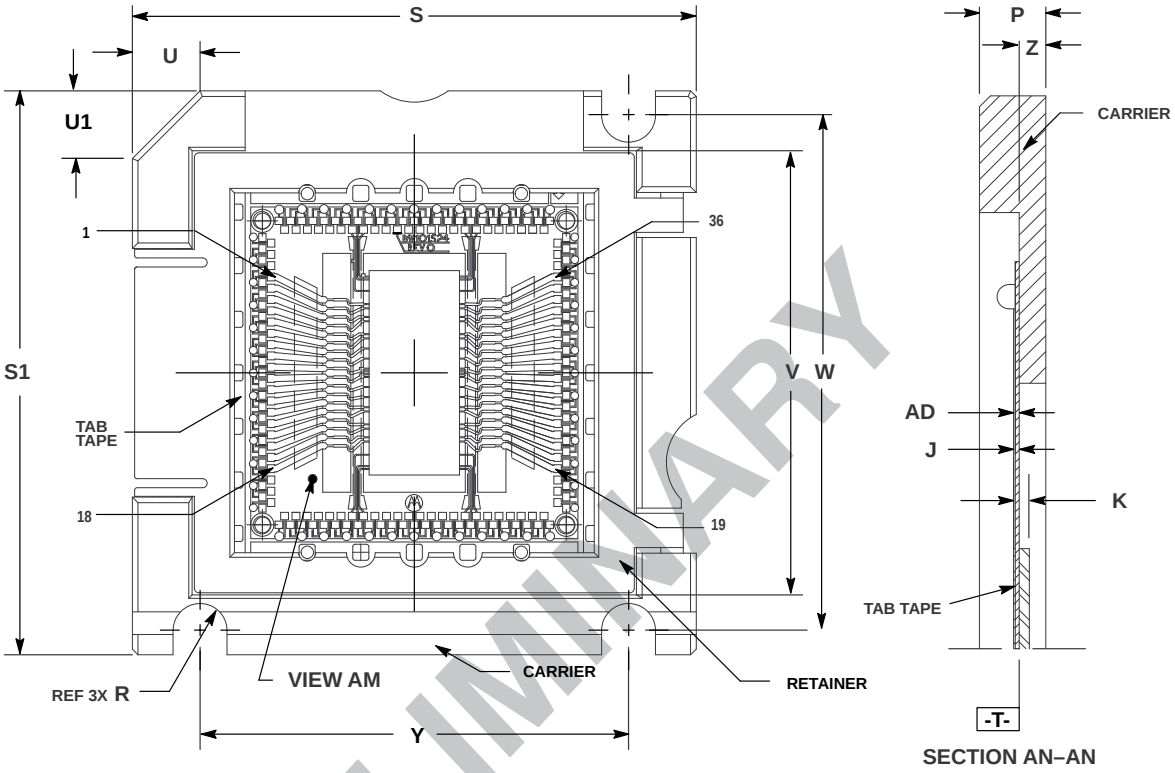
ORDERING INFORMATION
(Order by Full Part Number)

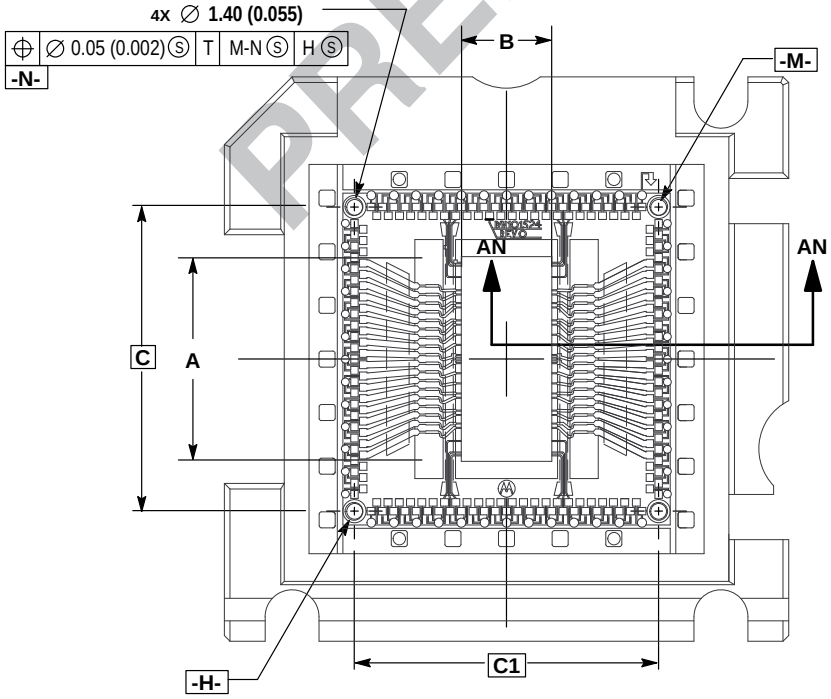


Full Part Numbers — MCM101524TB12
MCM101524TB15

PACKAGE DIMENSIONS

TB PACKAGE
400 MIL TAB
CASE 984A–01



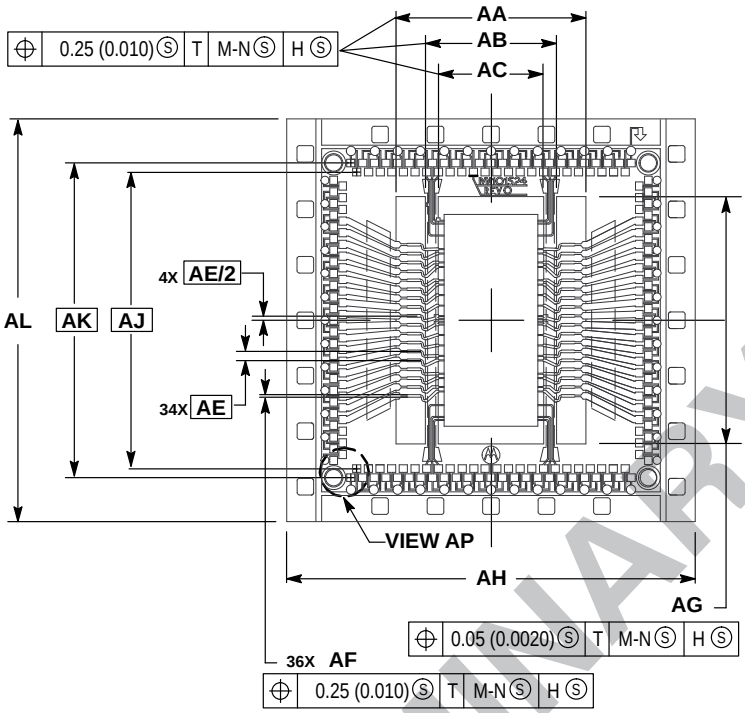


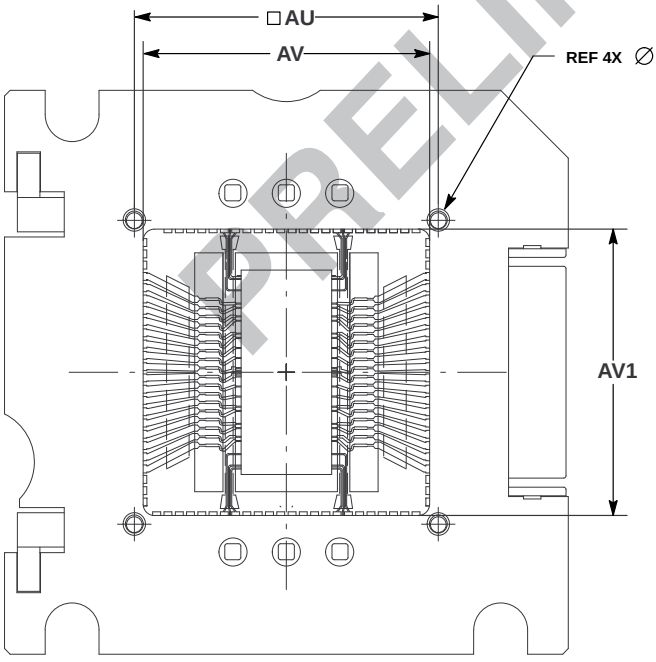
VIEW AM
TAPE CARRIER RETAINER ELIMINATED FROM VIEW FOR CLARITY

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

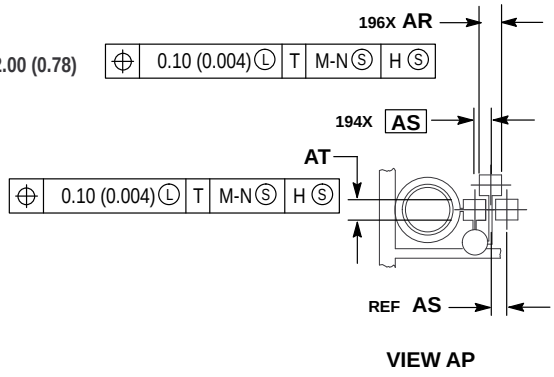
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.14 REF		0.714 REF	
B	8.03 REF		0.316 REF	
C	26.95 BSC		1.061 BSC	
C1	26.95 BSC		1.061 BSC	
J	—	0.25	—	0.010
K	—	0.71	—	0.028
P	3.00 REF		0.118 REF	
R	2.39 REF		0.094 REF	
S	50.00 REF		1.969 REF	
S1	50.00 REF		1.969 REF	
U	6.00 REF		0.236 REF	
U1	6.00 REF		0.236 REF	
V	39.40 REF		1.551 REF	
W	45.68 REF		1.798 REF	
Y	38.00 REF		1.496 REF	
Z	1.15	1.25	0.045	0.049
AA	16.21	16.31	0.638	0.642
AB	11.20	11.30	0.441	0.445
AC	8.99	9.09	0.354	0.358
AD	0.15	0.21	0.006	0.008
AE	0.762 BSC		0.030 BSC	
AF	0.18	0.28	0.007	0.011
AG	21.31	21.24	0.832	0.836
AH	35.00 REF		1.378 REF	
AJ	25.40 REF		1.000 REF	
AK	26.95 BSC		1.061 BSC	
AL	34.98 REF		1.377 REF	
AR	0.65	0.75	0.026	0.030
AS	0.50 BSC		0.020 BSC	
AT	0.60	0.70	0.024	0.028
AU	26.95 REF		1.061 REF	
AV	25.35	25.45	0.998	1.002
AV1	25.35	25.45	0.998	1.002

TB PACKAGE
400 MIL TAB
CASE 984A–01 (cont.)





BOTTOM VIEW



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