THAT Corporation

Quad Low-Noise NPN / PNP Transistor Array

THAT140

FEATURES

- Two Matched NPN Transistors
  Two Matched PNP Transistors
- Monolithic Construction
- Low Noise
  - 0.75 $nV/\sqrt{Hz}$ (PNP)
  - 0.8 $nV/\sqrt{Hz}$ (NPN)
- High Speed
  - f_t= 350 MHz (NPN)
  - f_t= 325 MHz (PNP)
- Excellent Matching - 500 µV typ
- Dielectrically Isolated
- 25 V V_{CEO}

APPLICATIONS

- Microphone Preamplifiers
- Tape Head Preamplifiers
- Current Sources
- Current Mirrors
- Log/Antilog Amplifiers
- Multipliers

DESCRIPTION

THAT140 is a quad, large-geometry monolithic NPN/PNP transistor array which combines low noise, high speed and excellent parametric matching. The large geometries typically result in 25 Ω base spreading resistance for the PNP devices (30 Ω for the NPNs), producing 0.75 $nV/\sqrt{Hz}$ voltage noise (0.8 $nV/\sqrt{Hz}$ for the NPNs). This makes these parts an ideal choice for low-noise amplifier input stages.

Fabricated on a Complementary Bipolar Dielectrically Isolated process, all four transistors are electrically isolated from each other by a layer of oxide. The resulting low collector-to-substrate capacitance produces a typical NPN f_t of 350 MHz, 325 Mhz for the PNPs. This delivers AC performance similar to discrete 2N3904- and 2N3906-class devices. Dielectric isolation also minimizes crosstalk and provides complete DC isolation.

Substrate biasing is not required for normal operation, though the substrate should be grounded to optimize speed. The monolithic construction assures excellent parameter matching and tracking over temperature.

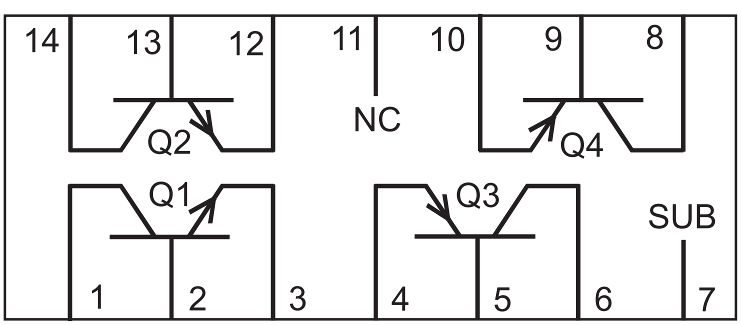

Figure 1. Pin Configuration

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SPECIFICATIONS[1]

Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
NPN Collector-Emitter Voltage	BV_{CEO}	I_C = 1 mAdc, I_B = 0	25	35	—	V
NPN Collector-Base Voltage	BV_{CBO}	I_C = 10 μAdc, I_E = 0	25	35	—	V
NPN Emitter-Base Voltage	BV_{EBO}	I_E = 10 μAdc, I_C = 0	5	—	—	V
NPN Collector Current	I_C		10	20		mA
NPN Emitter Current	I_E		10	20		mA
PNP Collector-Emitter Voltage	BV_{CEO}	I_C = 1 mAdc, I_B = 0	-25	-40	—	V
PNP Collector-Base Voltage	BV_{CBO}	I_C = 10 μAdc, I_E = 0	-25	-40	—	V
PNP Emitter-Base Voltage	BV_{EBO}	I_E = 10 μAdc, I_C = 0	-5	—	—	V
PNP Collector Current	I_C		-10	-20		mA
PNP Emitter Current	I_E		-10	-20		mA
Collector-Collector Voltage	BV_{CC}		±100	±200	—	V
Emitter-Emitter Voltage	BV_{EE}		±100	±200	—	V
Operating Temperature Range	T_A		0		70	°C
Maximum Junction Temperature	T_{JMAX}				150	°C
Storage Temperature	T_{STORE}		-45		125	°C

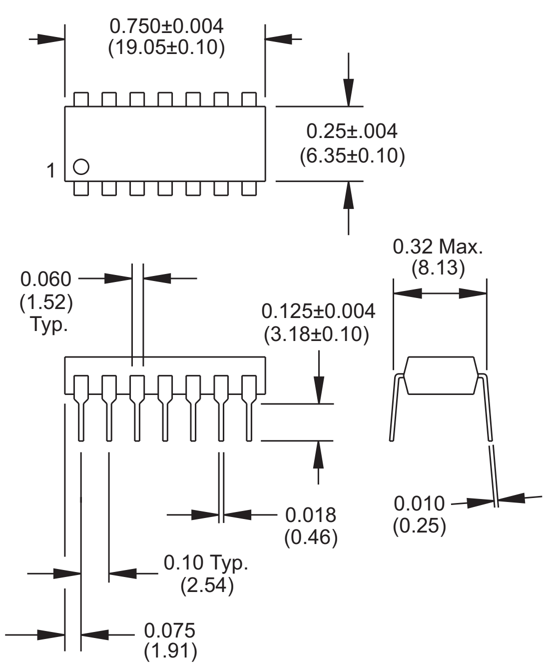

Figure 2. Dual-In-Line Package Outline

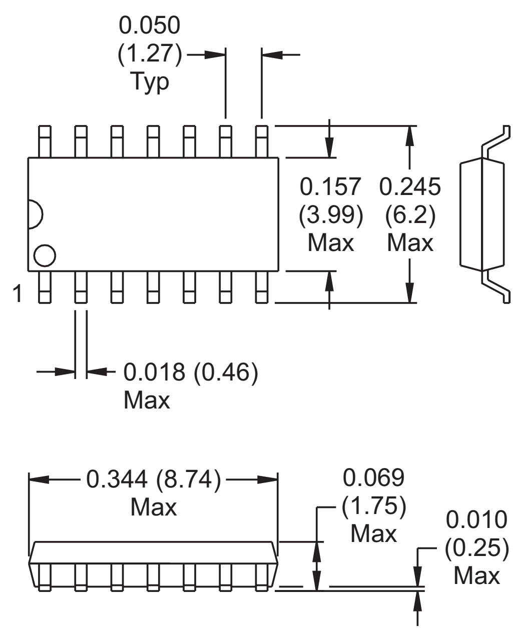

Figure 3. Surface Mount Package Outline

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Electrical Characteristics[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
NPN Current Gain	h_{fe}	V_{CB} = 10 V				
		I_C = 1 mA	60	100	—	
		I_C = 10 µA	60	100	—	
NPN Current Gain Matching	Δh_{fe}	V_{CB} = 10 V, I_C = 1 mA	—	5	—	%
NPN Noise Voltage Density	e_N	V_{CB} = 10 V, I_C = 1 mA, 1 kHz	—	0.8	—	nV / $\sqrt{Hz}$
NPN Gain-Bandwidth Product	f_t	I_C = 1 mA, V_{CB} = 10 V		350		MHz
NPN ΔV_{BE} (V_{BE1}-V_{BE2})	V_{OS}	I_C = 1 mA	—	±0.5	±3	mV
		I_C = 10 µA	—	±0.5	±3	mV
NPN ΔI_B (I_{B1}-I_{B2})	I_{OS}	I_C = 1 mA	—	±500	±1500	nA
		I_C = 10 µA	—	±5	±15	nA
NPN Collector-Base Leakage Current	I_{CBO}	V_{CB} = 25 V	—	25	—	pA
NPN Bulk Resistance	r_{BE}	V_{CB} = 0 V, 10µA < I_C < 10mA	—	2	—	Ω
NPN Base Spreading Resistance	r_{bb}	V_{CB} = 10 V, I_C = 1mA	—	30	—	Ω
NPN Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100 µA	—	0.05		V
NPN Output Capacitance	C_{OB}	V_{CB} = 10 V, I_E = 0 mA, 100 kHz		3		pF
NPN Collector-Collector Capacitance (Q_1-Q_2)	C_{CC}	V_{CC} = 0 V, 100 kHz		0.7		pF
PNP Current Gain	h_{fe}	V_{CB} = 10 V				
		I_C = 1 mA	50	75	—	
		I_C = 10 µA	50	75	—	
PNP Current Gain Matching	Δh_{fe}	V_{CB} = 10 V, I_C = 1 mA	—	5	—	%
PNP Noise Voltage Density	e_N	V_{CB} = 10 V, I_C = 1 mA, 1 kHz	—	0.75	—	nV / $\sqrt{Hz}$
PNP Gain-Bandwidth Product	f_t	I_C = 1 mA, V_{CB} = 10 V		325		MHz
PNP ΔV_{BE} (V_{BE3}-V_{BE4})	V_{OS}	I_C = 1 mA	—	±0.5	±3	mV
		I_C = 10 µA	—	±0.5	±3	mV
PNP ΔI_B (I_{B3}-I_{B4})	I_{OS}	I_C = 1 mA	—	±700	±1800	nA
		I_C = 10 µA	—	±7	±18	nA
PNP Collector-Base Leakage Current	I_{CBO}	V_{CB} = 25 V	—	-25	—	pA
PNP Bulk Resistance	r_{BE}	V_{CB} = 0 V, 10µA < I_C < 10mA	—	2	—	Ω
PNP Base Spreading Resistance	r_{bb}	V_{CB} = 10 V, I_C = 1mA	—	25	—	Ω
PNP Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100 µA	—	-0.05		V
PNP Output Capacitance	C_{OB}	V_{CB} = 10 V, I_E = 0 mA, 100 kHz		3		pF
PNP Collector-Collector Capacitance (Q_3-Q_4)	C_{CC}	V_{CC} = 0 V, 100 kHz		0.6		pF

1. All specifications subject to change without notice.
2. Unless otherwise noted, T_A=25°C.

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Notes

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