N-Channel Enhancement Mode MOSFET Switch

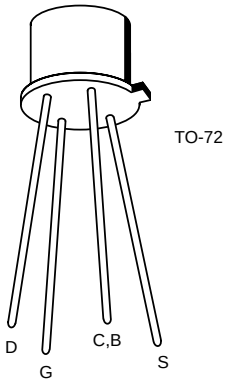
calogic CORPORATION

3N170 / 3N171

FEATURES

- **Low Switching Voltages**
- **Fast Switching Times**
- **Low Drain-Source Resistance**
- **Low Reverse Transfer Capacitance**

PIN CONFIGURATION



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HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow the procedures outlined below.

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on as transient voltages may cause permanent damage to the devices.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)

Drain-Gate Voltage	±35V
Drain-Source Voltage	25V
Gate-Source Voltage	±35V
Drain Current	30mA
Storage Temperature Range	-65°C to +200°C
Operating Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation	300mW
Derate above 25°C	2.4mW/°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Part	Package	Temperature Range
3N170-71	Hermetic TO-72	-55°C to +150°C
X3N170-71	Sorted Chips in Carriers	-55°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) Substrate connected to source.

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-Source Breakdown Voltage		25		V	I_D = 10µA, V_{GS} = 0
I_{GSS}	Gate Leakage Current			±10	pA	V_{GS} = ±35V, V_{DS} = 0
				100		V_{GS} = 35V, V_{DS} = 0, T_A = 125°C
I_{DSS}	Zero-Gate-Voltage Drain Current			10	nA	V_{DS} = 10V, V_{GS} = 0
				1.0	µA	T_A = 125°C
$V_{GS(th)}$	Gate-Source Threshold Voltage	3N170	1.0	2.0	V	V_{DS} = 10V, I_D = 10µA
		3N171	1.5	3.0		
$I_{D(on)}$	"ON" Drain Current		10		mA	V_{GS} = 10V, V_{DS} = 10V
$V_{DS(on)}$	Drain-Source "ON" Voltage			2.0	V	I_D = 10mA, V_{GS} = 10V
$r_{ds(on)}$	Drain-Source ON Resistance			200	Ω	V_{GS} = 10V, I_D = 0, f = 1kHz
$\lvert Y_{fs} \rvert$	Forward Transfer Admittance		1000		µS	V_{DS} = 10V, I_D = 2.0mA, f = 1kHz
C_{rss}	Reverse Transfer Capacitance (Note 1)			1.3	pF	V_{DS} = 0, V_{GS} = 0, f = 1MHz
C_{iss}	Input Capacitance (Note 1)			5.0		V_{DS} = 10V, V_{GS} = 0, f = 1MHz
$C_{d(sub)}$	Drain-Substrate Capacitance (Note 1)			5.0		$V_{D(SUB)}$ = 10V, f = 1MHz
$t_{d(on)}$	Turn-On Delay Time (Note 1)			3.0	ns	VDD = 10V, $I_{D(on)}$ = 10mA, $V_{GS(on)}$ = 10V, $V_{GS(off)}$ = 0, R_G = 50Ω
t_r	Rise Time (Note 1)			10		
$t_{d(off)}$	Turn-Off Delay Time (Note 1)			3.0		
t_f	Fall Time (Note 1)			15		

NOTE 1: For design reference only, not 100% tested.