

TO-252



Pin Definition:

1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
500	2.7 @ $V_{GS}=10V$	1.5

General Description

The TSM4ND50 N-Channel enhancement mode Power MOSFET is produced by planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

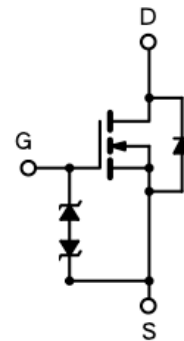
Features

- Low gate charge typical @ 12nC
- Low Crss typical @ 10pF
- Fast Switching
- 100% avalanche tested
- Improved dv/dt capability
- ESD Protection

Ordering Information

Part No.	Package	Packing
TSM4ND50CP RO	TO-252	2,500pcs / 13" Reel

Block Diagram



N-Channel MOSFET

Absolute Maximum Rating (Ta=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	3	A
Pulsed Drain Current	I_{DM}	12	A
Continuous Source Current (Diode Conduction)	I_S	3	A
Peak Diode Recovery (Note 2)	dv/dt	4.5	V/ns
Single Pulse Drain to Source Avalanche Energy (Note 3)	E_{AS}	120	mJ
Total Power Dissipation @ $T_C=25^\circ C$	P_{DTOT}	45	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R_{\theta_{JC}}$	2.78	$^\circ C/W$
Thermal Resistance - Junction to Ambient	$R_{\theta_{JA}}$	100	$^\circ C/W$

Notes: Surface mounted on FR4 board $t \leq 10sec$

Electrical Specifications ($T_a = 25^\circ\text{C}$ unless otherwise noted)

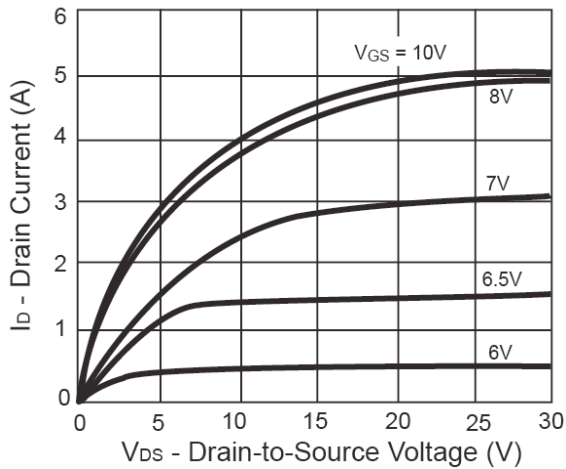
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	500	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 1.5A$	$R_{DS(ON)}$	--	2.3	2.7	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	3.0	--	4.5	V
Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 10	μA
Forward Transconductance	$V_{DS} = 15V, I_D = 1.5A$	g_{fs}	--	1.5	--	S
Dynamic^b						
Total Gate Charge	$V_{DS} = 400V, I_D = 3A,$ $V_{GS} = 10V$	Q_g	--	12	--	nC
Gate-Source Charge		Q_{gs}	--	3.4	--	
Gate-Drain Charge		Q_{gd}	--	6.4	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	310	--	pF
Output Capacitance		C_{oss}	--	49	--	
Reverse Transfer Capacitance		C_{rss}	--	10	--	
Switching^c						
Turn-On Delay Time	$V_{GS} = 10V, I_D = 1.5A,$ $V_{DD} = 250V, R_G = 4.7\Omega$	$t_{d(on)}$	--	22	--	ns
Turn-On Rise Time		t_r	--	9	--	
Turn-Off Delay Time		$t_{d(off)}$	--	9	--	
Turn-Off Fall Time		t_f	--	4.5	--	
Source Drain Diode						
Source Drain Current		I_{SD}	--	--	3	A
Diode Forward Voltage	$I_S = 3A, V_{GS} = 0V$	V_{SD}	--	--	1.6	V
Reverse Recovery Time	$V_{DD} = 40V, I_S = 3A,$ $di/dt = 100A/\mu s, T_J = 150^\circ C$ (See test circuit)	t_{fr}	--	315	--	nS
Reverse Recovery Charge		Q_{fr}	--	940	--	μC
Reverse Recovery Current		I_{RRM}	--	7.2	--	A

Notes:

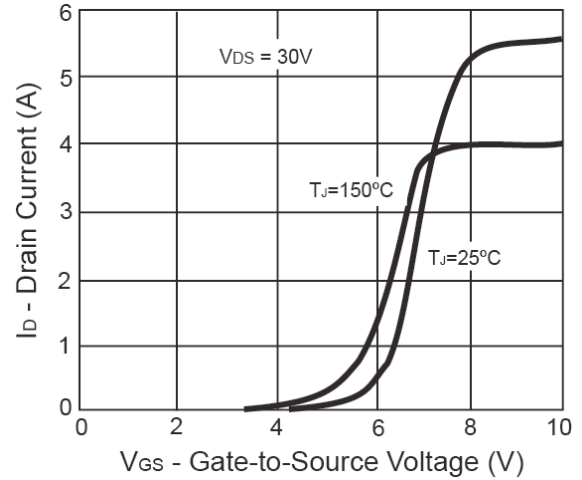
1. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
2. $I_{SD} < 4.5A$, $di/dt < 200A/\mu s$, $V_{DD} < BV_{DSS}$
3. Starting $V_{DD} = 50V$, $H = 27mH$, $T_J = 25^\circ C$
4. Pulse width limited by safe operating area.

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

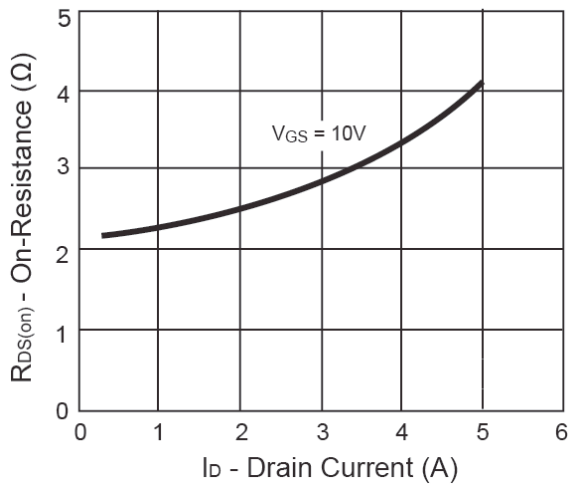
Output Characteristics



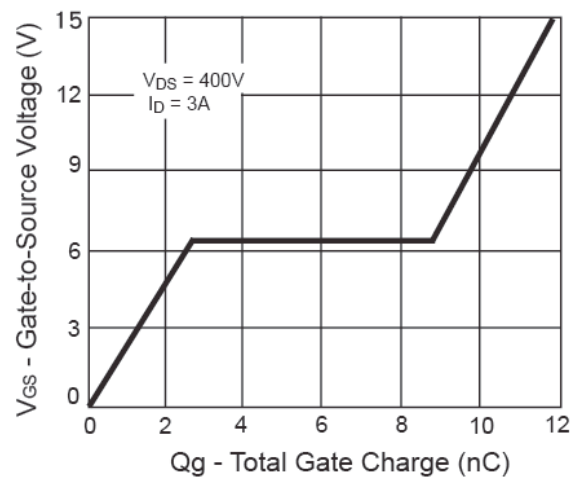
Transfer Characteristics



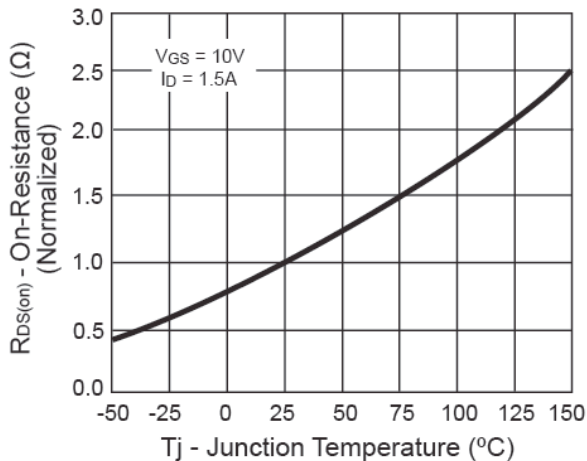
On-Resistance vs. Drain Current



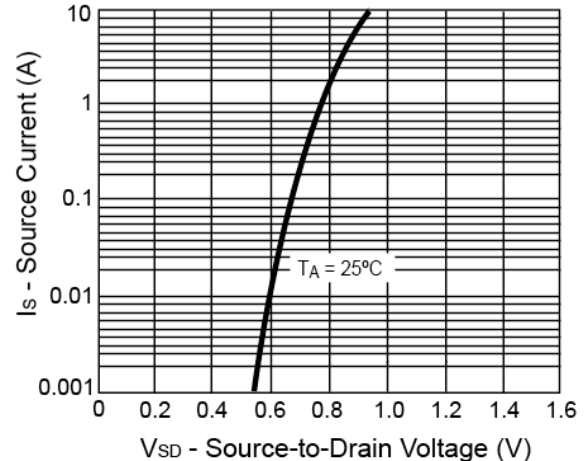
Gate Charge



On-Resistance vs. Junction Temperature

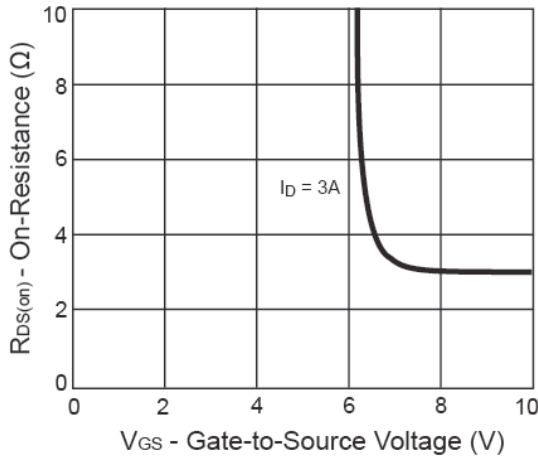


Source-Drain Diode Forward Voltage

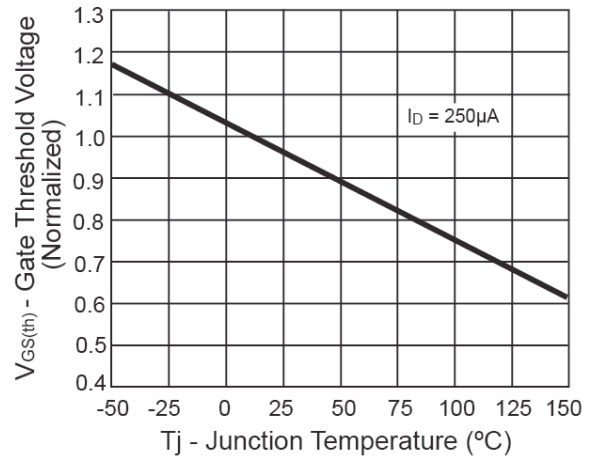


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

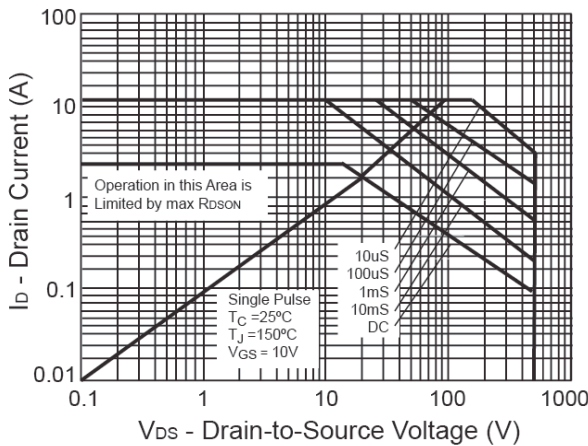
On-Resistance vs. Gate-Source Voltage



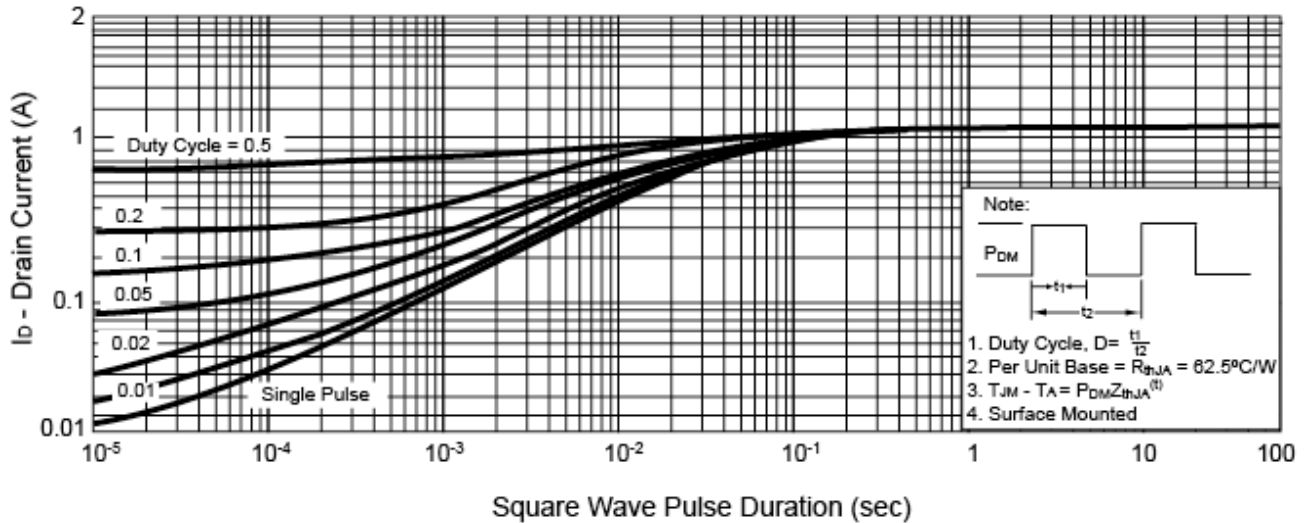
Threshold Voltage



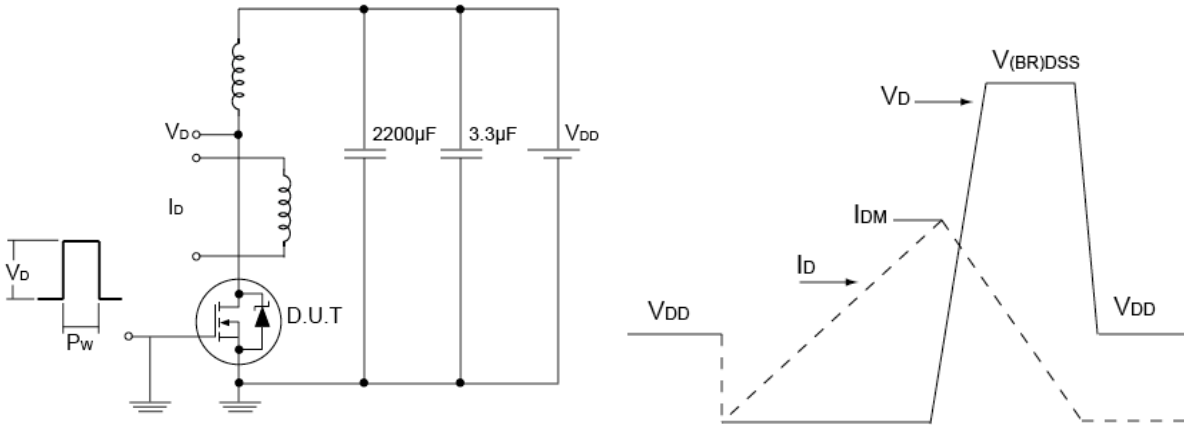
Maximum Safe Operating Area



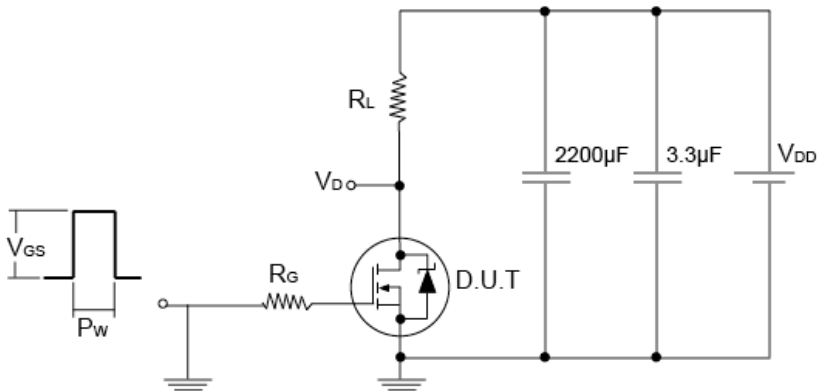
Normalized Thermal Transient Impedance, Junction-to-Ambient



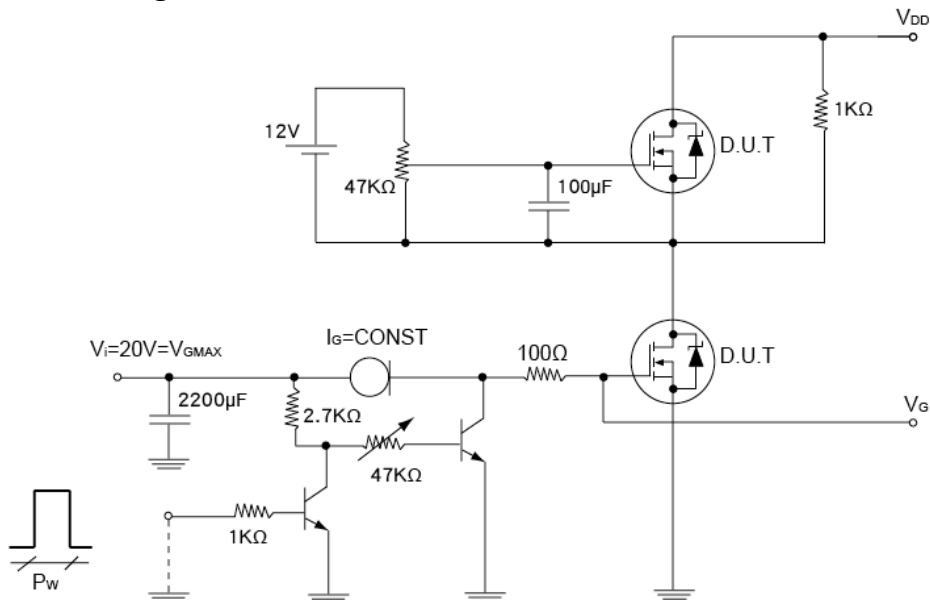
Unclamped Inductive Load Test Circuit and Waveform



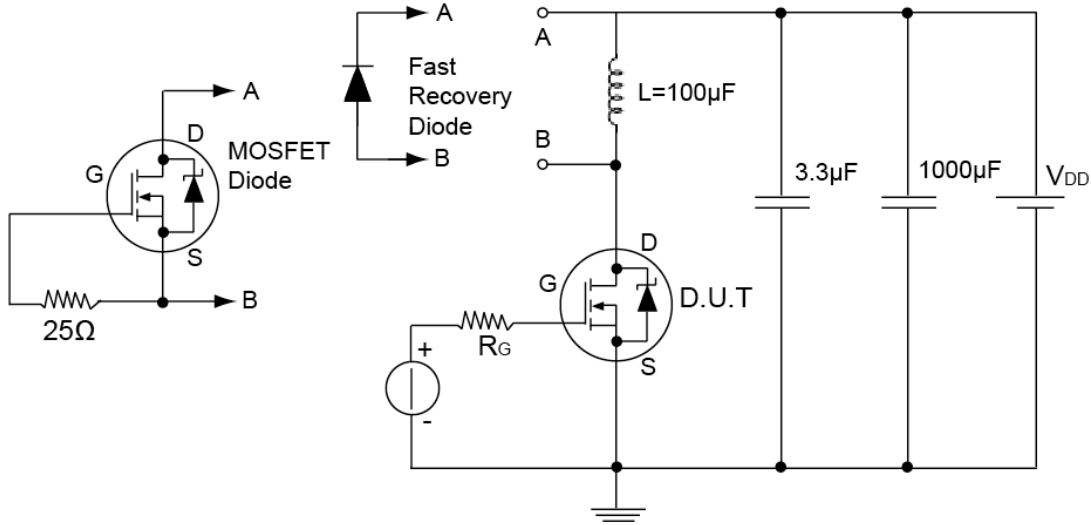
Switching Time Test Circuits for Resistive Load



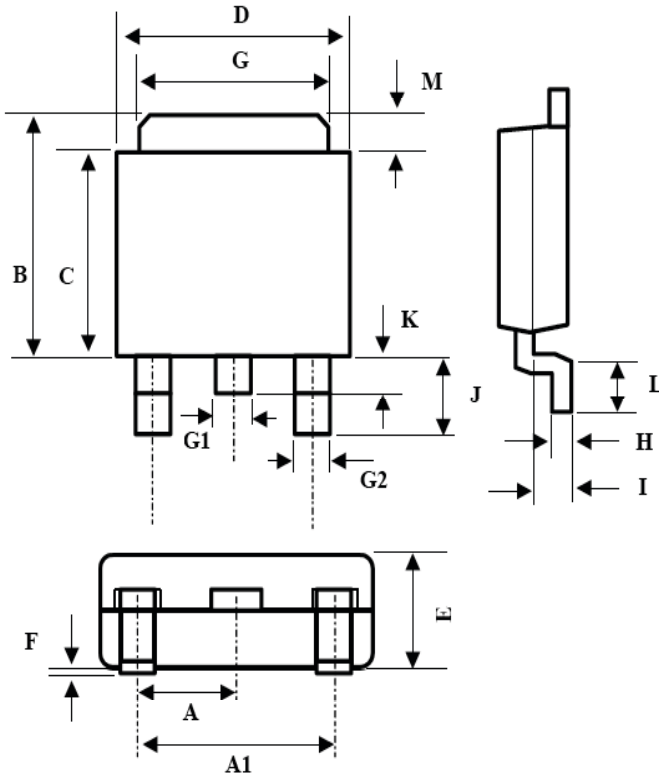
Gate Charge Test Circuit



Test Circuit for Inductive Load Switching and Diode Recovery Times

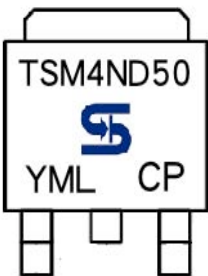


SOT-252 Mechanical Drawing



TO-252 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.3BSC		0.09BSC	
A1	4.6BSC		0.18BSC	
B	6.80	7.20	0.268	0.283
C	5.40	5.60	0.213	0.220
D	6.40	6.65	0.252	0.262
E	2.20	2.40	0.087	0.094
F	0.00	0.20	0.000	0.008
G	5.20	5.40	0.205	0.213
G1	0.75	0.85	0.030	0.033
G2	0.55	0.65	0.022	0.026
H	0.35	0.65	0.014	0.026
I	0.90	1.50	0.035	0.059
J	2.20	2.80	0.087	0.110
K	0.50	1.10	0.020	0.043
L	0.90	1.50	0.035	0.059
M	1.30	1.70	0.051	0.67

Marking Diagram



- Y** = Year Code
- M** = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apr, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
- L** = Lot Code

Notice

Specifications of the products displayed herein are subject to change without notice. TSC or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in TSC's terms and conditions of sale for such products, TSC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TSC products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TSC for any damages resulting from such improper use or sale.