TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM3900D

20V Dual N-Channel MOSFET

SOT-26

Pin Definition:

1. Gate 1
2. Source 2
3. Gate 2
6. Drain 1
5. Source 1
4. Drain 2

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
20	55 @ V_{GS} = 4.5V	2.0
	70 @ V_{GS} = 2.5V	1.5
	110 @ V_{GS} = 1.8V	1.0

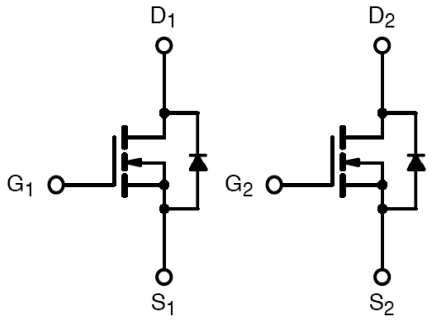
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



Dual N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM3900DCX6 RF	SOT-26	T&R

Absolute Maximum Rating (Ta = 25 °C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current		I_D	2	A
Pulsed Drain Current		I_{DM}	8	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	1.6	A
Maximum Power Dissipation	Ta = 25 °C	P_D	2.0	W
	Ta = 70 °C		1.3	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to CaseThermal Resistance	$R\Theta_{JC}$	30	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	80	°C/W

Notes:

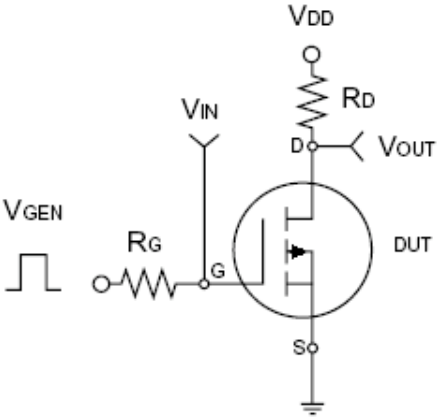
a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 5 sec.

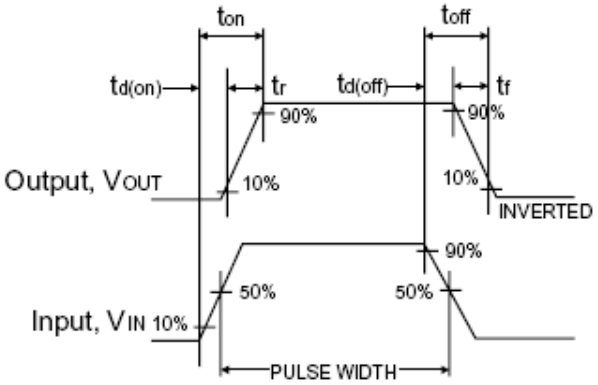
Electrical Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(TH)}$	0.65	0.95	1.2	V
Gate Body Leakage	V_{GS} = ±8V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 16V, V_{GS} = 0V	I_{DSS}	--	--	1.0	uA
On-State Drain Current	V_{DS} ≥ 5V, V_{GS} = 4.5V	$I_{D(ON)}$	5	--	--	A
Drain-Source On-State Resistance	V_{GS} = 4.5V, I_D = 2.0A	$R_{DS(ON)}$	--	45	55	mΩ
	V_{GS} = 2.5V, I_D = 1.5A		--	50	70	
	V_{GS} = 1.8V, I_D = 1.0A		--	80	110	
Forward Transconductance	V_{DS} = 5V, I_D = 2.4A	g_{fs}	--	5	--	S
Diode Forward Voltage	I_S = 1.6A, V_{GS} = 0V	V_{SD}	--	0.79	1.1	V
Dynamic[b]						
Total Gate Charge	V_{DS} = 10V, I_D = 2.4A, V_{GS} = 4.5V	Q_g	--	3.69	--	nC
Gate-Source Charge		Q_{gs}	--	0.70	--	
Gate-Drain Charge		Q_{gd}	--	1.06	--	
Input Capacitance	V_{DS} = 10V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	427.12	--	pF
Output Capacitance		C_{oss}	--	80.56	--	
Reverse Transfer Capacitance		C_{rss}	--	57	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = 10V, R_L = 10Ω, I_D = 1A, V_{GEN} = 4.5V, R_G = 6Ω	$t_{d(on)}$	--	6.16	--	nS
Turn-On Rise Time		t_r	--	7.56	--	
Turn-Off Delay Time		$t_{d(off)}$	--	16.61	--	
Turn-Off Fall Time		t_f	--	4.07	--	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



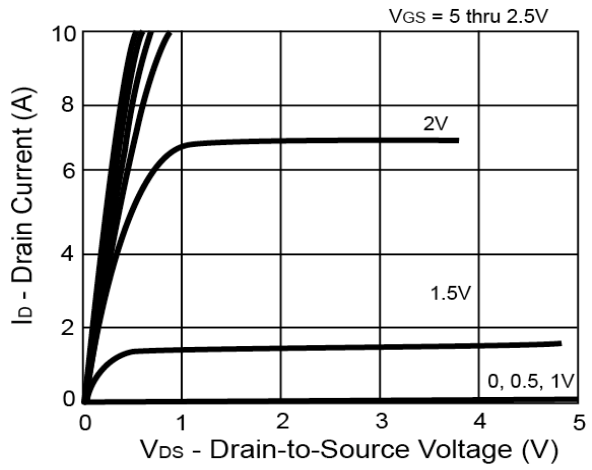
Switching Test Circuit



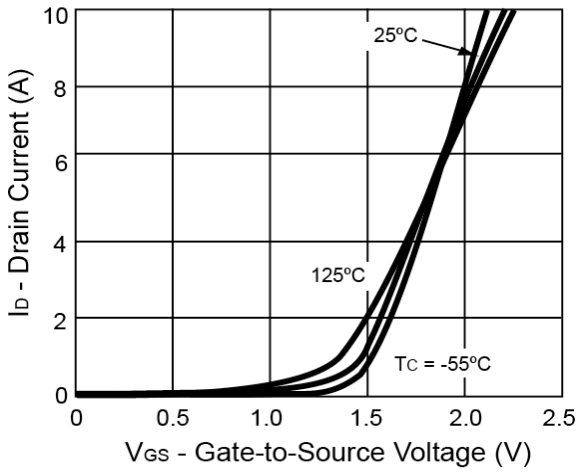
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25 °C, unless otherwise noted)

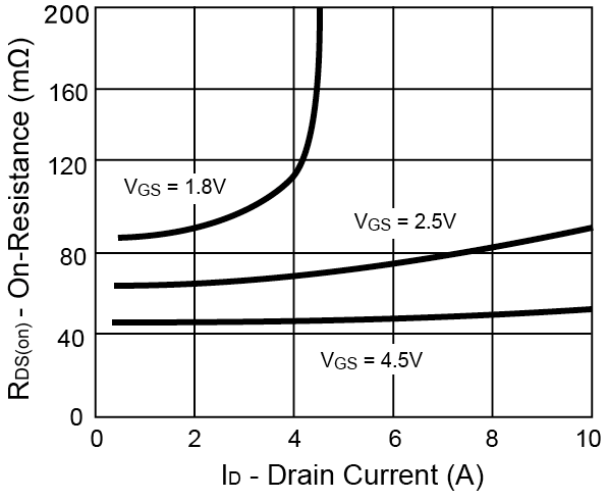
Output Characteristics



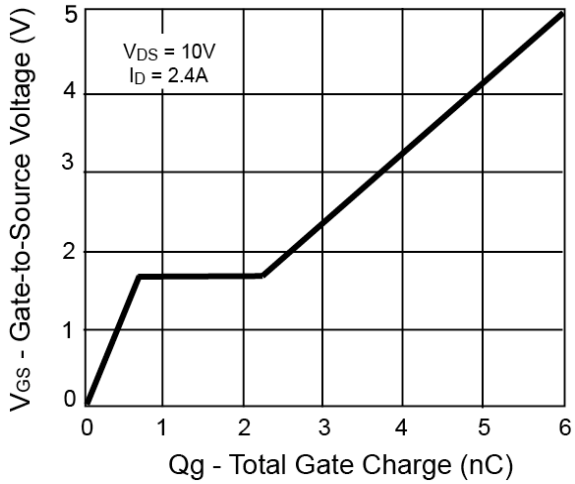
Transfer Characteristics



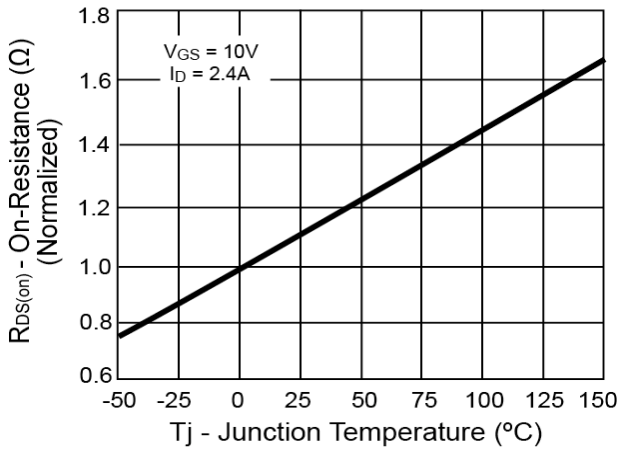
On-Resistance vs. Drain Current



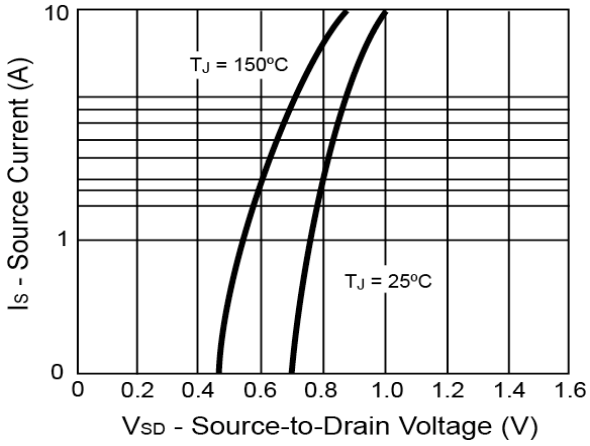
Gate Charge



On-Resistance vs. Junction Temperature

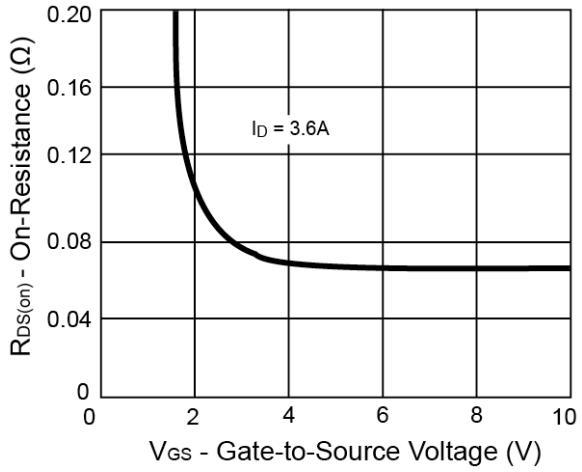


Source-Drain Diode Forward Voltage

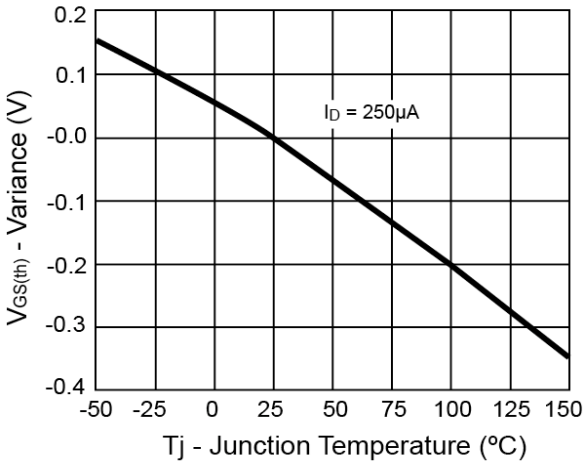


Electrical Characteristics Curve (Ta = 25 °C, unless otherwise noted)

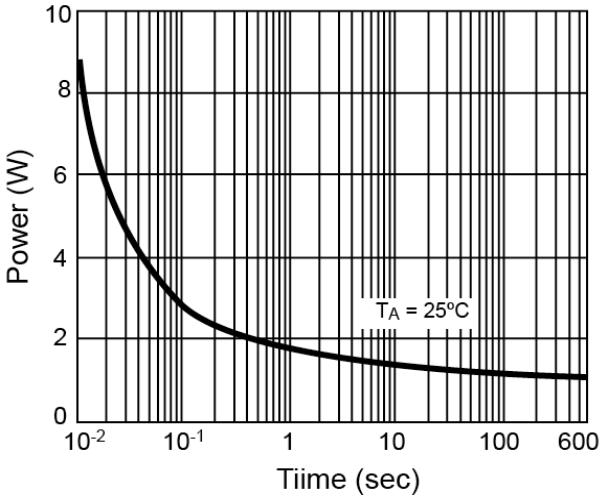
On-Resistance vs. Gate-Source Voltage



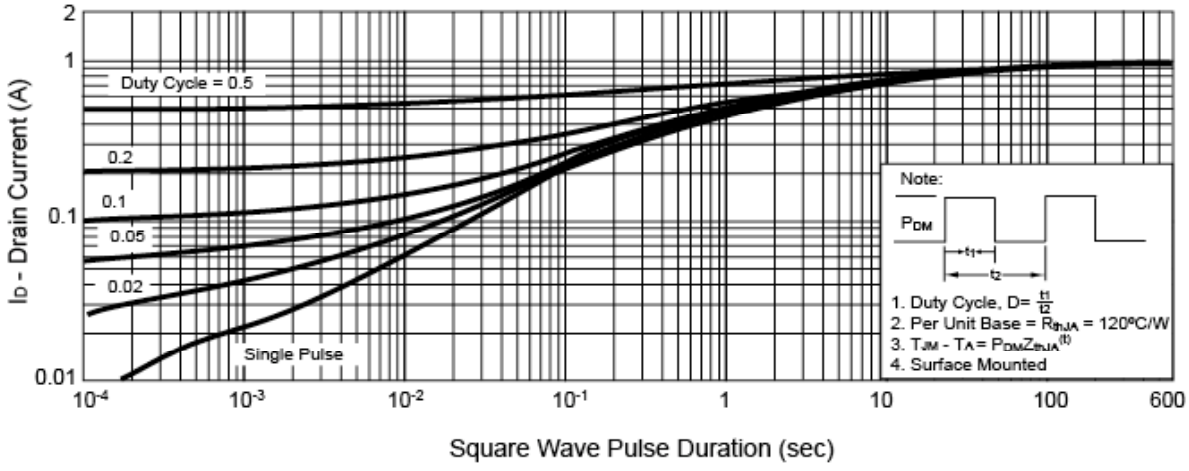
Threshold Voltage



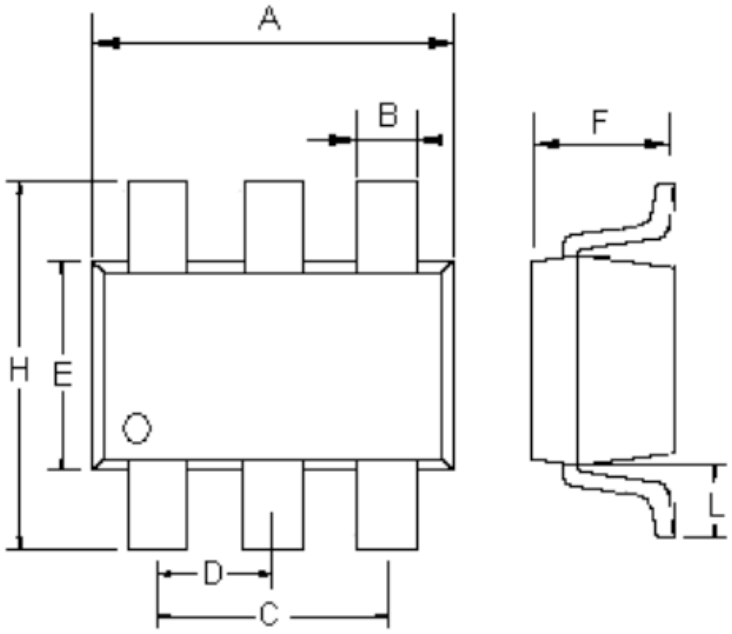
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-26 Mechanical Drawing



SOT-26 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	2.70	3.00	0.106	0.118
B	0.25	0.50	0.010	0.020
C	1.90(typ)		0.075(typ)	
D	0.95(typ)		0.037(typ)	
E	1.50	1.70	0.059	0.067
F	1.05	1.35	0.041	0.053
H	2.60	3.00	0.102	0.118
L	0.60(typ)		0.024(typ)	

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