



P-Channel Enhancement-Mode Vertical DMOS Power FETs

T-39-19

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package				
			TO-39	TO-92	TO-220	Quad P-DIP	Quad C-DIP
-40V	4Ω	1.5A	VP0204N2	—	VP0204N5	VP0204N6	VP0204N7
-60V	4Ω	1.5A	VP0206N2	VP0206N3	VP0206N5	VP0206N6	VP0206N7
-100V	4Ω	1.5A	VP0210N2	VP0210N3	VP0210N5	—	—

Features

- Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

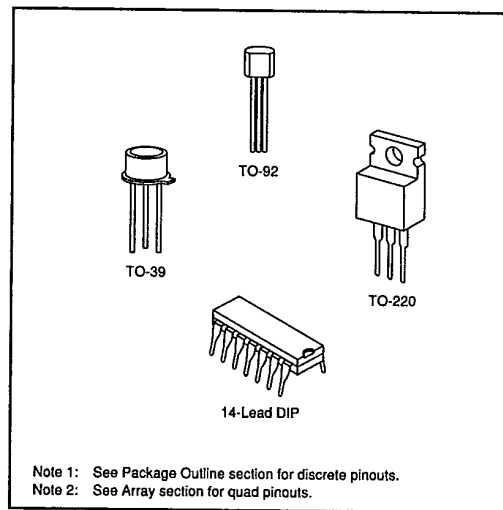
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- Motor control
- Convertors
- Amplifiers
- Switches
- Power supply circuits
- Driver (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
 Note 2: See Array section for quad pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JC} °C/W	θ_{JA} °C/W	I_{DR}	I_{DRM}^*
TO-39	-0.8A	-4.0A	6W	125	20	-0.8A	-4.0A
TO-92	-0.4A	-3.5A	1W	170	125	-0.4A	-3.5A
TO-220	-2.0A	-4.5A	27W	70	4.7	-2.0A	-4.5A
Plastic Dip	Refer to Arrays & Special Functions Section.						
Ceramic Dip							

* I_D (continuous) is limited by max rated T_J .

Electrical Characteristics (@ 25°C unless otherwise specified)

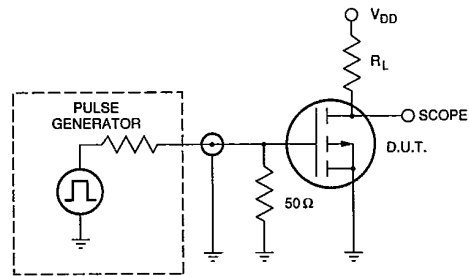
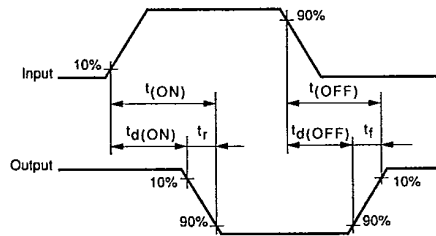
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP0210	-100			V $I_D = -2.5\text{mA}, V_{GS} = 0$
		VP0206	-60			
		VP0204	-40			
$V_{GS(th)}$	Gate Threshold Voltage	-1.0		-3.5	V	$V_{GS} = V_{DS}, I_D = -2.5\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.0	-3.5	mV/°C	$I_D = -2.5\text{mA}, V_{GS} = V_{DS}$
I_{GSS}	Gate Body Leakage		-1.0	-100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			-25	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
			-0.6	-1.0	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	-0.4			A	$V_{GS} = -5\text{V}, V_{DS} = -25\text{V}$
		-1.5	-2.5			$V_{GS} = -10\text{V}, V_{DS} = -25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		3.5	8.0	Ω	$V_{GS} = -5\text{V}, I_D = -0.25\text{A}$
			3	4.0		$V_{GS} = -10\text{V}, I_D = 500\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.75	1.2	%/°C	$I_D = -1.0\text{A}, V_{GS} = -10\text{V}$
G_{FS}	Forward Transconductance	0.3	0.5		S	$V_{DS} = -25\text{V}, I_D = -1.0\text{A}$
C_{ISS}	Input Capacitance		90	150	pF	$V_{GS} = 0, V_{DS} = -25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		65	85		
C_{RSS}	Reverse Transfer Capacitance		15	20		
$t_{d(ON)}$	Turn-ON Delay Time		5	10	ns	$V_{DD} = -25\text{V}$ $I_D = -1\text{A}$ $R_S = 50\Omega$
t_r	Rise Time		7	10		
$t_{d(OFF)}$	Turn-OFF Delay Time		10	15		
t_f	Fall Time		6	10		
V_{SD}	Diode Forward Voltage Drop	-1.3	-2.0			
t_{rr}	Reverse Recovery Time		430		ns	$I_{SD} = -1\text{A}, V_{GS} = 0$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated (Pulse test: 300µs pulse, 2% duty cycle.)

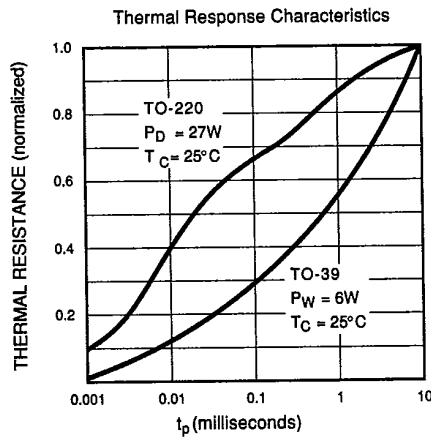
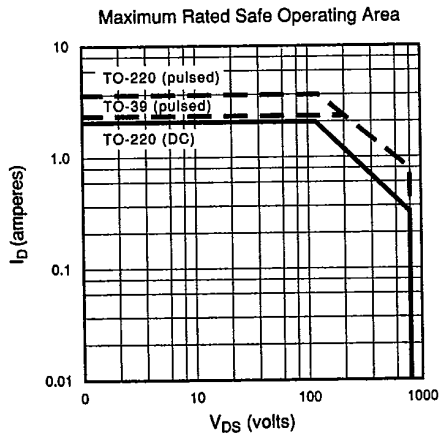
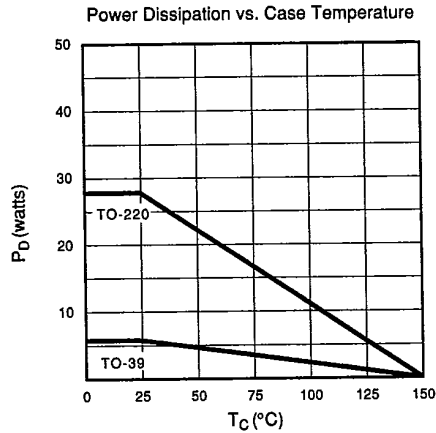
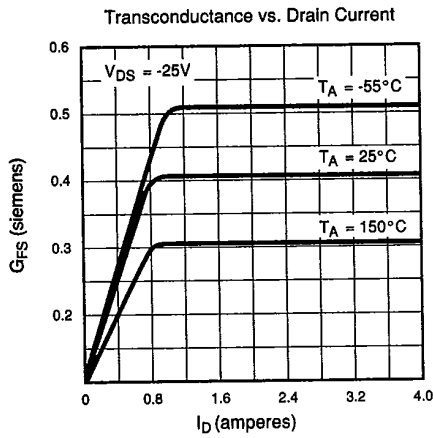
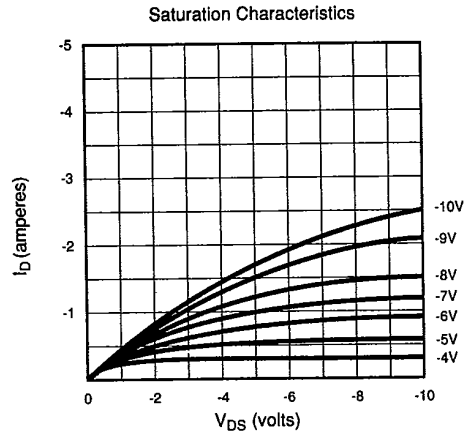
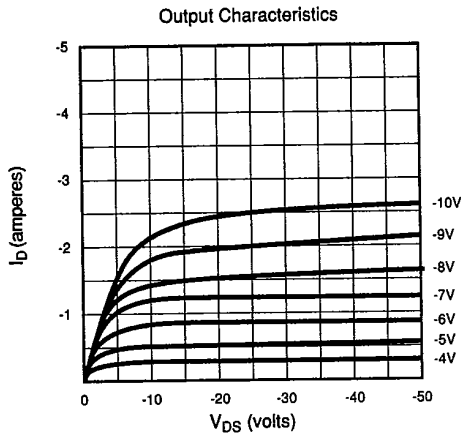
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



Typical Performance Curves

T-39-19



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