Quad 2-input AND gate

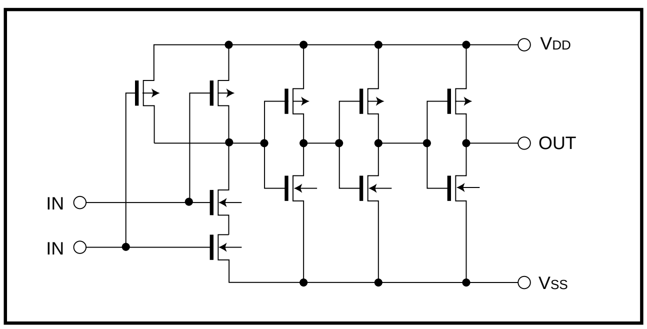
BU4081B / BU4081BF / BU4081BFV

The BU4081B, BU4081BF, and BU4081BFV are dual-input positive-logic AND gates with four circuits mounted on a single chip. An inverter-type buffer is added to the gate output, improving input / output transmission speed, and an increased load capacitance suppresses fluctuation in transmission time to a minimum.

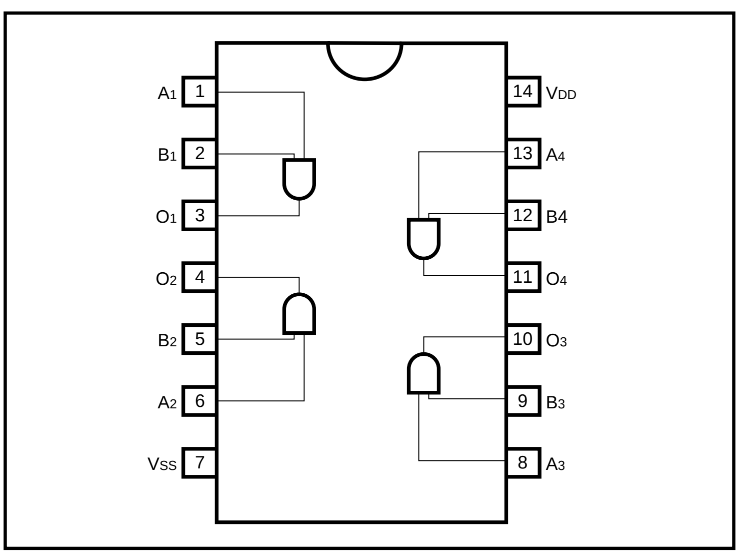
●Features

1) Low power dissipation.
2) Wide range of operating power supply voltages.
3) High input impedance.
4) High fan-out.
5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●Logic circuit diagram



●Block diagram



● Absolute maximum ratings (Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	– 0.3 ~ + 18	V
Power dissipation	Pd	1000 (DIP), 450 (SOP), 350 (SSOP)	mW
Operating temperature	Topr	– 40 ~ + 85	°C
Storage temperature	Tstg	– 55 ~ + 150	°C
Input voltage	V_{IN}	– 0.3 ~ V_{DD} + 0.3	V
I / O pin current	$I_{I/O}$	± 10	mA

● Electrical characteristics (unless otherwise noted, V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions: V_{DD} (V)	Conditions	Measurement circuit
Input high level voltage	V_{IH}	3.5	—	—	V	5	—	Fig.1
		7.0	—	—		10		
		11.0	—	—		15		
Input low level voltage	V_{IL}	—	—	1.5	V	5	—	Fig.1
		—	—	3.0		10		
		—	—	4.0		15		
Input high level current	I_{IH}	—	—	0.3	µA	15	V_{IH} = 15V	Fig.1
Input low level current	I_{IL}	—	—	– 0.3	µA	15	V_{IL} = 0V	Fig.1
Output high level voltage	V_{OH}	4.95	—	—	V	5	I_O = 0mA	Fig.1
		9.95	—	—		10		
		14.95	—	—		15		
Output low level voltage	V_{OL}	—	—	0.05	V	5	I_O = 0mA	Fig.1
		—	—	0.05		10		
		—	—	0.05		15		
Output high level current	I_{OH}	– 0.16	—	—	mA	5	V_{OH} = 4.6V	Fig.1
		– 0.4	—	—		10	V_{OH} = 9.5V	
		– 1.2	—	—		15	V_{OH} = 13.5V	
Output low level current	I_{OL}	0.44	—	—	mA	5	V_{OL} = 0.4V	Fig.1
		1.1	—	—		10	V_{OL} = 0.5V	
		3.0	—	—		15	V_{OL} = 1.5V	
Static current dissipation	I_{DD}	—	—	1	µA	5	V_I = V_{DD} or GND	—
		—	—	2		10		
		—	—	4		15		

Switching characteristics (unless otherwise noted, V_{SS} = 0V, Ta = 25°C, C_L = 50pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions	Measurement circuit
Output rise time	t_{TLH}	—	180	—	ns	5	—	Fig.2
		—	90	—		10		
		—	65	—		15		
Output fall time	t_{THL}	—	100	—	ns	5	—	Fig.2
		—	50	—		10		
		—	40	—		15		
"L" to "H" Propagation delay time	t_{PLH}	—	160	—	ns	5	—	Fig.2
		—	65	—		10		
		—	50	—		15		
"H" to "L" Propagation delay time	t_{PHL}	—	160	—	ns	5	—	Fig.2
		—	65	—		10		
		—	50	—		15		
Input capacitance	C_{IN}	—	5	—	pF	—	—	—

● Measurement circuits

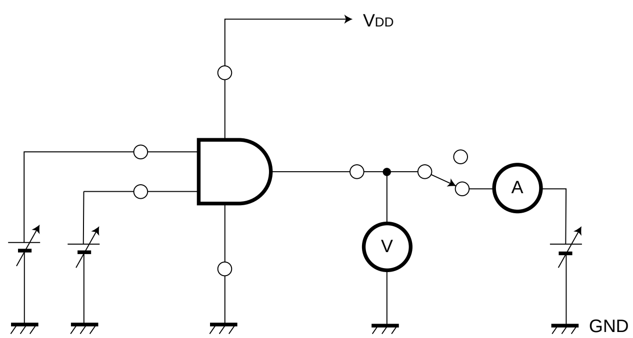


Fig. 1 DC characteristics

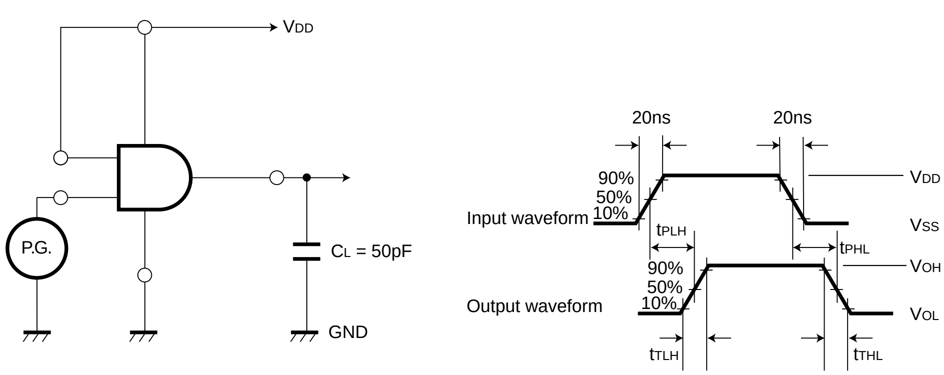


Fig. 2 Switching characteristics

● Electrical characteristic curve

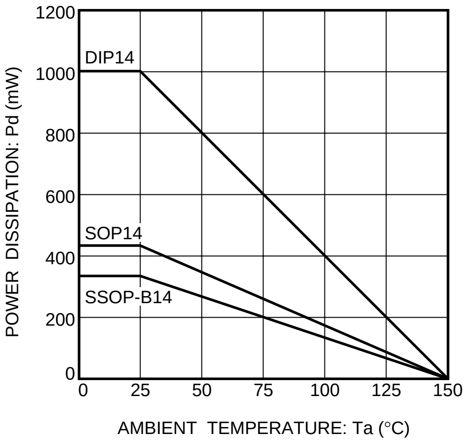
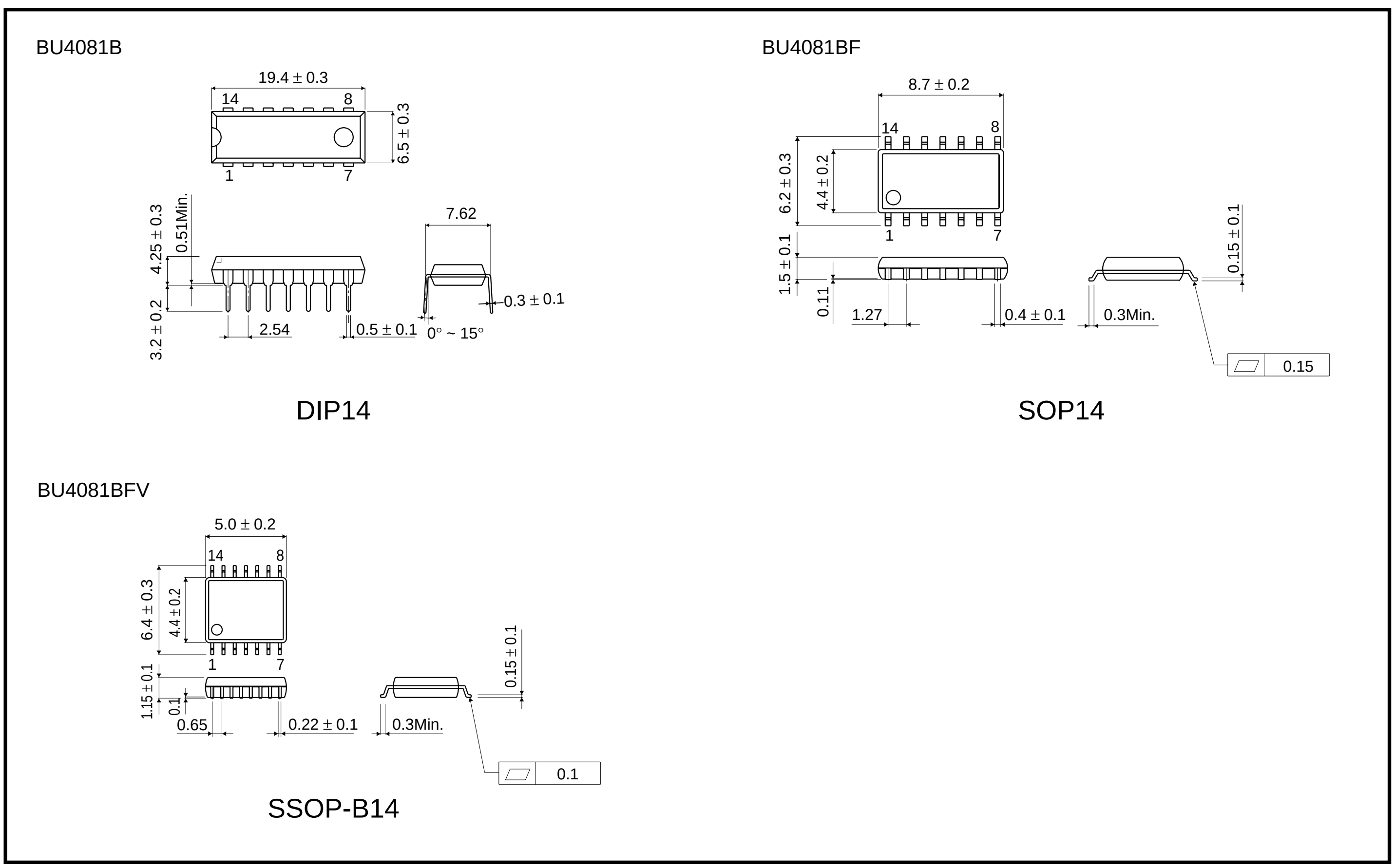


Fig. 3 Power dissipation vs. Ta

● External dimensions (Units: mm)



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