

NTNS3A65PZ

Small Signal MOSFET

-20 V, -281 mA, Single P-Channel,
SOT-883 (XDFN3) 1.0 x 0.6 x 0.4 mm
Package

Features

- Single P-Channel MOSFET
- Ultra Low Profile SOT-883 (XDFN3) 1.0 x 0.6 x 0.4 mm for Extremely Thin Environments Such as Portable Electronics
- Low $R_{DS(on)}$ Solution in the Ultra Small 1.0 x 0.6 mm Package
- 1.5 V Gate Drive
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Side Switch
- High Speed Interfacing
- Optimized for Power Management in Ultra Portable Solutions

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	-20	V	
Gate-to-Source Voltage		V_{GS}	± 8	V	
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$	-281	mA
			$T_A = 85^\circ\text{C}$	-202	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	-332		
Power Dissipation (Note 1)	Steady State	P_D	$T_A = 25^\circ\text{C}$	155	mW
	$t \leq 5$ s			218	
Pulsed Drain Current	$t_p = 10$ μs	I_{DM}	-842	mA	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode) (Note 2)		I_S	-130	mA	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using the minimum recommended pad size, or 2 mm², 1 oz Cu.
2. Pulse Test: pulse width ≤ 300 μs , duty cycle $\leq 2\%$

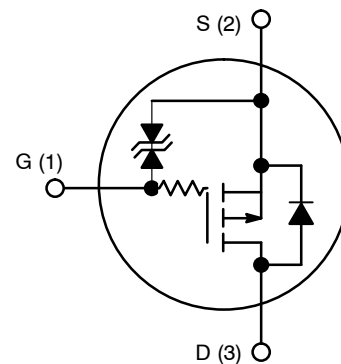


ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D Max
-20 V	1.3 Ω @ -4.5 V	-281 mA
	2.0 Ω @ -2.5 V	
	3.4 Ω @ -1.8 V	
	4.5 Ω @ -1.5 V	

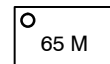
P-CHANNEL MOSFET



MARKING DIAGRAM



SOT-883 (XDFN3)
CASE 506CB



65 = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NTNS3A65PZT5G	SOT-883 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	804	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	574	

3. Surface-mounted on FR4 board using the minimum recommended pad size, or 2 mm², 1 oz Cu.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\ \mu\text{A}$, ref to 25°C		11		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -20\text{ V}$ $T_J = 25^\circ\text{C}$			-1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$			±10	μA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.2		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -200\text{ mA}$		0.9	1.3	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -100\text{ mA}$		1.3	2.0	
		$V_{GS} = -1.8\text{ V}, I_D = -50\text{ mA}$		1.8	3.4	
		$V_{GS} = -1.5\text{ V}, I_D = -10\text{ mA}$		2.3	4.5	Ω
Forward Transconductance	g_{FS}	$V_{DS} = -5\text{ V}, I_D = -200\text{ mA}$		0.58		S
Source-Drain Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -100\text{ mA}$		-0.8	-1.2	V

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}$, freq = 1 MHz, $V_{DS} = -10\text{ V}$		44		pF
Output Capacitance	C_{OSS}			6.7		
Reverse Transfer Capacitance	C_{RSS}			5.5		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}; I_D = -200\text{ mA}$		1.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.1		
Gate-to-Source Charge	Q_{GS}			0.2		
Gate-to-Drain Charge	Q_{GD}			0.2		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -200\text{ mA}, R_G = 2\ \Omega$		18		ns
Rise Time	t_r			32		
Turn-Off Delay Time	$t_{d(OFF)}$			178		
Fall Time	t_f			84		

4. Switching characteristics are independent of operating junction temperatures

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TYPICAL CHARACTERISTICS

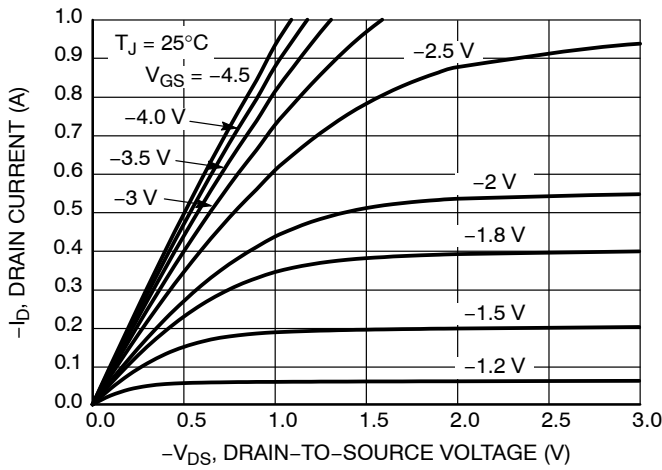


Figure 1. On-Region Characteristics

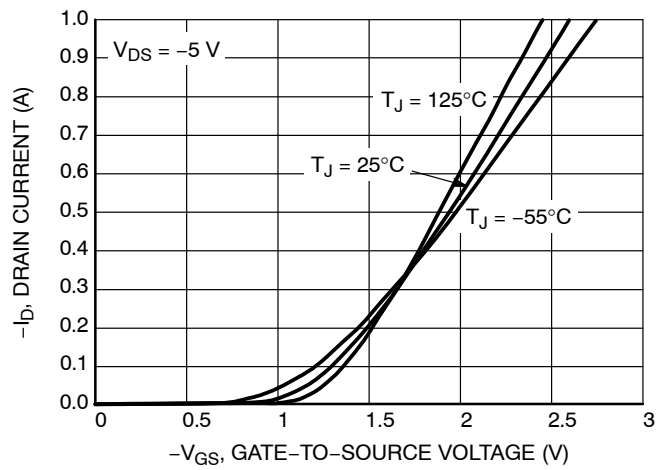


Figure 2. Transfer Characteristics

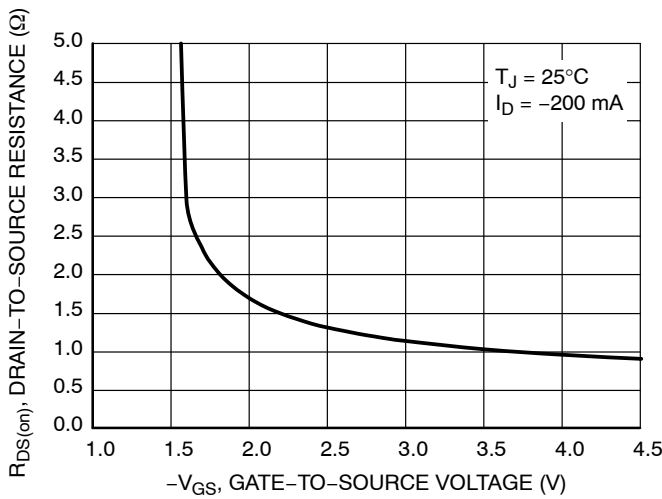


Figure 3. On-Resistance vs. Gate Voltage

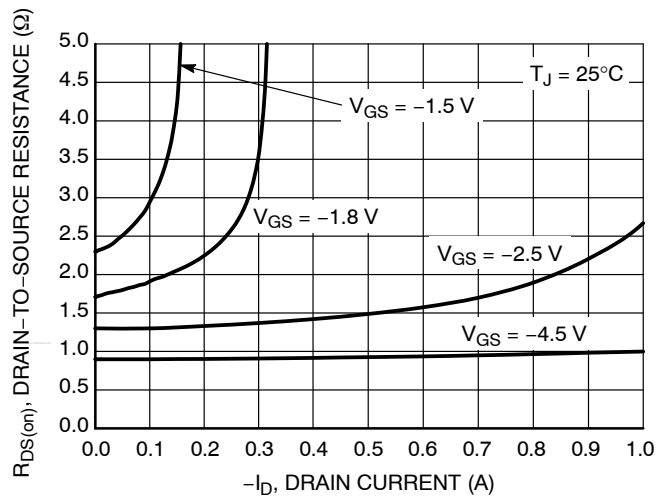


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

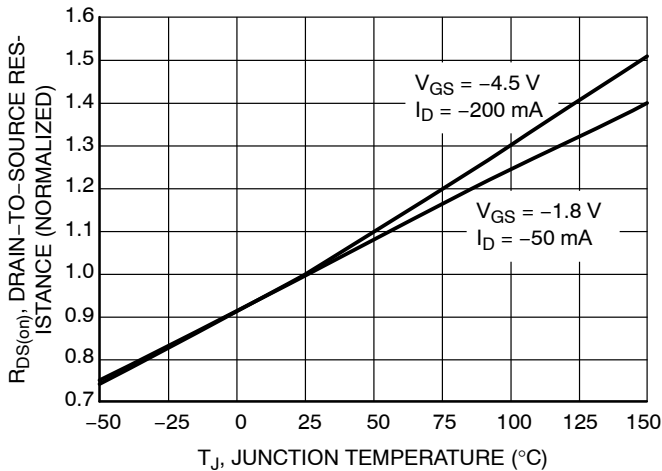


Figure 5. On-Resistance Variation with Temperature

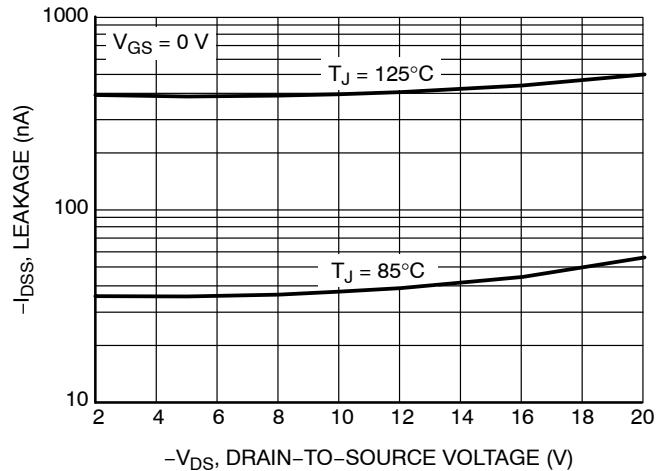


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

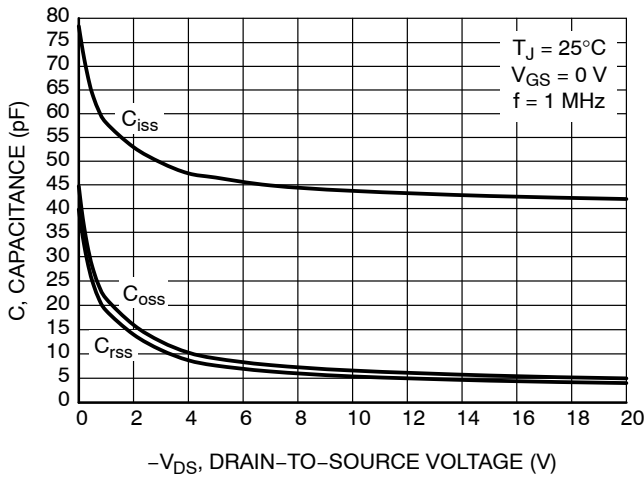


Figure 7. Capacitance Variation

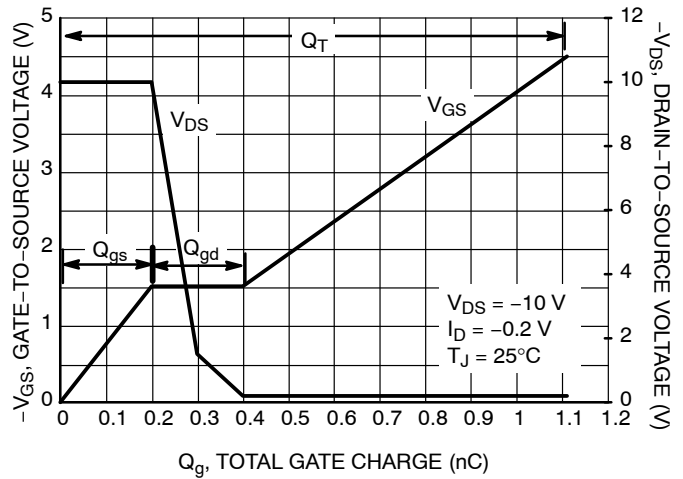


Figure 8. Gate-to-Source Voltage vs. Total Charge

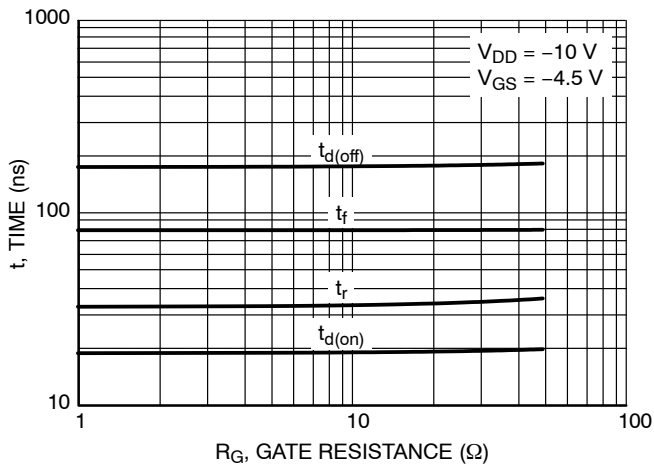


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

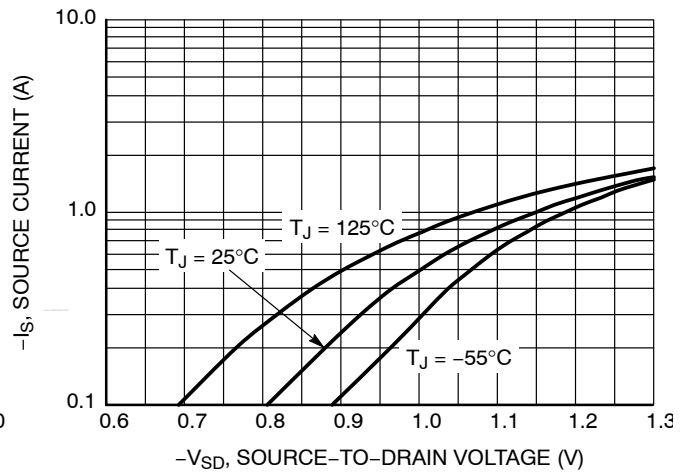


Figure 10. Diode Forward Voltage vs. Current

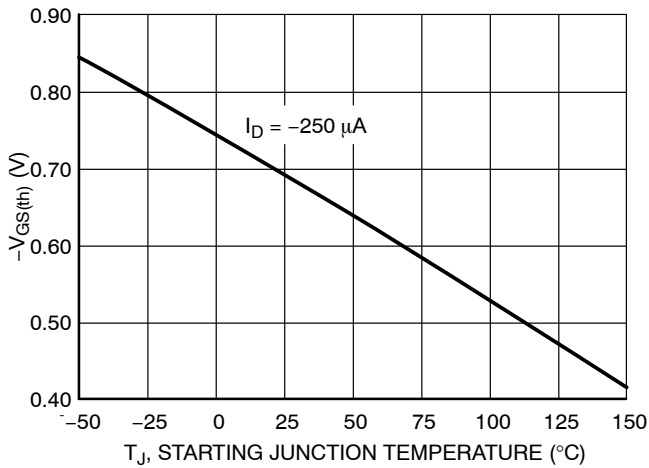


Figure 11. Threshold Voltage

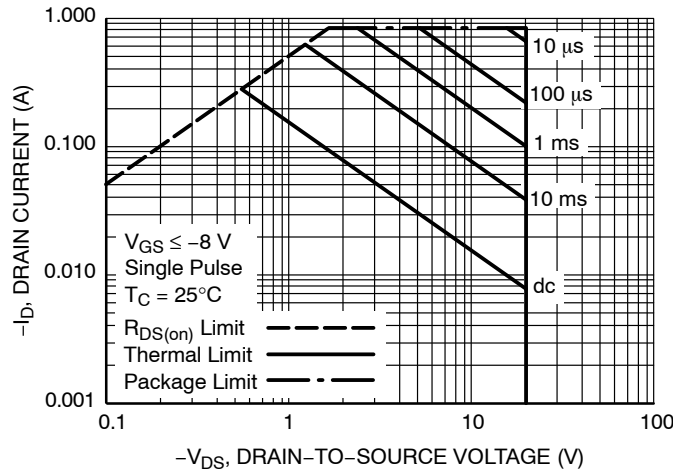


Figure 12. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS

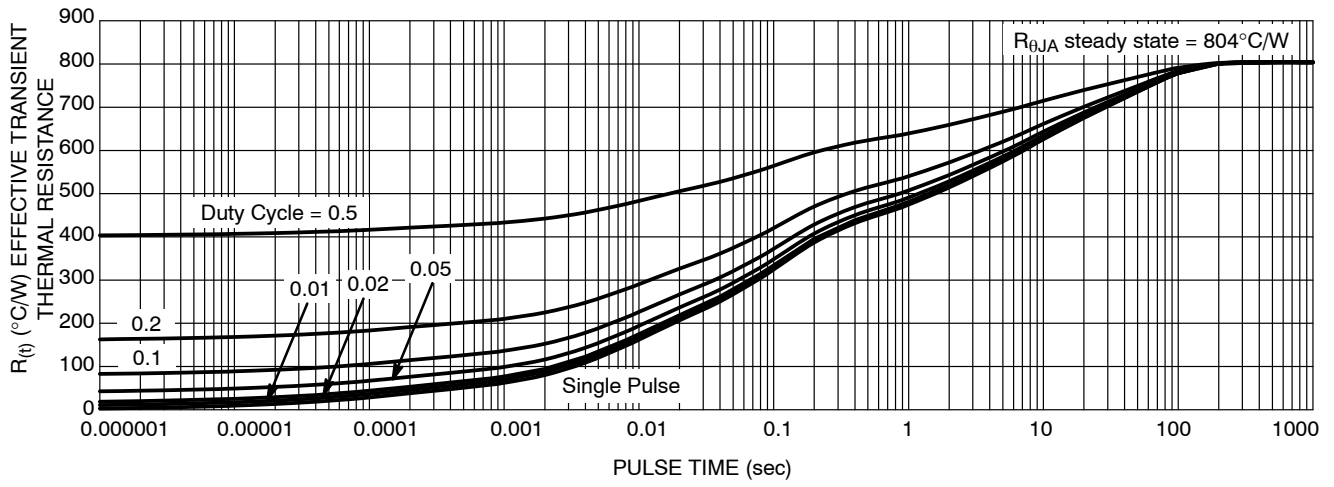
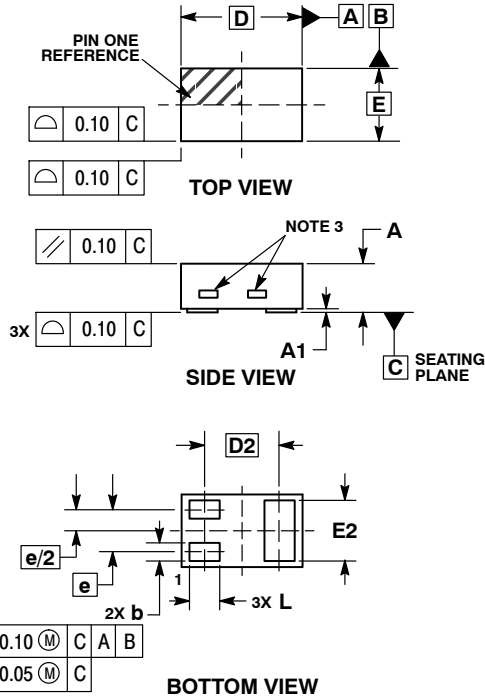


Figure 13. Thermal Response

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PACKAGE DIMENSIONS

SOT-883 (XDFN3), 1.0x0.6, 0.35P
CASE 506CB
ISSUE A

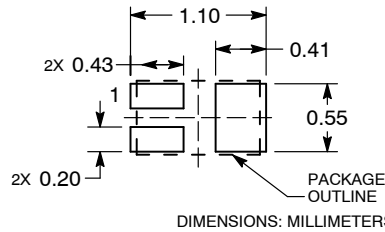


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

MILLIMETERS		
DIM	MIN	MAX
A	0.340	0.440
A1	0.000	0.030
b	0.075	0.200
D	0.950	1.075
D2	0.620 BSC	
e	0.350 BSC	
E	0.550	0.675
E2	0.425	0.550
L	0.170	0.300

RECOMMENDED SOLDER FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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