GEC PLESSEY
SEMICONDUCTORS

MAY 1996
ADVANCE INFORMATION
D.S. 3913 3.0

MV1822

PDC, VPS AND TIME RECEIVER

(Supersedes version in October 1995 Media IC Handbook, HB3120 –3.0)

The MV1822 is a member of the Enhanced Video Automation (EVA) family for receiving Programme Delivery Control (PDC) messages, packet 8/30 Format 2, broadcast in World System Teletext (WST). It will automatically switch to receiving Video Programme System (VPS) data from TV line 16 in Manchester bi–phase format in the absence of PDC data. Under control of the mode pins, it can also receive Broadcast Service Data Packet format one data to provide Unified Date and Time (UDT) or Time data from headers. The data from a service can be read via the I²C bus connections in a standard format (see pages 7, 8 and 9).

FEATURES

- On–chip analog data slicing
- Low external component count
- Low frequency 6·9375MHz oscillator
- I²C Bus and $\overline{DAV}$ released during power down
- Automatic PDC/VPS operation
- Advanced CMOS technology gives low power dissipation and high reliability
- "Fast–Mode" I²C bus

APPLICATIONS

- Accurate programme recordings via PDC and VPS
- Automatic Date/Time setting of VCR and TV
- Automatic tuning of VCR and TV via station ident

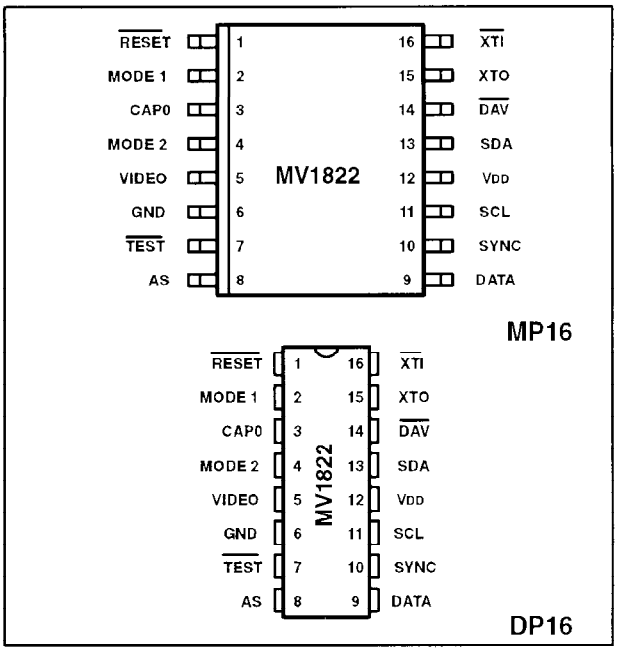


Fig. 1 Pin connections – top view

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0·3 to 7·0V
All inputs	–0·3 to V_{DD} +0·3V
Operating Temperature	–40 to +85°C
Storage Temperature	–65 to 150°C

ORDERING INFORMATION

MV1822 IG DPAS
MV1822 IG MPES
MV1822 IG MPEE (Tape and Reel)

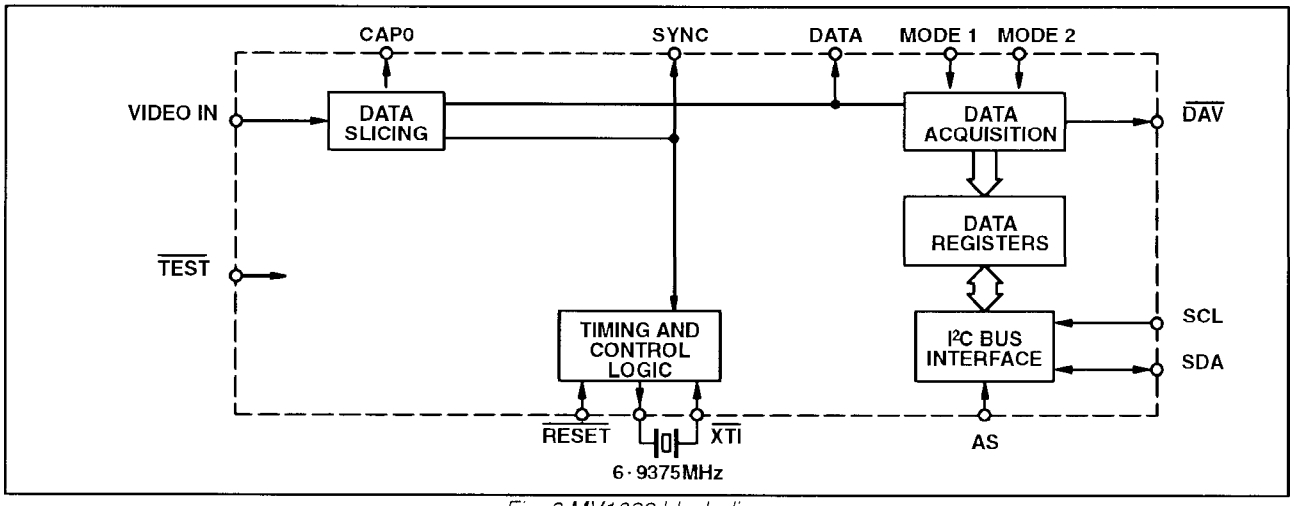


Fig. 2 MV1822 block diagram

ELECTRICAL CHARACTERISTICS

T_{amb}= −40°C to +85°C, V_{DD}=5V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	12	4·5	5·0	5·5	V	
Supply current	12		20		mA	
VIDEO input	5					220nF ±20% input capacitor
Voltage amplitude		1·0	1·8	2·5	V_{pp}	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	
CAP0	3					
Capacitor value			220		nF	Connected to GND
Capacitor tolerance		−20%		+20%		
Effective series resistance				5	Ω	1MHz
DATA & SYNC outputs	9 & 10					
Output voltage High		$0·8V_{DD}$	$0·95V_{DD}$		V	I_{OH} = −2·0mA
Output voltage Low			0·1	0·4	V	I_{OL} = 2·0mA
MODE1, MODE2 & AS	2,4 & 8					75k (nom) pull-down resistor
Input voltage Low		−0·3		$0·2V_{DD}$	V	
Input Voltage High		$0·8V_{DD}$		V_{DD}+0·3	V	
Input current Low		−10		+10	µA	V_{IN}=V_{SS}
Input current High		18	67	275	µA	V_{IN}=V_{DD}
XTI input	16					1M (nom) resistor to XTO
Input voltage Low		−0·3		$0·2V_{DD}$	V	
Input voltage High		$0·8V_{DD}$		V_{DD}+0.3	V	
Input current Low		−0·5	−5·0	−20	µA	−0·3<V_{IN}<V_{IL} max
Input current High		0·5	1·5	20	µA	V_{IH} min <V_{IN}<(V_{DD}+0·3)
XTO output	15					
Output voltage High		$0·8V_{DD}$	$0·9V_{DD}$		V	I_{OH}= −0·1mA
Output voltage Low			0·1	0·4	V	I_{OL}=0·1mA
Frequency			6·9375		MHz	±100ppm
I²C bus						
SCL, SDA Schmitt inputs	11, 13					
Input voltage Low		−0·3		$0·3V_{DD}$	V	
Input voltage High		$0·7V_{DD}$		V_{DD}+0·3	V	
Output Voltage Low			0·1	0·6	V	I_{OL}=6·0mA
SCL Clock Frequency	11	0		400	kHz	
Hysteresis Voltage		0·2	0·4		V	
DAV Data available	14					
Output voltage Low			0·1	0·4	V	I_{OL}=2·0mA
RESET Schmitt input	1					
Threshold voltage falling		1·4	1·9		V	
Threshold voltage rising			3·1	3·8	V	
Hysteresis Voltage		0·6	1·2		V	
Input current Low		−10		+10	µA	V_{IN}=V_{SS}
Input current High		−10		+10	µA	V_{IN}=V_{DD}

Table 1

Pins	Test	Test Levels	Notes
SDA & SCL	Human body model	1kV on 100pF through 1k5Ω	< 15% LTPD
SDA & SCL	Machine model	100V on 200pF through 0Ω & <500nH	
All others	Human body model	4kV on 100pF through 1k5Ω	Meets Mil. Std. 883D class 3 requirements
All others	Machine model	400V on 200pF through 0Ω & <500nH	

LTPD=Lot Tolerant Percent Defective

Table 2 ESD data

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency	6·937500MHz AT cut.
Tolerance over operating temperature range	+50ppm
Tolerance overall	±100ppm
Nominal load capacitance	30pF.
Equivalent series resistance	<20Ω

PIN DESCRIPTION

Symbol	Pin No	Pin Name and Description
$\overline{\text{RESET}}$	1	Active low reset.
MODE 1	2	Control input see truth table below for function. Includes a 75kΩ pull–down resistor
CAP0	3	Capacitor zero, storage for reference voltage
MODE 2	4	Control input see truth table below for function. Includes a 75kΩ pull–down resistor
VIDEO	5	Input for composite video signal with negative going syncs
GND	6	Ground, 0V
$\overline{\text{TEST}}$	7	Test pin, for factory use only, leave open circuit or connected to V_{DD}
AS	8	Address select for I^2C bus. 0010 0001 if set high. or 0010 0011 if set low
DATA	9	Data output
SYNC	10	Sync output
SCL	11	I^2C bus serial clock input
V_{DD}	12	Positive supply voltage, +5V
SDA	13	I^2C bus bi–directional data port
$\overline{\text{DAV}}$	14	Active low open drain output data available signal to microprocessor
XTO	15	Crystal out, 6·9375MHz fundamental crystal with on–chip 1MΩ resistor to XTI
XTI	16	Crystal input

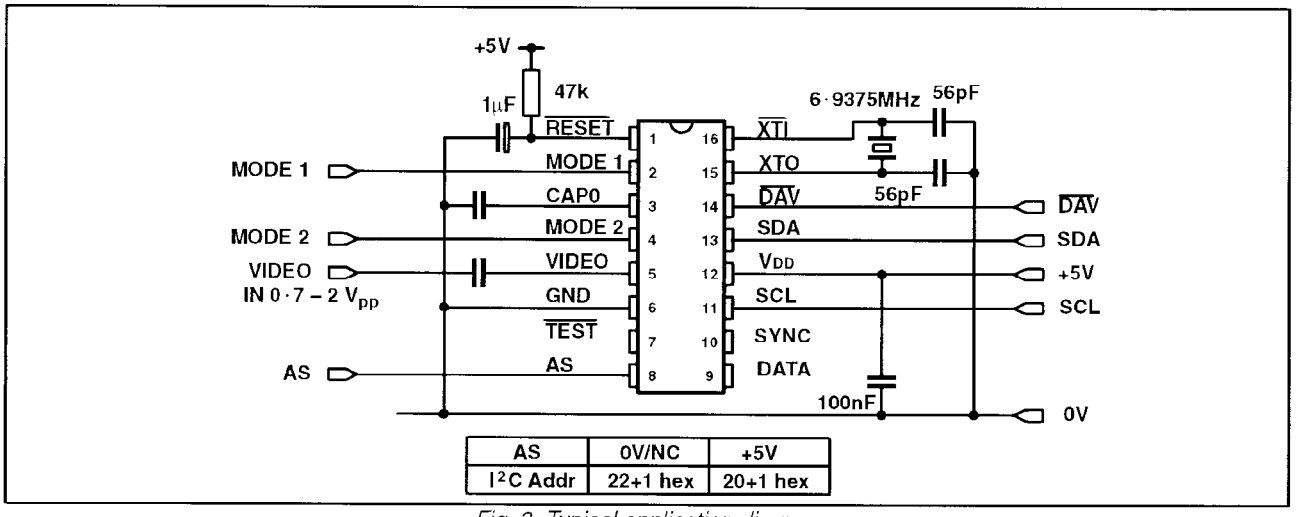


Fig. 3. Typical application diagram

TRUTH TABLE FOR MODE 1 & 2 PINS.

MODE 2 (pin 4)	MODE 1 (pin 2)	FUNCTION
0	0	PDC or VPS
0	1	VPS only
1	0	UDT
1	1	HEADER TIME

Pins MODE 1 and MODE 2 are latched in on the leading edge of sync. When either pin changes state, the contents of the read registers are reset to all 1's and $\overline{DAV}$ is reset off.

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1822 to lock on to the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6–22 and 318–335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext or VPS line 16 data. In normal use both MODE 1 and MODE 2 pins are set low to receive PDC or VPS data. When UDT data is required, the MODE 1 pin must be low and the MODE 2 pin must be high. When VPS only data is required, the MODE 1 pin must be high and the MODE 2 pin low. When TIME data from the header is required, both MODE 1 and MODE 2 pins are set high. An internal pull–down resistor is provided on each mode pin so that for normal mode of operation, the pins may be left open circuit.

Byte number convention

There are 45 bytes in a teletext data packet, numbered 1 to 45. Bytes 1 and 2 are the clock run in, byte 3 is the framing code, bytes 4 and 5 are the magazine and row address group. In packet 8/30 byte 6 is used to indicate the designation code.

PDC reception

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and only valid Broadcast Service Data Packets (BSDP) are accepted. These are also known as packet 8/30. Format two packets, containing the PDC message, are signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8, 4) and stored in seven registers each of eight bits. If the complete message is correctly received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by the $\overline{DAV}$ pin going low. At the same time the data is transferred to a second bank of registers, provided there is no I^2C bus activity at the time, reorganised with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to read out on the I^2C bus when so requested, see page 7.

VPS reception

The VPS data consists of 15 eight bit words encoded in Manchester bi–phase format with a data rate of 2·5Mbits/sec. It is transmitted in only TV line 16 so similar data on other TV lines is excluded. A data low to high transition indicates a binary zero and a high to low transition indicates a binary one. Word 1 acts as a clock run in code (10/10/10/10/10/10/10/10) to synchronise the decoder. Word 2 is a start code (10/00/10/10/10/01/10/01) to verify the required data. Note, the second element 00 contains a deliberate violation of the Manchester bi–phase format which is only permitted in word 2. Words 5, 11, 12, 13, 14 and 15 are Manchester bi–phase decoded and if verified are stored in the input registers. When all the message is correctly received, an interrupt to the microprocessor is signalled by the $\overline{DAV}$ pin going low. At the same time the data is transferred to a second bank of registers, provided there is no I^2C bus activity at the time, reorganised into the sequence – Words 11, 12, 13, 14, 5, 15, followed by 11111110, to be read out on the I^2C bus when requested, see page 7.

PDC/VPS arbitration

In normal mode with both MODE 1 and MODE 2 pins low, PDC data transmitted via Teletext packets 8/30 Format 2, will take precedence over VPS data. A 64 state frame counter is reset by every valid PDC packet, which will inhibit VPS reception until the counter reaches maximum. This will ensure that if receiving both signals on a given transmission, the PDC data will dominate, but if it does at any time cease to be received, the VPS data will be enabled within 2·56 seconds of the last PDC packet. This allows for one packet 8/30 format 2 to be missed without changing to VPS operation.

VPS only mode

In this mode there will be no 2·56 second delay before acquiring VPS signals.

UDT reception

When UDT is enabled, PDC and VPS reception is disabled. When packet 8/30 format one is received, the UDT data in 8 bit format, starting with byte 13, is read into the internal registers provided the I^2C bus is not busy. The received UDT data from byte 16 to byte 21 inclusive has had a one added to each data nibble, to ensure transitions exist when the time data contains many zeros. The MV1822 therefore subtracts a one from each nibble in bytes 16 to 21, so that the output will supply actual UDT data. See pages 5 and 8 for details. The data is not Hamming encoded, so when the complete packet to byte 25 has been received, an interrupt to the microcontroller is generated by the $\overline{DAV}$ pin going low.

When $\overline{DAV}$ is low, I^2C bus readout inhibits reception of further UDT data. If readout is attempted before $\overline{DAV}$ goes low, FF bytes will be output and data reception will not be affected.

If readout occurs after the reception of further UDT data has begun then FF bytes will be output and data reception will not be affected. However, if $\overline{DAV}$ is already low when another packet 8/30 format one is received, then $\overline{DAV}$ will be released at byte 13, until all data has been received at byte 25, when a new interrupt to the microcontroller will be generated by the $\overline{DAV}$ pin going low again. This process will repeat until the data is read via I^2C.

Header TIME

If UDT data is not being broadcast, the time data may be obtained from the last eight bytes of the header packets. If the transmission is in serial mode, C11=1, the last eight bytes of **every** header will be received. Any byte failing parity check will not be written to the registers and the previous value in that location will be retained. As each byte is accepted, numerical data having values 30 to 39 hex (0 to 9 ASCII) will be 30 hex (0 ASCII) subtracted before being written to the registers. All other data will be written as F hex. If the transmission is in parallel mode, C11=0, the last eight bytes of only **magazine 100** headers will be received and processed. When all eight bytes have been received with no errors, an interrupt to the microcontroller is generated by the $\overline{DAV}$ pin going low. At the

same time the data is transferred to a second bank of registers, provided there is no I2C bus activity at the time. Details of the data output format on the I2C bus are given on page 9.

I²C bus interface

The MV1822 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20+1hex) with the address select (AS) pin set high, or 0010 0011 (22+1hex) with the AS pin set low. The read bit (LSB) must always be set, it is not possible to write to the MV1822.

On recognising its address, the MV1822 will send an acknowledge and then transmit on the SDA line the first byte from the output registers, most significant bit (MSB) first. It will then monitor the SDA line "for an acknowledge" from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1822 will release the data line to allow the microprocessor to send a stop condition. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged.

In normal mode there will be seven bytes of data available, the final data byte will be either, PDC byte 13 followed by 1111 or 11111110 for VPS messages, see page 7. The last nibble of the message serves to indicate the source of data: 1111=PDC, 1110=VPS

In UDT mode there will be 13 bytes of data available when $\overline{DAV}$ has gone low, the last byte contains the second half of the 2nd Short Programme Label, see page 8.

In header TIME mode there will be four bytes of data available when $\overline{DAV}$ has gone low, see page 9.

When readout is complete, the $\overline{DAV}$ pin is released. If the microprocessor continues to send clocks on the SCL line, the MV1822 will output FF bytes on the SDA line. Also if the MV1822 is re–addressed before further data is received and $\overline{DAV}$ goes low, the MV1822 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an Acknowledge (followed optionally by a STOP condition) after any byte has been sent by the MV1822. The $\overline{DAV}$ pin will then be released. Also, if after a partial readout, the microprocessor sends a repeat START condition followed by the MV1822 I²C bus address, or the mode pins are changed state, $\overline{DAV}$ pin will be released and the MV1822 will output FF bytes on the SDA line.

To prevent any corruption of the data in the output registers during I²C bus activity, valid PDC or VPS messages are held in the incoming registers until I²C bus activity ceases. Here they may be over–written by new PDC or VPS messages until the I²C bus activity ceases and they can be transferred to the output registers. In the absence of I²C bus reads, subsequent valid messages will continue to be transferred to the output registers over–writing any existing data. In this way the output registers always contain the latest PDC or VPS message, see page 7.

When $\overline{DAV}$ goes low I²C bus readout inhibits reception of further UDT data. If readout is attempted before $\overline{DAV}$ goes low, FF bytes will be output and data reception will not be affected.

General information

System clock is provided by an on chip 6·9375MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset ($\overline{RESET}$ pulled low), the $\overline{DAV}$ pin will be released. When the MV1822 is powered down, the I²C bus and $\overline{DAV}$ pins will be released so that the lines can be used by other devices.

Example of UDT packet 8/30 format one data

	Network Ident		LTO	Modified Julian Date (MJD)			Co–ordinated Universal Time (UTC)			SPL 1		SPL 2	
Byte number	13	14	15	16	17	18	19	20	21	22	23	24	25
Data received	5F	F6	85	F5	99	52	25	23	54	54	45	D3	54
I²C bus Data out	5F	F6	85	E4	88	41	14	12	43	54	45	D3	54

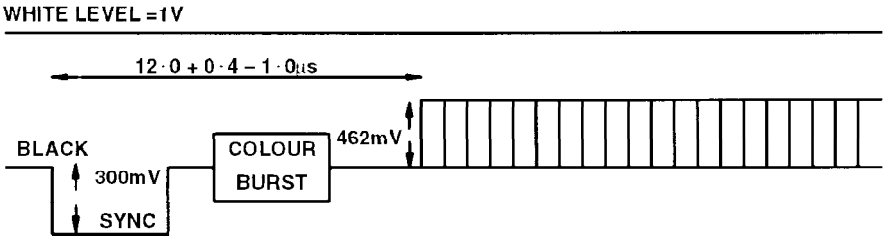
Notes: The I²C bus data in bytes 16 to 21 has had a one subtracted from each nibble to obtain actual data.
The example decodes to BBC 1, 7 August 1992, 15 hours, 12 minutes, 43 seconds British Summer Time or 14:12:43 Greenwhich Mean Time. The Local Time Offset (LTO) is + 1 hour.
SPL 1 & 2 decode as "TEST" when parity is removed.

Calendar date	Modified Julian Date	Day	Number
17:11:1858	00000	Wednesday	0
31:01:1982	45000	Sunday	4
01:01:1992	48622	Wednesday	0
01:01:1993	48988	Friday	2
13:01:1993	49000	Wednesday	0
01:01:1994	49353	Saturday	3
01:01:1995	49718	Sunday	4
10:10:1995	50000	Tuesday	6

Table 3. Modified Julian Date for various calendar dates

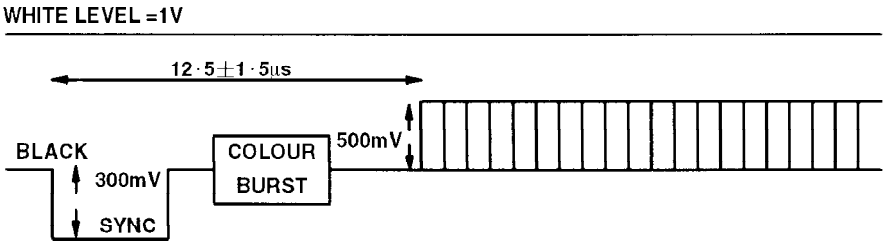
The day number is found from the equation MJD mod (7), i.e. divide by 7 and keep the integer remainder.

Video waveform of packet 8/30/2 (PDC)



For a $1V_{pp}$ signal, as shown, the data is $462mV_{pp}$ = 66% of picture. Time is measured from the negative sync edge to the peak of the seventh clock run–in pulse.

Video waveform of data line 16 (VPS)



For a $1V_{pp}$ video signal, as shown, the data is $500mV_{pp}$, modulation depth 71·4%. Time is measured from the negative sync edge to the start of data.

ORDER OF DATA OUTPUT ON THE I²C BUS

BIT ORDER		PDC DATA		BIT VALUE		VPS data
byte 1	bit 7	byte 16	bit 0 – CNI b9	———	reserved	byte 11
	bit 6		bit 1 – CNI b10	64	network (or programme provider)	
	bit 5		bit 2 – PIL b1	16		
	bit 4		bit 3 – PIL b2	8		
	bit 3	byte 17	bit 0 – PIL b3	4	day	
	bit 2		bit 1 – PIL b4	2		
	bit 1		bit 2 – PIL b5	1		
	bit 0		bit 3 – PIL b6	8		
byte 2	bit 7	byte 18	bit 0 – PIL b7	4		byte 12
	bit 6		bit 1 – PIL b8	2	month	
	bit 5		bit 2 – PIL b9	1		
	bit 4		bit 3 – PIL b10	16		
	bit 3	byte 19	bit 0 – PIL b11	8		
	bit 2		bit 1 – PIL b12	4	hour	
	bit 1		bit 2 – PIL b13	2		
	bit 0		bit 3 – PIL b14	1		
byte 3	bit 7	byte 20	bit 0 – PIL b15	32		byte 13
	bit 6		bit 1 – PIL b16	16		
	bit 5		bit 2 – PIL b17	8		
	bit 4		bit 3 – PIL b18	4	minute	
	bit 3	byte 21	bit 0 – PIL b19	2		
	bit 2		bit 1 – PIL b20	1		
	bit 1		bit 2 – CNI b5	8		
	bit 0		bit 3 – CNI b6	4		
byte 4	bit 7	byte 22	bit 0 – CNI b7	2	country	byte 14
	bit 6		bit 1 – CNI b8	1		
	bit 5		bit 2 – CNI b11	32		
	bit 4		bit 3 – CNI b12	16		
	bit 3	byte 23	bit 0 – CNI b13	8	network (or programme provider)	
	bit 2		bit 1 – CNI b14	4		
	bit 1		bit 2 – CNI b15	2		
	bit 0		bit 3 – CNI b16	1		
byte 5	bit 7	byte 14	bit 0 – PCS b1	2	status (define the analog sound	byte 5
	bit 6		bit 1 – PCS b2	1	transmission system)	
	bit 5		bit 2 – MI	1	mode indicator	
	bit 4		bit 3 – unallocated			
	bit 3	byte 15	bit 0 – CNI b1	128		
	bit 2		bit 1 – CNI b2	64		
	bit 1		bit 2 – CNI b3	32	country	
	bit 0		bit 3 – CNI b4	16		
byte 6	bit 7	byte 24	bit 0 – PTY b1	128		byte 15
	bit 6		bit 1 – PTY b2	64		
	bit 5		bit 2 – PTY b3	32		
	bit 4		bit 3 – PTY b4	16	programme type	
	bit 3	byte 25	bit 0 – PTY b5	8		
	bit 2		bit 1 – PTY b6	4		
	bit 1		bit 2 – PTY b7	2		
	bit 0		bit 3 – PTY b8	1		
byte 7	bit 7	byte 13	bit 0 – LC1 b1	2	Label Channel Identifier	– set to 1
	bit 6		bit 1 – LC1 b2	1	Interleaved up to four PIL messages	– set to 1
	bit 5		bit 2 – LUF	1	Label Update Flag (LUF)	– set to 1
	bit 4		bit 3 –PRF	1	Prepare to Record Flag	– set to 1
	bit 3		– set to 1			– set to 1
	bit 2		– set to 1			– set to 1
	bit 1		– set to 1			– set to 1
	bit 0		– set to 1			– set to 0

NOTE: Data is output on the I²C bus MSB first

Format 1. Order of UDT data output on the I²C bus

OUTPUT		INPUT			
byte 1	bit 7	byte 13	bit F–		
	bit 6		bit E–		
	bit 5		bit D–		
	bit 4		bit C–		
	bit 3		bit B–		
	bit 2		bit A–		
	bit 1		bit 9–		
	bit 0		bit 8–	**Network**	
byte 2	bit 7	byte 14	bit 7–	**Identification**	
	bit 6		bit 6–	**Code**	
	bit 5		bit 5–		
	bit 4		bit 4–		
	bit 3		bit 3–		
	bit 2		bit 2–		
	bit 1		bit 1–		
	bit 0		bit 0		
byte 3	bit 7	byte 15	bit 7–	reserved	
	bit 6		bit 6–	sign 0 = + 1 = –	
	bit 5		bit 5–	8	
	bit 4		bit 4–	4 **Time**	
	bit 3		bit 3–	2 **Offset**	
	bit 2		bit 2–	1 **Code**	
	bit 1		bit 1–	0·5	
	bit 0		bit 0–	reserved	
byte 4	bit 7	byte 16	bit 7–		
	bit 6		bit 6–	reserved	
	bit 5		bit 5		
	bit 4		bit 4		
	bit 3		bit 3–		
	bit 2		bit 2–	ten thousands	
	bit 1		bit 1–		
	bit 0		bit 0–		M
byte 5	bit 7	byte 17	bit 7–		
	bit 6		bit 6–	thousands	
	bit 5		bit 5–		
	bit 4		bit 4–		J
	bit 3		bit 3–		
	bit 2		bit 2–	hundreds	
	bit 1		bit 1–		
	bit 0		bit 0–		D
byte 6	bit 7	byte 18	bit 7–		
	bit 6		bit 6–	tens	
	bit 5		bit 5–		
	bit 4		bit 4–		
	bit 3		bit 3–		
	bit 2		bit 2–	units	
	bit 1		bit 1		
	bit 0		bit 0–		

NOTE: Data is output on the I²C bus MSB first

OUTPUT		INPUT			
byte 7	bit 7	byte 19	bit 7–		
	bit 6		bit 6–	hours tens	
	bit 5		bit 5–		
	bit 4		bit 4–		
	bit 3		bit 3–		
	bit 2		bit 2–	houts units	
	bit 1		bit 1–		
	bit 0		bit 0–		U
byte 8	bit 7	byte 20	bit 7–		
	bit 6		bit 6–	minutes tens	
	bit 5		bit 5–		
	bit 4		bit 4–		
	bit 3		bit 3–		T
	bit 2		bit 2–	minutes units	
	bit 1		bit 1–		
	bit 0		bit o–		
byte 9	bit 7	byte 21	bit 7–		
	bit 6		bit 6–	seconds tens	
	bit 5		bit 5–		C
	bit 4		bit 4–		
	bit 3		bit 3–		
	bit 2		bit 2–	seconds units	
	bit 1		bit 1–		
	bit 0		bit 0–		
byte 10	bit 7	byte 22	bit F–		
	bit 6		bit E–		
	bit 5		bit D–		
	bit 4		bit C–		
	bit 3		bit B–		
	bit 2		bit A–		
	bit 1		bit 9–		
	bit 0		bit 8–	**Short Programme**	
byte 11	bit 7	byte 23	bit 7–	**Label 1**	
	bit 6		bit 6–		
	bit 5		bit 5–		
	bit 4		bit 4–		
	bit 3		bit 3–		
	bit 2		bit 2–		
	bit 1		bit 1–		
	bit 0		bit 0–		
byte 12	bit 7	byte 24	bit F–		
	bit 6		bit E–		
	bit 5		bit D–		
	bit 4		bit C–		
	bit 3		bit B–		
	bit 2		bit A–		
	bit 1		bit 9–		
	bit 0		bit 8–	**Short Programme**	
byte 13	bit 7	byte 25	bit 7–	**Label 2**	
	bit 6		bit 6–		
	bit 5		bit 5–		
	bit 4		bit 4–		
	bit 3		bit 3–		
	bit 2		bit 2–		
	bit 1		bit 1–		
	bit 0		bit 0–		

Order of header TIME data output on the I²C bus

OUTPUT		INPUT		
byte 1	bit 7	byte 38	bit 3	**Most**
	bit 6		bit 2	**Significant**
	bit 5		bit 1	**Digit**
	bit 4		bit 0	
	bit 3	byte 39	bit 3	
	bit 2		bit 2	
	bit 1		bit 1	
	bit 0		bit 0	
byte 2	bit 7	byte 40	bit 3	
	bit 6		bit 2	
	bit 5		bit 1	
	bit 4		bit 0	
	bit 3	byte 41	bit 3	
	bit 2		bit 2	
	bit 1		bit 1	
	bit 0		bit 0	
byte 3	bit 7	byte 42	bit 3	
	bit 6		bit 2	
	bit 5		bit 1	
	bit 4		bit 0	
	bit 3	byte 43	bit 3	
	bit 2		bit 2	
	bit 1		bit 1	
	bit 0		bit 0	
byte 4	bit 7	byte 44	bit 3	
	bit 6		bit 2	
	bit 5		bit 1	
	bit 4		bit 0	
	bit 3	byte 45	bit 3	**Least**
	bit 2		bit 2	**Significant**
	bit 1		bit 1	**Digit**
	bit 0		bit 0	

NOTE: Data is output on the I²C bus MSB first

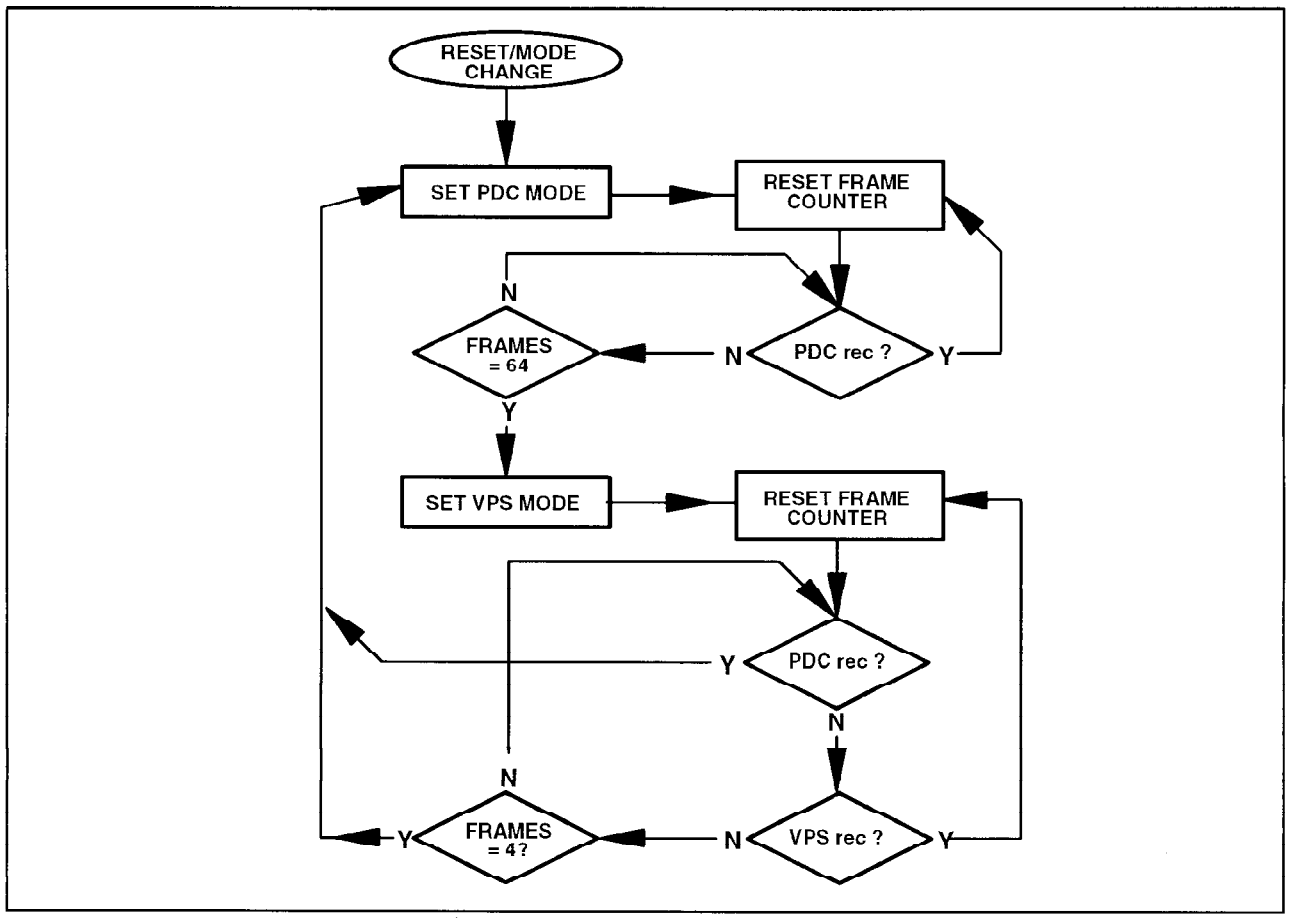


Fig. 4 Normal mode PDC/VPS switching

* The operation of the MV1822, in the presence of both Line 16 (VPS) and packet 8/30/2, follows the guide lines of the EBU Code Of Practice, SPB 459 Revision 2, February 1992, page 49:

"–when both Line 16 (VPS) and teletext delivered labels are available simultaneously, decoders should default to the teletext delivered service."

The counter is incremented once/frame.

One line =64µs One frame = 625 lines

PDC timeout count = 64 frames = 625 x 64µs x 64 = 2·65s
VPS timeout count = 4 frames = 625 x 64µs x 4 = 160ms

VPS only mode

The flow diagram above is not relevant.

For more information about all Zarlink products visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE