GEC PLESSEY
SEMICONDUCTORS

MAY 1996

D.S. 3908 2.1

MV1817

SINGLE CHIP TELETEXT DECODER FOR 625 LINE OPERATION

(Supersedes version in April 1994 Consumer IC Handbook, HB3120–2.0)

The MV1817 Television Data Service, TDS, IC incorporates all the features of the MV1815 with identical registers, so that MV1815 register control is software compatible. Additional TDS features are controlled by registers with addresses above those of the MV1815. A 2K/page system is included to enable extension packets to be stored with the display page data and page header data.

FEATURES

Acquisition

- Two page related data acquisition circuits
- On chip adaptive slicers for data and sync
- Accepts all data packets
- Advanced Header and Instant Page Clear working

Display

- High resolution 15x10 pixel characters
- Multi–lingual capability
- 26 display rows

Memory

- Up to 510 pages in one 4 bit organised DRAM
- 2K or 1K bytes per page

Synchronisation

- Three vertical time base modes:–
  - 312½–312½ interlaced
  - 312 – 312 non–interlaced – default
  - 312 – 313 non–interlaced
- Line (H) and field (V) sync inputs
- Full field operation
- On chip video switch

I²C bus etc.

- I²C bus interface bus to microcontroller
- I²C bus is released during power down
- Software compatible with MV1815
- Software maskable EVENT interrupts
- Register to indicate language variant

ORDERING INFORMATION

MV1817–3 CG DPAS – All Europe version
MV1817–3 CG GPBR – All Europe version

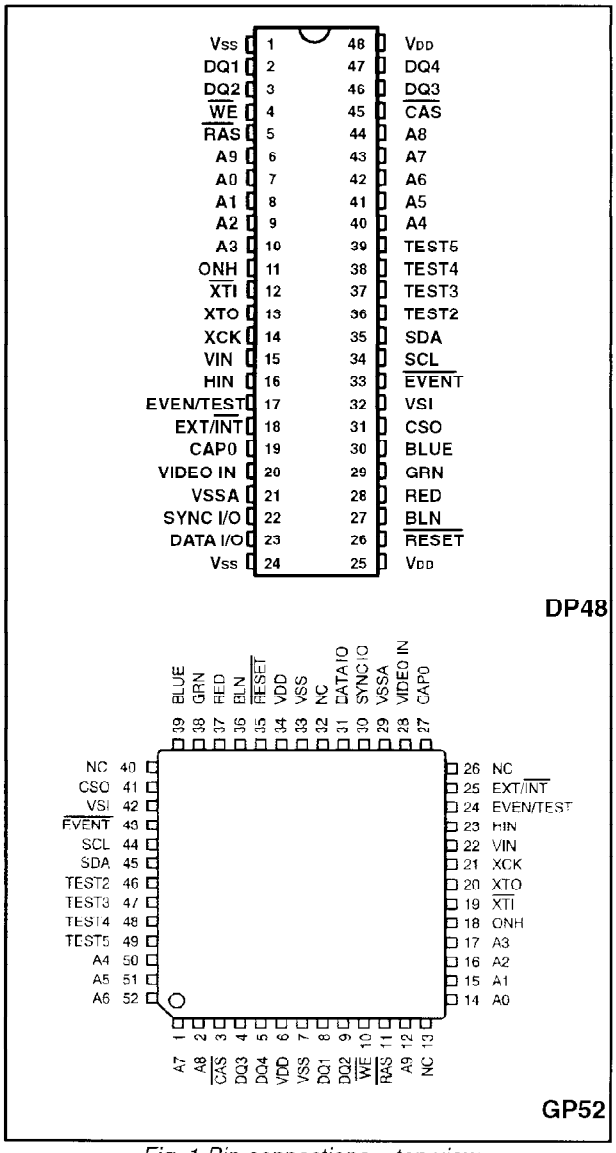

Fig. 1 Pin connections – top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	–0.3V to +7.0V
All inputs	–0.3V to V_{DD}+0.3V
Operating temperature	0°C to +70°C
Storage temperature	–65°C to 150°C

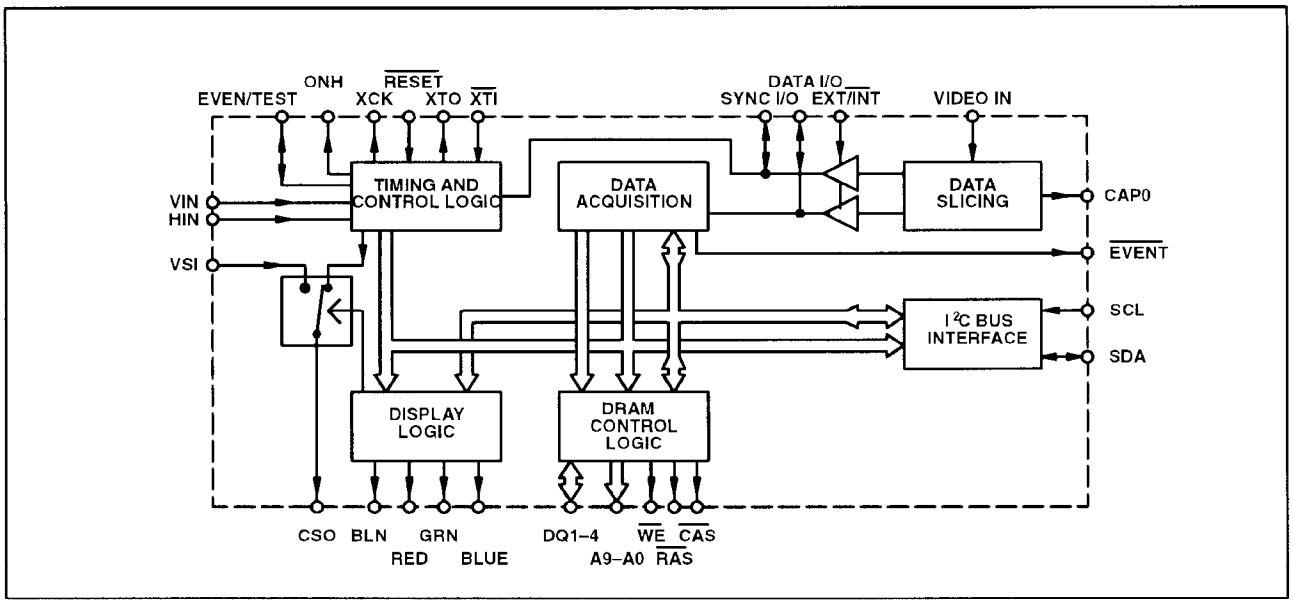

Fig. 2 Functional block diagram

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency (preferred)	6.93750MHz. AT cut
Tolerance over operating temperature range	±50ppm
Tolerance overall	±100ppm
Nominal load capacitance	30pF
Equivalent series resistance	<20Ω

ELECTRICAL CHARACTERISTICS

T_{amb}= 0°C to +70°C, V_{DD}= +5V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	25, 48	4.5	5.0	5.5	V	
Supply current	25, 48		80	140	mA	V_{DD}=5.5V White test screen
Video input, VSI	20, 32					Acquisition from TV lines 6–22 and 318–335
Voltage amplitude		0.7	1.0	2.0	V_{pp}	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	220nF input capacitor
CAP0	19					
Capacitor value			220		nF	Connected to GND
Capacitor tolerance		−10%		+10%		
Effective series resistance				5	Ω	1MHz
Sync I/O & Data I/O	22, 23					Acquisition from TV lines 2–22 and 314–335, see note 1.
Output voltage High (Data I/O only)		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=−2.0mA Sync I/O is an open drain output.
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Input voltage Low		0		$0.2V_{DD}$	V	
Input voltage High		$0.8V_{DD}$		V_{DD}	V	
Input current Low		−10		+10	µA	V_{IN}=V_{SS} or V_{DD}

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= 0°C to +70°C, V_{DD}= +5V +10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
EXT/INT	18					75k (nom) pull–down resistor
Input voltage Low		0		$0.2V_{DD}$	V	
Input voltage High		$0.8V_{DD}$		V_{DD}	V	
Input current Low		–10		+10	µA	$V_{IN}=V_{SS}$
Input current High		18	67	275	µA	$V_{IN}=V_{DD}$
XTI input	12					1M (nom) resistor to XTO
Input voltage Low		0		$0.2V_{DD}$	V	
Input voltage High		$0.8V_{DD}$		V_{DD}	V	
Input current Low		–0.5	–5.0	–20	µA	$-0.3 < V_{IN} < V_{IL}$ max
Input current High		0.5	1.5	20	µA	V_{IH} min$<V_{IN}<(V_{DD}+0.3)$
XTO output	13					
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–0.1mA
Output voltage Low			0.2	0.4	V	I_{OL}=0.1mA
Frequency			6.9375		MHz	±100ppm
I²C bus SCL, SDA Schmitt inputs	34, 35					
Input voltage Low		0		1.5	V	
Input voltage High		3.0		V_{DD}	V	
Output voltage Low			0.1	0.6	V	I_{OL}=6.0mA
SCL Clock Frequency			750	775	kHz	
Hysteresis voltage			0.4		V	
EVENT	33					75k (nom) pull–up resistor
Output voltage Low			0.2	0.4	V	I_{OL}=6.0mA open drain
RESET, Schmitt input	26					75k (nom) pull–up resistor
Threshold voltage falling		1.4	1.9			
Threshold voltage rising			3.1	3.8	V	
Hysteresis voltage			1.2		V	
Input current Low		–18	–67	–275	µA	$V_{IN}=V_{SS}$
Input current High		–10		+10	µA	$V_{IN}=V_{DD}$
VIN, HIN, Schmitt input	15, 16					
Threshold voltage falling		1.4	1.9			
Threshold voltage rising			3.1	3.8	V	
Hysteresis voltage			1.2		V	
Input current Low		–10		+10	µA	$V_{IN}=V_{SS}$
Input current High		–10		+10	µA	$V_{IN}=V_{DD}$
VIN pulse width		32			µs	
HIN pulse width		1			µs	at 90% level
VIN rise time				18	µs	10% to 90% level
HIN rise time				6	µs	10% to 90% level

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= 0°C to 170°C, V_{DD}= 15V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
ONH, XCK	11, 14					See note 2
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Red, Green, Blue	28, 29					
Output voltage High	30	$0.9V_{DD}$	$0.95V_{DD}$		V	I_{OH}=–8mA
Output voltage Low			0.2	0.4	V	I_{OL}=8mA
Tri–state leakage current		–10		10	µA	
Blank	27					
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–12mA
Output voltage Low			0.2	0.4	V	I_{OL}=12mA
CSO	31					With typical ac load of 360Ω
Output voltage swing		0.1		1.5	V_{PP}	Text mode only. See note 3
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–0.2mA with CSOT bit =1
Output voltage Low			0.2	0.4	V	I_{OL}=1.6mA with CSOT bit =1
Even output/Test input (Schmitt)	17					75k (nom) pull–down resistor
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Threshold voltage falling		1.4	1.9			
Threshold voltage rising			3.1	3.8	V	
Hysteresis voltage		0.6	1.2		V	
Input current Low		–10		–10	µA	V_{IN}=V_{SS}
Input current High		18	67	275	µA	V_{IN}=V_{DD}
Data DQ1 – DQ4	2, 3					75k (nom) pull–up resistor
Output voltage High	46, 47	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Input voltage Low		0		0.8	V	
Input voltage High		2.0		V_{DD}	V	
Input current Low		–18	–67	–275	µA	V_{IN}=V_{SS}
Input current High		–10		+10	µA	V_{IN}=V_{DD}
Address A0 – A9	4 – 10					See note 4
$\overline{RAS}$, $\overline{CAS}$, WE	40 – 45					
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}= –2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA

NOTE1. Acquisition window is wider when sliced data is supplied to DATA I/O to accommodate satellite transmissions.
NOTE 2 XCK output will be 6.9375MHz with XCKH=0 in register TADD, or 13.875Mhz with XCKH=1.
NOTE 3. CSO output voltage when in Picture or Mix modes will depend on the size of the video signal applied to VSI pin 32, together with the attenuation due to the internal video switch (30Ω nom) and the external load on pin 31. In these modes the video signal at pin 32 is switched straight through to pin 31. The maximum current allowed through the video switch is 24 mA.
NOTE 4. Capacitive loading on $\overline{RAS}$ and $\overline{CAS}$ should not exceed 20pF per pin.

Output voltage high specification ensures the output will also drive TTL levels of V_{DD}–2.1V at the specified current.

Pin N0	Name	Pin Description
1, 24	V_{SS}	Power ground 0V, both pins must be connected.
2, 3, 46, 47	DQ1–4	DRAM data lines, with internal 75k pull–up resistors.
4	$\overline{WE}$	DRAM write enable.
5	$\overline{RAS}$	DRAM row address strobe.
6–10, 40–44	A9, A0–8	DRAM address outputs.
11	ONH	On hours output.
12	$\overline{XTI}$	Crystal input or external clock input.
13	XTO	Crystal output.
14	XCK	Divided output of VCO clock, default 6.9375MHz. If XCKH bit in TADD register is set high, the output is 13.875MHz.
15	VIN	Vertical sync input positive pulse. If bit VINV in MODE register is set high, the signal may be a negative pulse.
16	HIN	Horizontal sync input positive pulse. If bit HINV in MODE register is set high, the signal may be a negative pulse.
17	EVEN/TEST	Even output is enabled by bits IOE and EOE in SYNCSW register. If EVEN output is not used it should be left open circuit. TEST input is used for factory testing. An internal 75k pull–down resistor is included.
18	EXT/$\overline{INT}$	Control pin for SYNC I/O and DATA I/O, with internal 75k pull–down. When high, supply sliced sync and data.
19	CAP0	Black level reference capacitor.
20	VIDEO IN	PAL composite signal with negative syncs.
21	VSSA	Analog ground.
22	SYNC I/O	Sliced sync input/output, (open drain output).
23	DATA I/O	Sliced data input/output, (push–pull output).
25, 48	V_{DD}	Power, +4.5V to +5.5V, both pins must be connected.
26	$\overline{RESET}$	Active low reset input, with 75k pull up–resistor.
27	BLN	Blanking output, high power push–pull driver.
28	RED	Red output, high power push–pull tri–state driver.
29	GRN	Green output, high power push–pull tri–state driver.
30	BLUE	Blue output, high power push–pull tri–state driver.
31	CSO	Composite sync output generated in text modes. In picture modes, connected to VSI through <30Ω video switch, see Fig. 6.
32	VSI	Composite video switch input.
33	$\overline{EVENT}$	Active low open drain output interrupt to microcontroller, with internal 75k pull–up.
34	SCL	Standard I^2C bus serial clock input.
35	SDA	Standard I^2C bus serial data input/output. Address is 0010 001R/$\overline{W}$ (22hex).
36	TEST2	For factory test only, do not connect.
37	TEST3	For factory test only, do not connect.
38	TEST4	For factory test only, do not connect.
39	TEST5	for factory test only, do not connect.
45	$\overline{CAS}$	DRAM column address strobe.

PINS	TEST	TEST LEVELS	NOTES
SDA &SCL	Human body model	1kV on 100pK through 1k5Ω	<15% LTPD
SDA & SCL	Machine model	100V on 200pF through 0Ω & <500nH	
All others	Human body model	2kV on 100pF through 1k5Ω	Meets Mil Std. 883D class 2 requirements
All others	Machine model	200V on 200pF through 0Ω & <500nH	

LTPD=Lot Tolerant Percent Defective

ESD data

ADDRESS dec/hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	RADD	A17	A16	IAI	RA4	RA3	RA2	RA1	RA0	W	00
0/0	ACONA	ACQ	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
1/1	STORA	STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	W	02
2/2	PGS1A	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
3/3	PGS2A	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	20
4/4	PGS3A	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	00
5/5	ACONB	$\overline{\text{HLD}}$	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
6/6	STORB	STB7	STB6	STB5	STB4	STB3	STB2	STB1	STB0	W	03
7/7	PGS1B	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
8/8	PGS2B	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	00
9/9	PGS3B	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	88
10/A	RECON	WI0	WI24	WI25	PINB	PINA	FF	CDB	CDA	W	00
11/B	DISCON1	INV	RLH	DSB	CLS	CUR	BLC	LS3	UDI	W	00
12/C	DISCON2	LS0	LS1	LS2	MGS	IHD	SPH	BX1	BX0	W	00
13/D	DISCON3	TXT	MIX	INT	REV	UDK	SPOS	ST2	ST1	W	00
14/E	DISCON4	BXP	BXH	BXT	BXS	DHT	DHB	SG2	SG1	W	00
15/F	HADD	A15	A14	A13	A12	A11	A10	A9	A8	W	00
16/10	LADD	A7	A6	A5	A4	A3	A2	A1	A0	W	00
17/11	WDATA	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	W	00
19/13	SCROLL	WI29	MV	CRL	SRA4	SRA3	SRA2	SRA1	SRA0	W	00
20/14	SYNCSW	ESS	–	BXSDEL	CSOT	IOE	EOE	SEN	SVS	W	00
21/15	MODE	MD3	MD2	MD1	312:313	VHLD	HVEN	HINV	VINV	W	24
22/16	TADD	–	A18	RESET	XCKH	2K/ST	DISC	ADEC	DST8	W	00
23/17	DISPST	DSTI7	DST6	DST5	DST4	DST3	DST2	DST1	DST0	W	00
24/18	DPOS	V3	V2	V1	V0	H3	H2	H1	H0	W	7B
25/19	ENABLE	NPR	VHR	830	X/24A	X/28	X/27	X/26	X/24B	W	EE
26/1A	ACCENT	APA	APB	C8APIA	C8APIB	SCAPIA	SCAPIB	–	AHEN	W	00
0/0	EVENTA	NPR	VHR	830A	X/24	X/28	X/27	X/26	C9	R	–
1/1	EVENTB	NPR	VHR	830B	X/24	X/28	X/27	X/26	C8	R	–
2/2	CBITSA	C14	C13	C12	C11	C10	C7	C6	C5	R	–
3/3	PGR1A	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
4/4	PGR2A	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
5/5	PGR3A	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
6/6	CBITSB	C14	C13	C12	C11	C10	C7	C6	C5	R	–
7/7	PGR1B	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
8/8	PGR2B	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
9/9	PGR3B	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
10/A	HAMMC	HC7	HC6	HC5	HC4	HC3	HC2	HC1	HC0	R	FF
17/11	RDATA	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	–
18/12	EXTEND	APIIA	APIIB	RSIND	–	CLSI	ONH	C9B	C9A	R	–
31/1F	STATUS	SL2	SL1	SL0	SR4	SR3	SR2	SR1	SR0	R	–

Table 1. Register details

WRITE REGISTERS

RADD

A17–16	Memory address
IAI	Inhibit auto increment
RA5–0	Register address

ACON A/B

ACQ	*Acquisition on*
MGC	Magazine compare
PBC	Page tens compare
PAC	Page units compare
SDC	Sub–code compare digit D
SCC	Sub–code compare digit C
SBC	Sub–code compare digit B
SAC	Sub–code compare digit A
$\overline{HLD}$	Hold display

PGS 1,2,3 A/B

SAS3–0	Sub–code digit A (LSD) select
SBS2–0	Sub–code digit B select
SCS3–0	Sub–code digit C select
SDS1–0	Sub–code digit D (MSD) select
PAS3–0	Page (units) select
PBS3–0	Page (tens) select
MS2–0	Magazine select

RECON

WI0	Write inhibit packet 0
WI24	Write inhibit packet 24
WI25	Write inhibit packet 25
PINB	Parity check inhibit Acquisition B
PINA	Parity check inhibit Acquisition A
FF	Full Field mode
CDB	Clear store disable Acquisition B
CDA	Clear store disable Acquisition A

DISCON1

INV	Invert display colours
RLH	Roll headers
DSB	Display acquisition circuit B (A if zero)
CLS	Clear current display store
CUR	Cursor enable
BLC	Block cursor
LS3	Language group select
UDI	Display update indicator

DISCON2

LS2–0	Language select
MGS	Magazine serial
IHD	Inhibit display rows 1–25
SPH	Suppress header
BX1–0	Boxing control bits

DISCON3

TXT	Text/ not picture
MIX	Mix text and picture
INT	Text interlace sync mode
REV	Reveal hidden text
UDK	Update key – inhibit rows 0–25
SPOS	Status line 2 position, top if set high
ST2	Display status line 2
ST1	Display status line 1

DISCON4

BXP	Box page number
BXH	Box header
BXT	Box time
BXS	Box status rows
DHT	Double height top
DHB	Double height bottom
SG2–1	Separated graphics control bits

HADD & LADD

A15–0	Memory address

WDATA

WD7–0	Write data byte to memory

SCROLL

WI29	Write inhibit packet 29
MV	Majority vote on framing code
CRL	Cursor lock
SRA4–0	Scroll value 0–23 only

SYNCSW

ESS	External sync source
BXSDEL	Box status delay by one character
CSOT	CSO TTL signal
IOE	Interlace output enable
EOE	Even output enable
SEN	Select enable SVS
SVS	Select VSI input as sync source

MODE

MD3	H sync mode 3
MD2	H sync mode 2
MD1	H sync mode 1
312:313	Non–interlace 312:313 mode
VHLD	Vertical sync half line delay (Fig. 9)
HVEN	H and V inputs enable
HINV	H invert
VINV	V invert

TADD

A18	Memory address
RESET	Reset to default state
XCKH	XCK output 13.875MHz or 6.9375MHz when low
2K/ST	2K/store mode
DISC	Disconnect display from acquisition
ADEC	Automatic memory decrement
DST8	Store number for display bit 8

DISPST

DST7–0	Store number for display bits 7–0

DPOS

V3–0	Vertical position in 2 line steps
H3–0	Horizontal position in 4 pixel steps

ENABLE

NPR	Enable NPR flag in read regs
VHR	Enable VHR flag in read regs
830	Enable 830 flag i read regs
X/24A	Enable X/24A flag in read regs
X/28	Enable X/28 flag in read regs
X/27	Enable X/27 flag in read regs
X/26	Enable X/26 flag in read regs
X/24B	Enable X/24 flag in read regs

ACCENT

APA–B	Accent protection A/B
C8APIA–B	C8 accent protection inhibit A/B
SCAPIA–B	Sub–code accent protection inhibit A/B
AHEN	Advanced headers enable

READ REGISTER

EVENT A/B

NPR	New page received flag
VHR	Valid header received flag
830A	Packet 8/30 format 1 received flag
830B	Packet 8/30 format 2 received flag
X/24	Packet X/24 received flag
X/28	Packet X/28 received flag
X/27	Packet X/27 received flag
X/26	Packet X/26 received flag
C8	Update indicator

PGR 1,2,3 A/B

SAR3–0	Sub–code digit A (LSD) received
SBR2–0	Sub–code digit B received
SCR3–0	Sub–code digit C received
SDR1–0	Sub–code digit D (MSD) received
PAR3–0	Page (units) received
PBR3–0	Page (tens) received
MR2–0	Magazine received

RDATA

RD7–0	Read data byte from memory

CBITS A/B

C14–12	Language select bits (C14 is LSB)
C11	Magazine serial
C10	Inhibit display
C7	Suppress header
C6	Sub–title
C5	News flash

HAMMC

HC7–0	Hamming counter

EXTEND

APII A/B	Accent protection inhibit indication A/B
RSIND	Reset indication
CLSI	Clear screen indicator
ONH	On hours flag
C9 A/B	Interrupted sequence bit Acq A/B

STATUS

SL2–0	Status language indication
SR4–0	Status revision indication
SL2–0=003	All Europe version

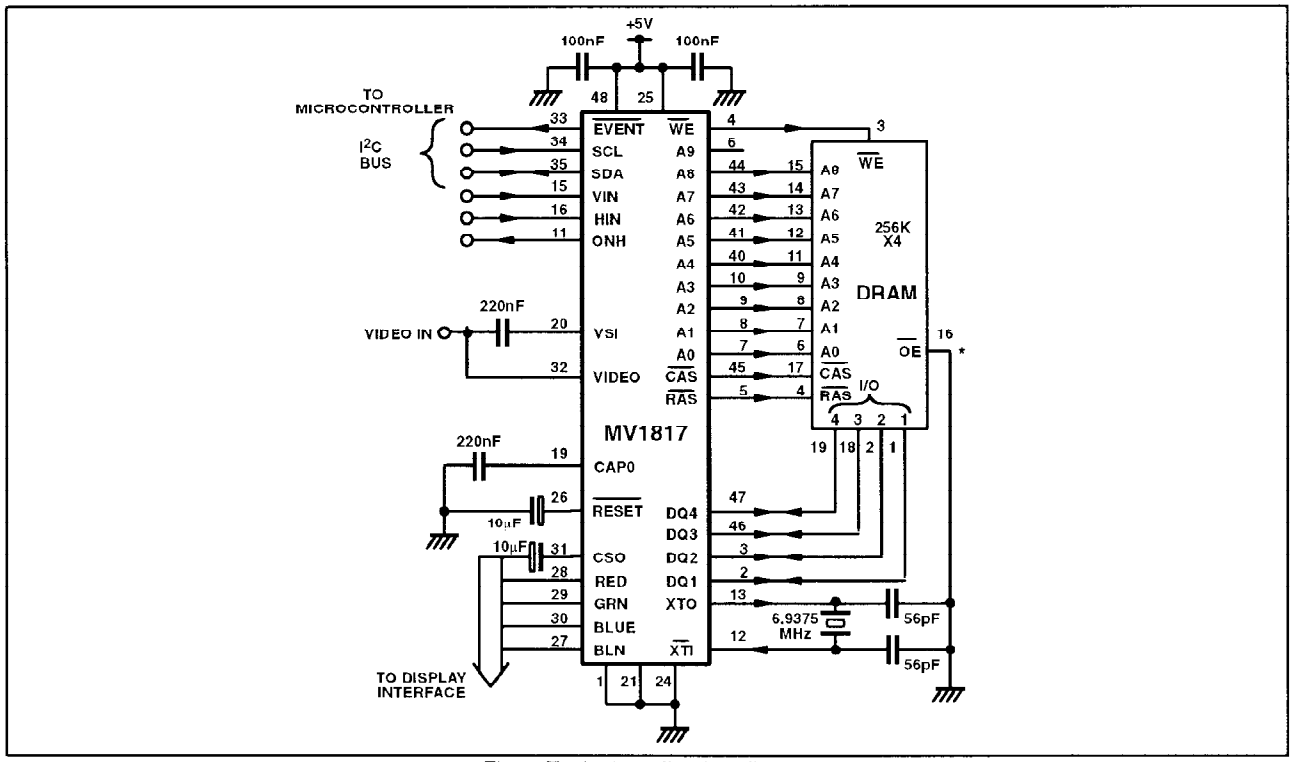

Fig. 3 Typical application diagram

* Note, on some DRAM devices $\overline{OE}$ should not be low during a write cycle. An inverted $\overline{WE}$ can be connected to $\overline{OE}$ in such cases.

I²C bus Interface – SCL and SDA.
Control of the MV1817 registers is through this interface. The I²C bus address is 0010 001 R/$\overline{W}$

The circuit works as a slave transmitter with bit eight set high or as a slave receiver with bit eight set low. In receive mode, the first data byte is written to RADD register, where the least significant five bits form the sub–address. The most significant three bits of RADD are data bits, see Table 1.

Automatic incrementing of the registers allows successive data bytes to be written to, or read from the registers. The automatic incrementing can be disabled by setting IAI bit five of RADD to one. Automatic increment can be changed to automatic decrement (for DRAM address NOT registers) by setting ADEC bit high in TADD register. All DRAM addresses may be accessed via the I²C bus interface.

When WDATA or RDATA registers are reached, the automatic incrementing accesses successive bytes of data in the DRAM starting from the current value of HADD and LADD. Automatic incrementing of registers will operate above WDATA from SCROLL register onwards.

MEMORY MAPS

The DRAM memory as viewed from the I²C bus is organised in 1024 (400hex) byte blocks, referred to as a store. Stores 0 and 1 in 1K/store mode are reserved for the non–display packets from acquisition A and B respectively. Stores A0 and B0 in 2K/store mode are reserved for the packets X/29 and 8/30 from acquisition A and B respectively.

The table below shows the start addresses for each store. The store numbers relate to the values in the STORA, STORB and DISPST registers.

1K/store	Start addresses hex TADD, RADD, HADD, LADD	2K/store
STORE 0	0 0 00 00	STORE A0
STORE 1	0 0 04 00	STORE B0
STORE 2	0 0 08 00	STORE 1 DISPLAY
STORE 3	0 0 0C 00	STORE 1 EXT PKTS
STORE 4	0 0 10 00	STORE 2 DISPLAY
STORE 5	0 0 14 00	STORE 2 EXT PKTS
STORE 6	0 0 18 00	STORE 3 DISPLAY
STORE 7	0 0 1C 00	STORE 3 EXT PKTS
	etc. until	
STORE 508	1 3 F0 00	STORE 254 DISPLAY
STORE 509	1 3 F4 00	STORE 254 EXT PKTS
STORE 510	1 3 F8 00	STORE 255 DISPLAY
STORE 511	1 3 FC 00	STORE 255 EXT PKTS

Table 2 Memory organisation

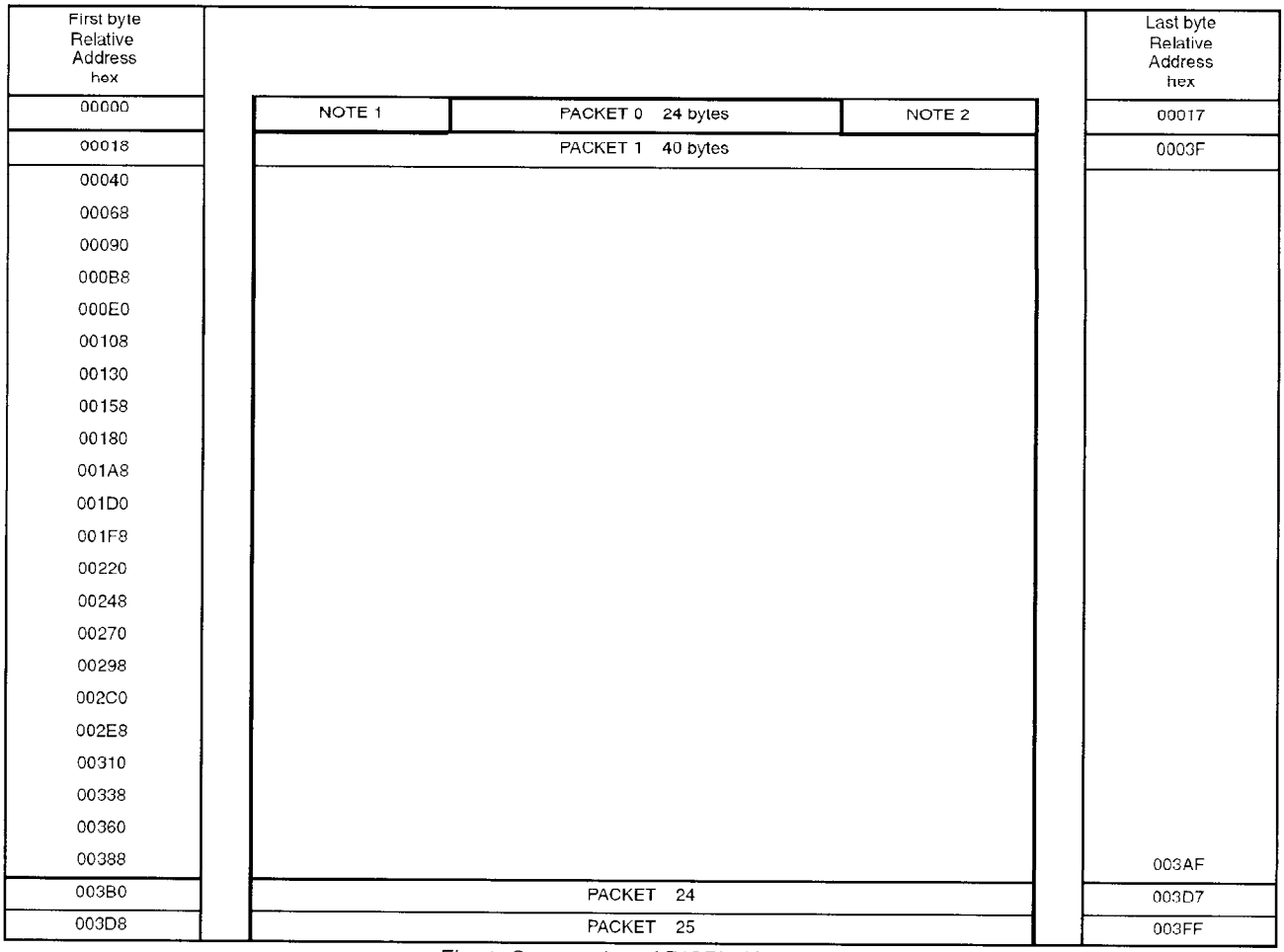

Fig. 4. Organsation of DISPLAY memory

Note 1. Page number, 8 bytes from store 0 (A0) with absolute addresses 000 to 007

Note 2. Time display, 8 bytes from store 0 (A0) with absolute addresses 008 to 00F

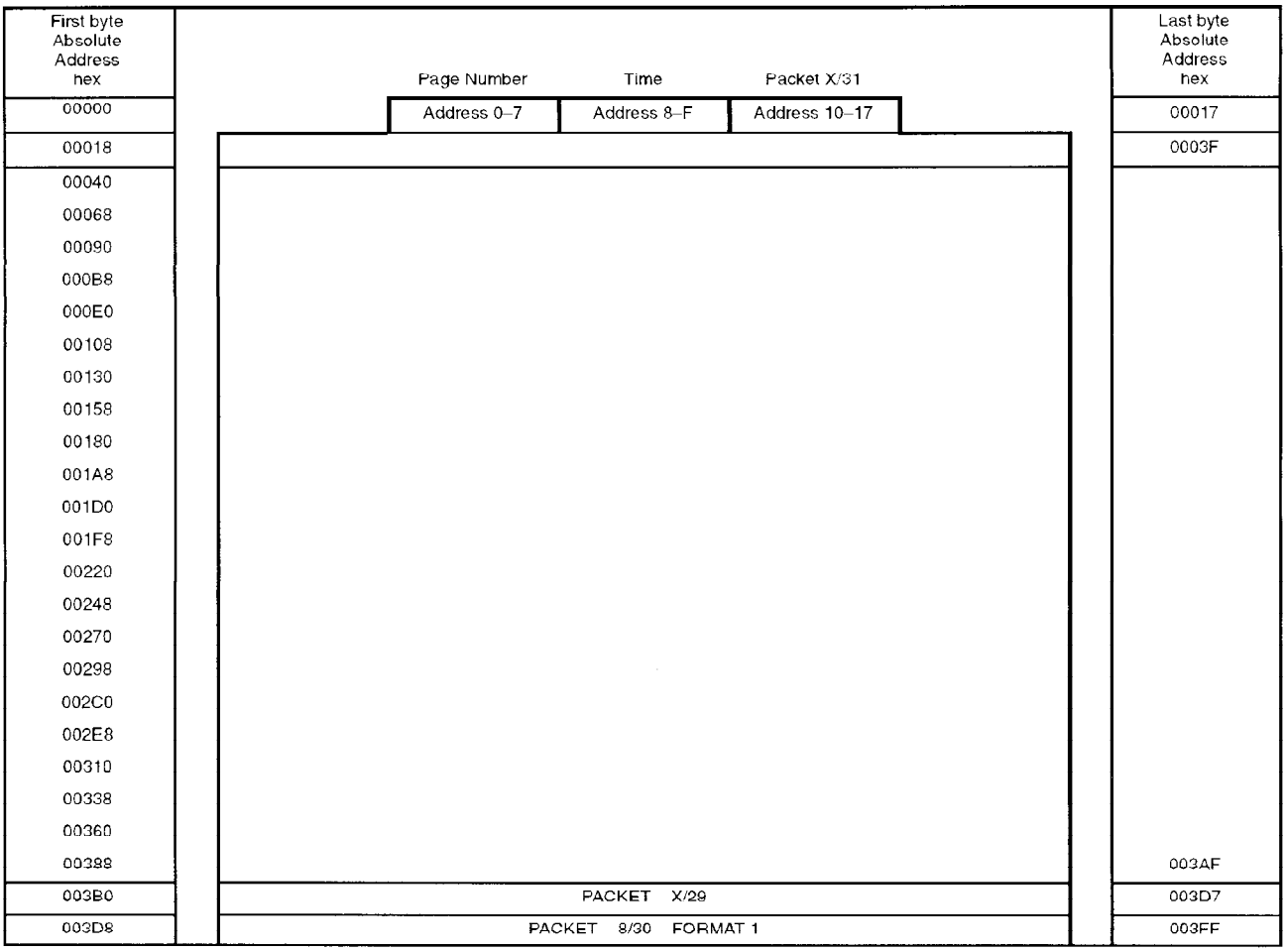

Fig. 5. Store 0 (A0) Memory organisation.

NOTE: Store 1 (B0) is organised similarly except that, in 1K/store mode it accepts acquisition circuit B packets X/26 etc. and packet 8/30 format 2 in the last row. To obtain addresses for store 1 (B0) add 400hex. Bytes 400 to 417hex are not used in store 1 (B0).

In 2K/store mode, all page related extension packets, X/26, X/27 and X/28, are directed to the store adjacent to the display store, see Table 2. Up to 23 of these packets are stored in the order received with no fixed location in the memory. The first four bytes with relative address 000 to 003 contain a copy of the related acquisition circuit data in CBITS and PGR1–3 registers in the same order. Bytes 004 to 017_{hex} are not used by the MV1817. The last two rows will not be used by the MV1817 since X/29 and 8/30 packets only go to stores A0 and B0 (or to stores 0 and 1 in 1K/store mode).

Synchronisation

In the usual configuration where a video signal is applied to the data and sync slicer, a composite sync output (CSO) is generated from the sliced video input. CSO can be modified by register bits to provide 312:312, 312:313 or 312.5:312.5 text syncs, or switch through the video switch input signal direct. If video syncs are selected with SEN=1 and SVS=1 (in SYNCSW register), the action of the 312:313 bit (in MODE register) is inhibited.

When the vertical synchronisation circuit finds a field sync datum, (see Fig. 6) it is disabled for 64 lines so that double field synchronisation is avoided.

If the display is to be synchronised to horizontal and vertical signals via the HIN and VIN pins, the HVEN enable bit in the MODE register must be set high. This will disable the action of interlace (INT) bit in DISCON3 register and also 312:313 bit in MODE register. HIN and VIN signals are normally positive pulses, but inverted signals may be applied provided that the appropriate HINV and VINV bits are set high in the MODE register. The leading edge of VIN pulse is sampled at –4.7µs and +27.3µs with respect to HIN pulse to establish which is the EVEN or ODD field, see Fig. 7. The VIN pulse should be at least 32µs minimum and the HIN pulse 1µs minimum.

If required, the vertical pulse may be delayed by half a line period by setting VHLD bit high in MODE register, see Fig. 8.

LS(3210)	0000	0001	0010	0011	0100	0101	0110	0111
TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH	ROMANIAN
2/3	£	#	#	£	é	ç	#	#
2/4	$	$	¤	$	ï	$	ů	$
4/0	@	§	É	é	à	¡	č	Ţ
5/B	←	Ä	Ä	°	ë	á	ť	Â
5/C	½	Ö	Ö	ç	ê	é	ž	Ş
5/D	→	Ü	Å	→	ù	í	ý	Ă
5/E	↑	^	Ü	↑	î	ó	í	ţ
5/F	#	_	_	#	#	ú	ř	ı
6/0	▒	°	é	ù	è	¿	é	ţ
7/B	¼	ä	ä	à	á	ü	á	â
7/C	‖	ö	ö	ò	ô	ñ	ě	ş
7/D	¾	ü	å	è	û	è	ú	ă
7/E	÷	ß	ü	ì	ç	à	š	î

LS(3210)	1000	1001	1010	1011	1100	1101	1110	1111
TABLE POSITION	POLISH	GERMAN	HUNGARIAN	TURKISH	DANISH	SERBO CROAT	CZECH	SOUTH AFRICAN
2/3	#	#	#	₺	£	#	#	£
2/4	ń	$	ú	ğ	$	$	ů	$
4/0	ą	§	É	İ	@	Č	č	ŉ
5/B	Ƶ	Ä	í	Ş	Æ	Ć	ť	ë
5/C	ś	Ö	Ö	Ö	Ø	Ž	ž	ê
5/D	Ł	Ü	Á	Ç	Å	Đ	ý	ù
5/E	ć	^	ű	Ü	↑	Š	í	é
5/F	ó	_	ő	Ğ	#	ë	ř	ï
6/0	ę	°	é	ı	▒	č	é	š
7/B	ż	ä	ó	ş	æ	ć	á	ä
7/C	ś	ö	ö	ö	ø	ž	ě	ô
7/D	ł	ü	á	ç	å	đ	ú	ü
7/E	ź	ß	ü	ü	÷	š	š	ö

Table 3 Narional Optional Characters. Language version 003.

ROW	COLUMN (bits 5, 6, 7 & 8)																	
	2	2a	3	3a	4	5	6	6a	7	7a	8	9	A	B	C	D	E	F
0			0			P			p		Á	Ë	Ö	Ý	ë	þ		
1	!		1		A	Q	a		q		À	Ę	ő	ź	í	ŕ	↑	
2	"		2		B	R	b		r		Ă	Ê	ó	ž	ì	ú	←	→
3			3		C	S	c		s		Ä	Í	Ø	á	î	û	¼	½
4			4		D	T	d		t		Â	Ì	Þ	à	ï	ü	¾	÷
5	%		5		E	U	e		u		Ą	Ï	Ŕ	â	ĭ	ú		
6	&		6		F	V	f		v		Ā	Î	Ř	ã	ľ	ý		
7	'		7		G	W	g		w		Æ	Ĭ	Ś	ă	Ľ	ą		
8	(		8		H	X	h		x		Ć	Ĺ	ś	ä	ň	°		
9	)		9		I	Y	i		y		Č	Ľ	Ť	æ	ó	ş		
A	*		:		J	Z	j		z		Ç	Ń	Ú	ć	ò	°		
B	+		;		K		k				Ď	Ň	Ù	đ	ő	·		
C	,		<		L		l				Đ	Ń	Ü	é	ö	ß		
D	-		=		M		m				É	Ó	Ű	è	ő	£		
E	.		>		N		n				È	Ô	Ű	é	ô	$		
F	/		?		O		o				Ë	Õ	Ů	ê	ø	#		

Table 4. Character ROM contents as viewed by the display. Language version 003.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes, like the control columns 0 and 1 listed in table 6.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
□ Characters in these positions are displayed according to the setting of LS(0–3) bits, see table 3.
When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown with black as forground colour. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

Graphic symbols to scale

Page closure.

In serial mode, any header will close a page being received.
In parallel mode, only a header from the selected magazine will close a page being received.

Advanced Header and Instant Page Clear *transmission systems.*

With these systems, the main page header packet is transmitted in the same VBI, before the associated data packets, without the standard 20ms page clearing interval. The MV1817 can be programmed to protect those associated data packets, in the same VBI, from erasure when the page is cleared. This feature is enabled for both systems by setting AHEN bit high in ACCENT register.

	INCLUDED IN MV1817- 3	NOT INCLUDED
CZECH	Ä Á Č Ď É Ě Í Ĺ Ľ Ň Ö Ó Ô Ŕ Ř Š Ś Ť Ü Ú Ů Ý Ź Ž ß § ° ä ď í ľ ň ö ó ô ŕ ü	
DENMARK	Æ æ Ø ø	
FRANCE	À Â Ç È É Ê Ë Ï Î Ô Û	Œ œ
HOLLAND	Ë ë	Ĳ ĳ
HUNGARY	Á Í Ó Ő Ú Ű á í ó ő ú ű	
ICELAND	Á Đ Í Ó Ö Þ Ú Ý Æ Ø ð ö þ ý æ ø	
ITALY	À È É Ì Í Ò Ù Ú í ú	
POLAND	Ą Ć Ę Ń Ó Ź $ § _	
ROMANIA	É Ě Ê Ĭ Ó é ě ê ĭ ó	
SPAIN	Á À Ã Ç É È Ï Í Ñ Ó Ò Õ Ŕ Ú Ü # · ª º → ↑ ã ä â ë ê ï î ô ò ö õ ŕ û	
TURKEY	Â Î Û â î û	

Table 5. Additional characters for the languages shown. Language version 003.

Accented characters added via X/26

These can be automatically locked in place on the screen by the MV1817 hardware, so that further reception of the page will not change accented characters to the level one fall–back characters. Whenever a page is cleared to spaces, the locked characters will be unlocked and also become spaces. Control of this feature is by setting APA/B bits in ACCENT register. The header should be cleared by software the first time a store is used to prevent random characters in the DRAM at power up from being locked. For pages where data is updated with C8 set, but clear page C4 is not set, the accent locking feature may be inhibited during current page reception by setting C8APIA/B bits. For rolling sub–coded pages where clear page C4 is not set, the accent locking feature may be inhibited during current page reception by setting SCAPIA.B bits. When these inhibit mechanisms are active, an indication is provided in EXTEND register by bits APIIA/B set high. They are set low when the current page is closed.

	0	1
0	Alpha Black	Graphic Black
1	Alpha Red	Graphic Red
2	Alph Green	Graphic Green
3	Alpha Yellow	Graphic Yellow
4	Alpha Blue	Graphic Blue
5	Alpha Magenta	Graphic Magenta
6	Alpha Cyan	Graphic Cyan
7	Alpha White [1]	Graphic White
8	Flash	Conceal Display [2]
9	Steady [1 2]	Contiguous Graphics [1 2]
A	End Box [1]	Separated Graphics [2]
B	Start Box [3]	No Action
C	Normal Height [1 2]	Black Background [1 2]
D	Double Height	New Background [2]
E	No Action	Hold Graphics
F	No Action	Release Graphics

Table 6. Control codes.

Notes:
1. Presumed set at the start of each display row.
2. Action "set at the current space", others are "set after the current space".
3. Two consecutive codes are transmitted, action takes place between them.

Sync switch register truth table

ESS	SEN	SVS	CSO output
0	0	X	VSI or digital sync selected by algorithm
0	1	0	Digital syncs
0	1	1	VSI switched through
1	X	X	Digital syncs from SYNC I/O

X=don't care.

Sync switch algorithm

The video signal will be switched through from VSI to CSO when:
TXT = 0 or MIX = 1 or TXT = 1 and BX1 = 1 and BX0 = 1.

EVEN output on TEST pin, truth table

IOE	EOE	CSO	Function
X	0	X	TEST configured as an input with an internal pull down resistor
0	1	INTERLACE	Enables EVEN output, which is held high.
1	1	INTERLACE	Enables EVEN output going high during the first field (lines 1–312½)
X	1	312:313	Enables EVEN output going high during the short field (312 lines)

X = don't care.

Note: CSO is not only dependent upon the state of the INT bit in DISCON4 register, but also on MIX and any other register bits which cause picture to be displayed, for example, UDK, BXP, BXH, BXT, BXS, or BX0–1 if start box codes are present on screen.

BOXING options and MIX mode, truth table

The bits BXP, BXH, BXT and BXS in DISCON4 register will BOX text into the picture when TXT and MIX mode are set, the BOXED text will retain its background colours. However, BOXED text using Box codes 0B in text together with BX0 or BX1 bits in DISCON2 will not override MIX and can be displayed as BOXED text by setting TXT & MIX bits low, or MIXED by setting MIX high. The BOXED STATUS ROWS can start at character position one by setting BXSDEL bit in SYNCSW register.

TXT	BX – 1.0		BX – n (n=P, H, T, S)	MIX	Status Area n	Boxed Text Areas		BASIC MODE
						Outside	Inside	
0	0.0		0	X	Picture	Picture	Picture	PICTURE
0	0.0		1	0	Boxed	Picture	Picture	
0	0.0		1	1	Mixed	Picture	Picture	
0	X.1	1.X	0	0	Picture	Picture	Text	NEWSFLASH
0	X.1	1.X	0	1	Picture	Picture	Mixed	
0	X.1	1.X	1	0	Boxed	Picture	Text	
0	X.1	1.X	1	1	Boxed	Picture	Mixed	
1	0.X	X.0	X	0	Text	Text	Text	TEXT
1	0.X	X.0	0	1	Mixed	Mixed	Mixed	
1	0.X	X.0	1	1	Boxed	Mixed	Mixed	
1	1.1		X	0	Text	Text	Picture	WINDOW
1	1.1		0	1	Mixed	Mixed	Picture	
1	1.1		1	1	Boxed	Mixed	Picture	

X = don't care.

BOX STATUS DELAY

When status rows 1 and/or 2 are enabled to be boxed into a picture or MIX text display, the first character in the row may be omitted and replaced by picture by setting the BXSDEL bit 5 in SYNCSW register high

SCROLL

A value in the range 0–23 can be used to move the text rows 1–23 up the screen, the rows 0, 24 and 25 remain fixed. A scroll value of 3 will cause text row 4 to be displayed in row 1. Text rows 1–3, in this example will appear in rows 21, 22 and 23 respectively. If half page expand is also used, by setting DHT in DISCON3 register, the text screen can be made to scroll through the expanded top half window. The position of the text in memory, is not affected by scroll, only the row addressing is changed to effect the display.

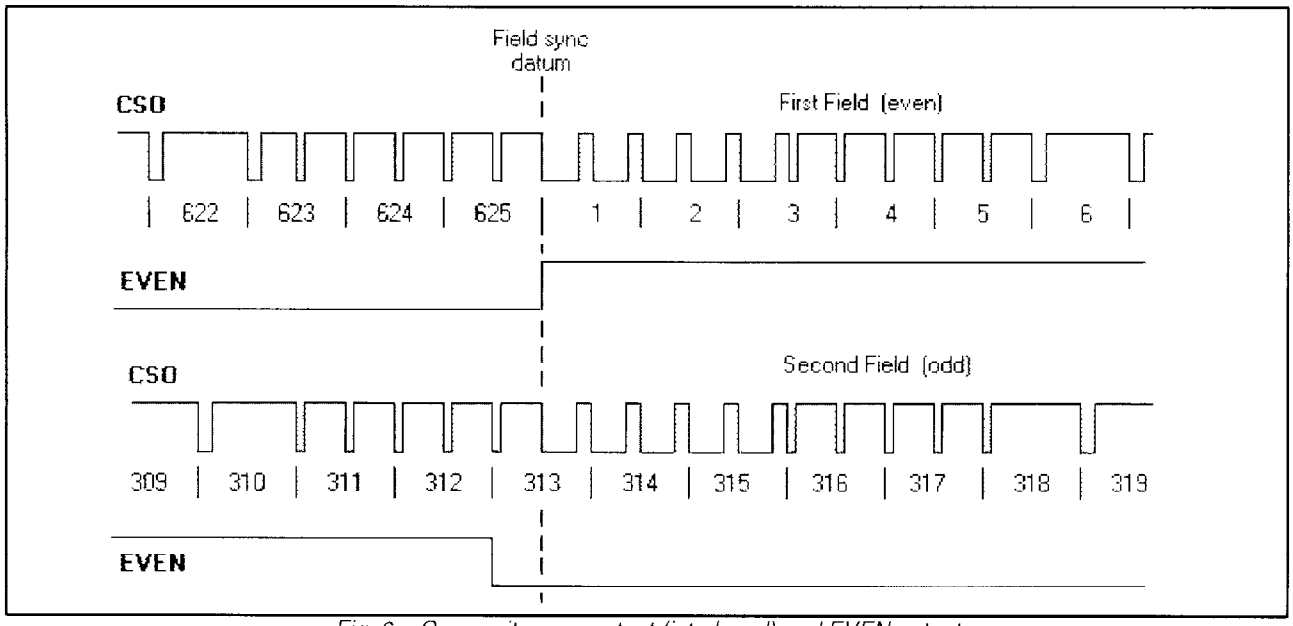

Fig. 6a. Composite sync output (interlaced) and EVEN output.

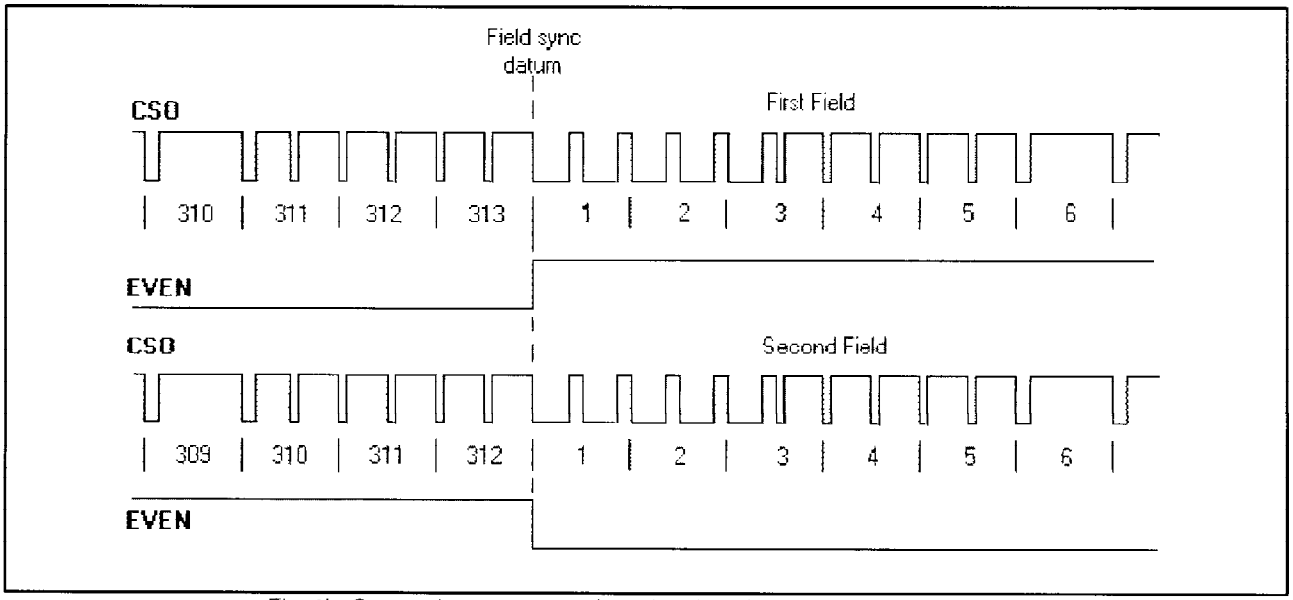

Fig. 6b. Composite sync output (non–interlaced 312:313) and EVEN output.

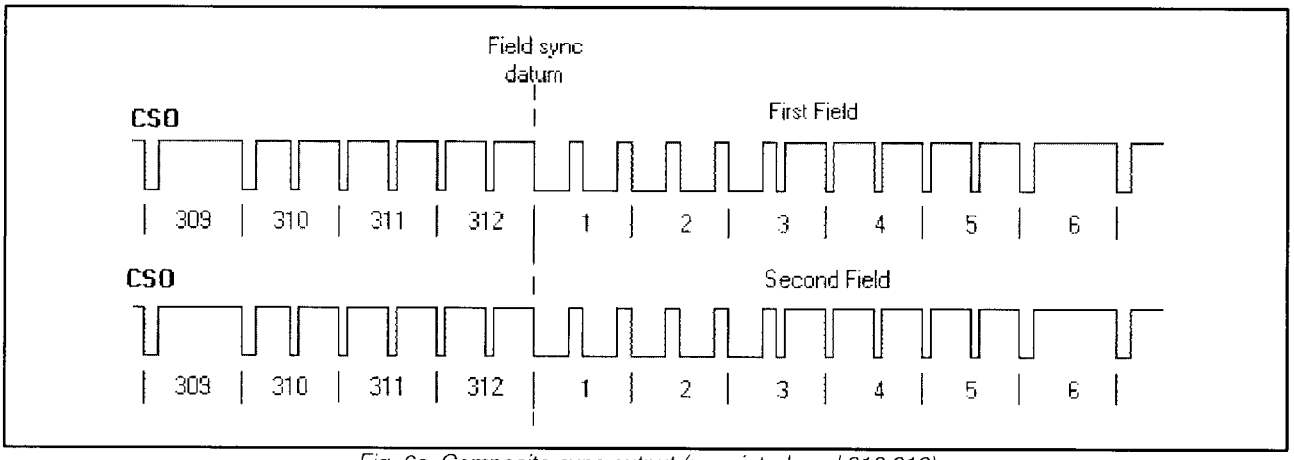

Fig. 6c. Composite sync output (non–interlaced 312:312).

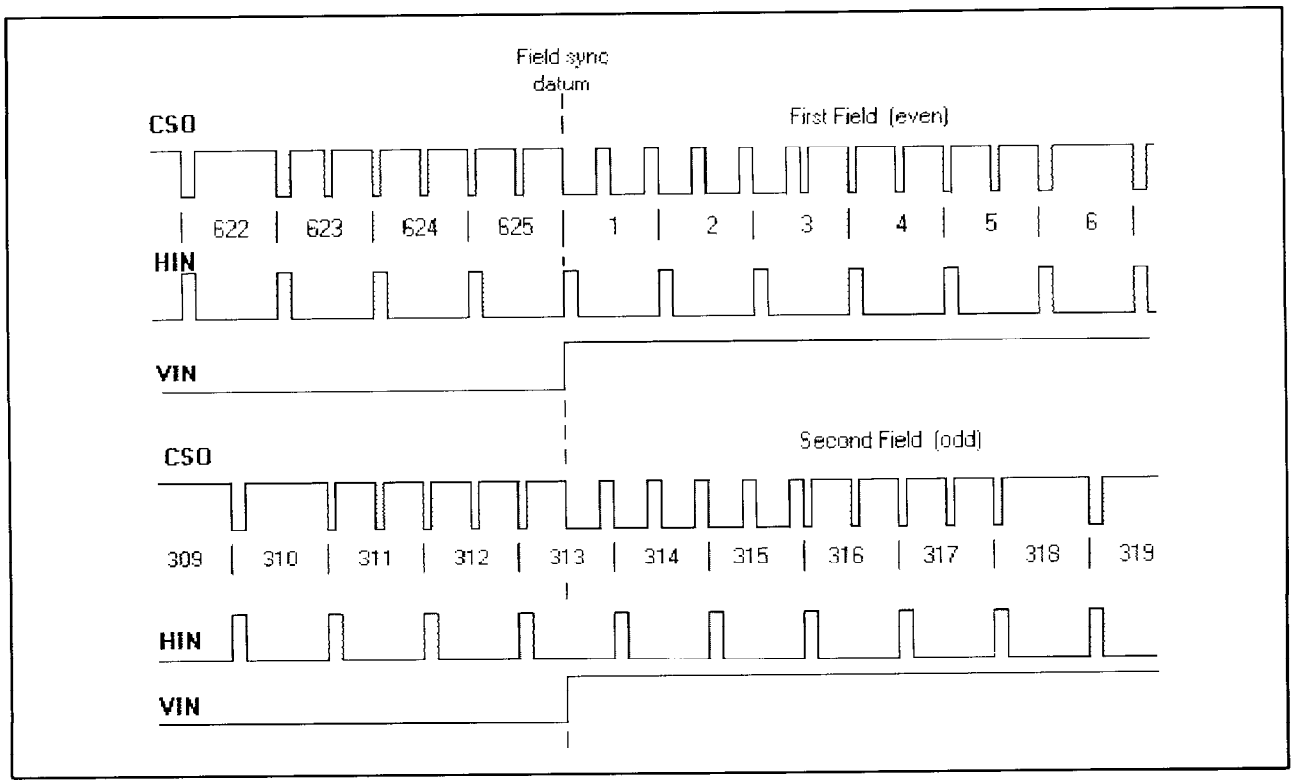

Fig. 7. Horizontal and Vertical input waveforms.

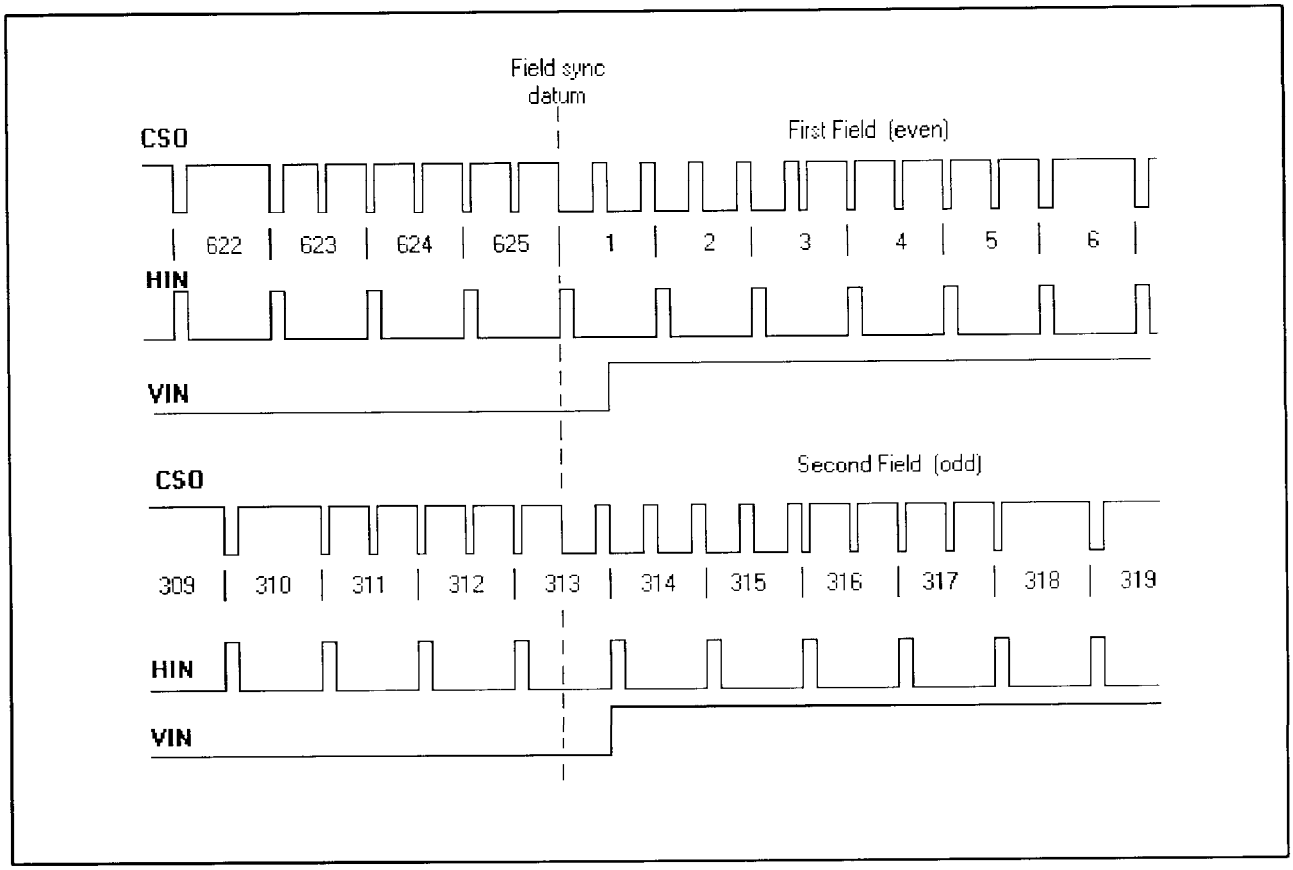

Fig. 8. Horizontal and Vertical input waveforms with Vertical Half Line Delay bit set.

Symbol	Parameters Description	Value for DRAM		Units
		Min	Max	
t_{RAC}	Access time from $\overline{RAS}$		<106	ns
t_{CAC}	Access time from $\overline{CAS}$		<43	ns
t_{CAA}	Access time from column address		<61	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge		<72	ns
t_{ASR}	Row address set–up time before $\overline{RAS}$	<27		ns
t_{RAH}	Row address hold time after $\overline{RAS}$	<45		ns
t_{RSH}	$\overline{RAS}$ hold time	<36		ns
t_{ASC}	Column address set–up time before $\overline{CAS}$	<18		ns
t_{CAH}	Column address hold time after $\overline{CAS}$	<54		ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	<72		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay	<63		ns
t_{RP}	$\overline{RAS}$ precharge time	<81		ns
t_{CP}	$\overline{CAS}$ precharge time	<27		ns
t_{CAS}	$\overline{CAS}$ low pulse width	<45		ns
t_{RAS}	$\overline{RAS}$ low pulse width	<171		ns
t_{DS}	Data set–up before $\overline{CAS}$	<18		ns
t_{DH}	Data hold time after $\overline{CAS}$	<54		ns
t_{WCS}	Write set–up before $\overline{CAS}$	<72		ns
t_{WCH}	Write hold time after $\overline{CAS}$	<72		ns
t_{PC}	Page mode cycle time	<72		ns
t_{REF} – 64Kx4	Refresh cycle time per $\overline{RAS}$ address		>1.033	ms
t_{REF} – 256Kx4	Refresh cycle time per $\overline{RAS}$ address		>2.066	ms
t_{REF} – 1Mx4	Refresh cycle time per $\overline{RAS}$ address		>4.133	ms

Table 7. Timing parameter required for DRAM.

NOTE: Timings are for nominal center points on edges, so care should be taken not to load the pins.

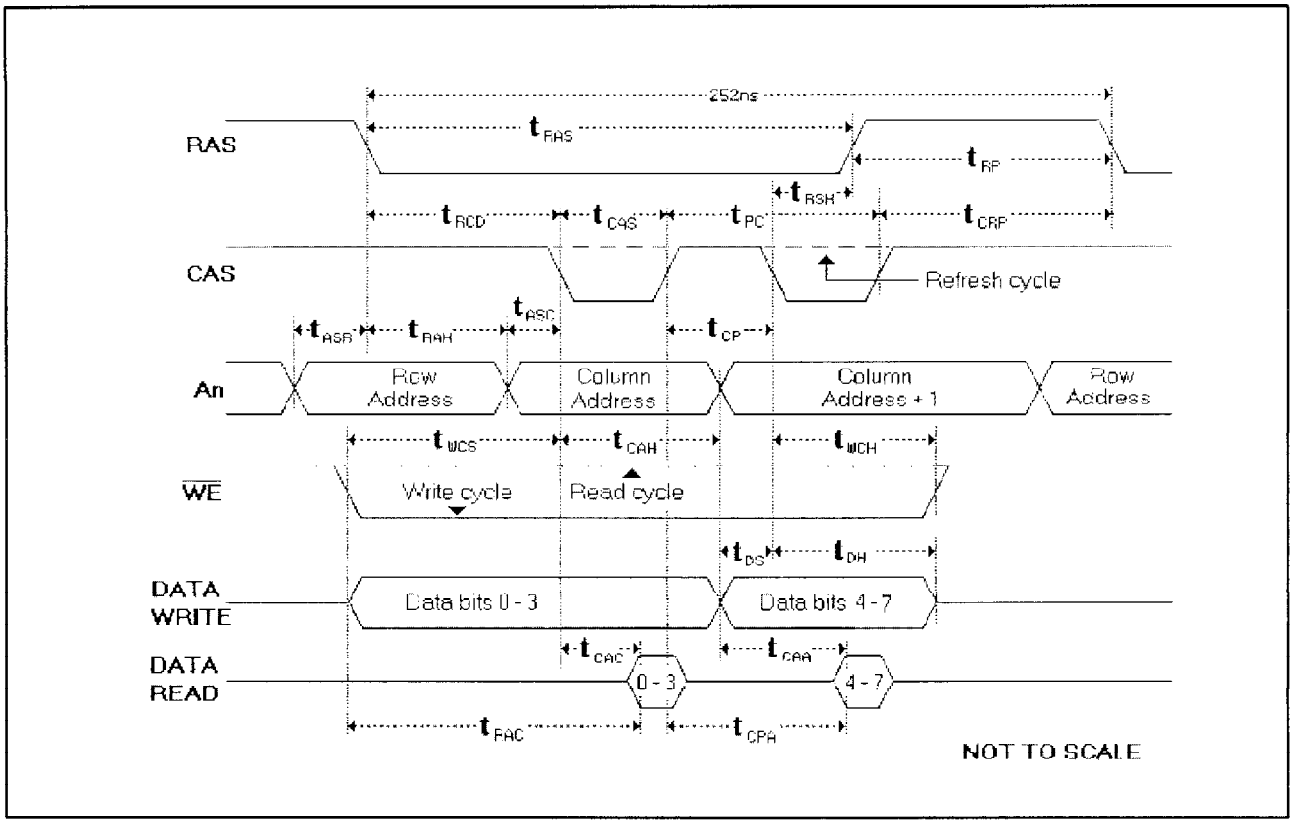

Fig. 9 DRAM interface.

DISPLAY STORE

The MV1817 has two modes of operation defined by the setting of DISC bit in TADD register.

1. With DISC set low, the display store is tied to acquisition circuit A, if DSB bit in DISCON1 register is low, or to acquisition circuit B if DSB bit is set high. STORA or STORB defines the working store for both acquisition and display.

2. With DISC set high, the display store is disconnected from the acquisition circuits and controlled independently by the DISPST register, together with DST8 in TADD register.

The store number programmed into STORA, STORB or DISPST registers is internally adjusted to take account of 2K/STORE working, see table 2. However, the I^2C bus addresses for the DRAM data are NOT internally adjusted in 2K/STORE mode, see again table 2.

DISPLAY POSITION

This may be adjusted by changing the value in the DPOS register. The lower 4 bits control the horizontal position. The default state is Bhex and the step size is four pixels (0.288 µs). Incrementing by one moves the display right by four pixels. This means the display can be moved 16 pixels (1.153 µs) right and 44 pixels (3.171 µs) left from the default position 15.28µs from leading negative edge of the Composite Sync Output horizontal sync pulse, see Fig. 10.

The upper 4 bits control the vertical position and the line numbers are referred to the Field Sync Datum on the Composite Sync Output, see Fig. 6. The default state is 7hex and the step size is 2 TV lines. Incrementing by one moves the display up two TV lines. The default start position is TV line 46 for a 24 row display and TV line 36 for a 25 or 26 row display. The range of movement is 16 TV lines up and 14 TV lines down from the default starting position, see Fig. 11.

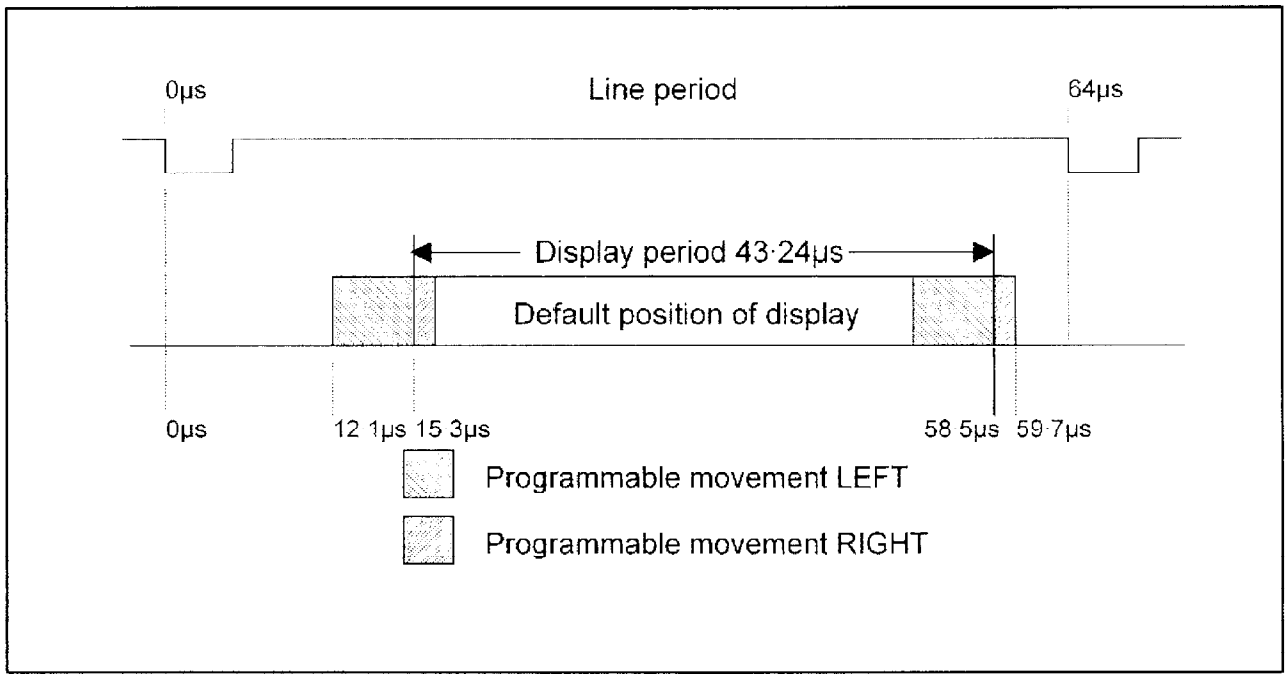

Fig. 10 Horizontal position and movement of text display.

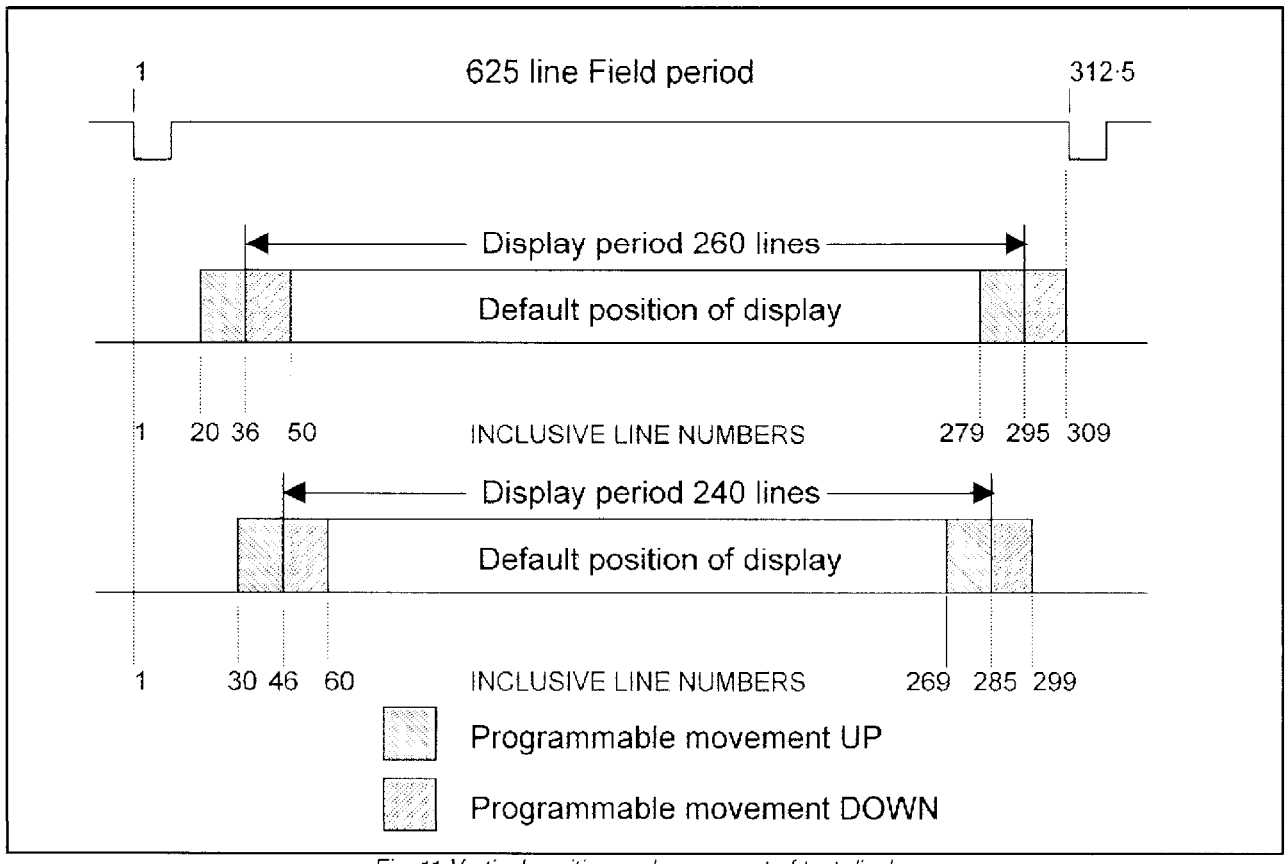

Fig. 11 Vertical position and movement of text display.

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