14-Bit, 20/40/65 MSPS Dual A/D Converter

Preliminary Technical Data

AD9248

FEATURES

Integrated Dual 14-Bit A-to-D Converters
Single 3 V Supply Operation (2.7 V to 3.6 V)
SNR = 73 dBc (to Nyquist, AD9248-65)
SFDR = 83 dBc (to Nyquist, AD9248-65)
Low Power: 600 mW at 65 MSPS
Differential Input with 500 MHz 3 dB Bandwidth
Exceptional Cross Talk Immunity > 85dB
Flexible Analog Input: 1 V p-p to 2 V p-p Range
Offset Binary or Twos Complement Data Format
Clock Duty Cycle Stabilizer

APPLICATIONS

Ultrasound Equipment
IF Sampling in Communications Receivers:
IS-95, CDMA One, IMT-2000
Battery-Powered Instruments
Hand-Held Scopemeters
Low Cost Digital Oscilloscopes

GENERAL DESCRIPTION

The AD9248 is a dual, 3 V, 14-bit, 20/40/65 MSPS analog-to-digital converter. It features dual high performance sample-and hold amplifiers and an integrated voltage reference. The AD9248 uses a multistage differential pipelined architecture with output error correction logic to provide 14-bit accuracy and guarantee no missing codes over the full operating temperature range at up to 65 MSPS data rates. The wide bandwidth, differential SHA allows for a variety of user selectable input ranges and offsets including single-ended applications. It is suitable for various applications including multiplexed systems that switch full-scale voltage levels in successive channels and for sampling inputs at frequencies well beyond the Nyquist rate.

Dual single-ended clock inputs are used to control all internal conversion cycles. A duty cycle stabilizer is available on the AD9248-65 and can compensate for wide variations in the clock duty cycle, allowing the converters to maintain excellent performance. The digital output data is presented in either straight binary or twos complement format. Out-of-range signals indicate an overflow condition, which can be used with the most significant bit to determine low or high overflow. Fabricated on an advanced CMOS process, the AD9248 is available in a space saving 64-lead LQFP and is specified over the industrial temperature range (–40? C to +85? C).

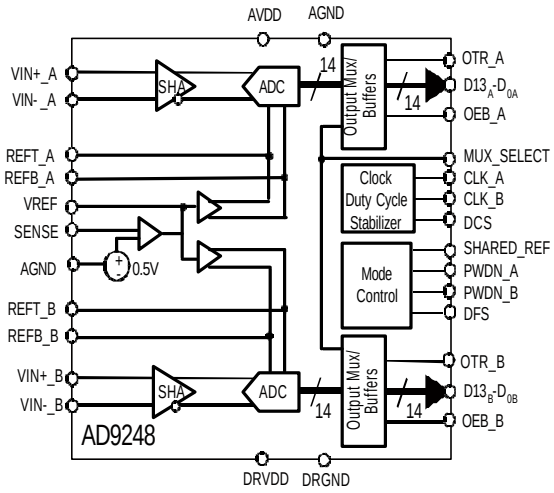

Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

1. Pin compatible with AD9238, 12-bit 20/40/65MSPS ADC.
2. Speed grade options of 20 MSPS, 40 MSPS, and 65 MSPS allow flexibility between power, cost, and performance to suit an application.
3. Low power consumption:

   AD9248-65: 65 MSPS = 600 mW.
   AD9248-40: 40 MSPS = 330 mW.
   AD9248-20: 20 MSPS = 180 mW.
4. The patented SHA input maintains excellent performance for input frequencies up to 100 MHz and can be configured for single-ended or differential operation.
5. Typical channel isolation of 85 dB @ f_{IN} = 10 MHz.
6. The clock duty cycle stabilizer (AD9248-65 only) maintains performance over a wide range of clock duty cycles.
7. The OTR output bits indicate when either input signal is beyond the selected input range.
8. Multiplexed data output option enables single-port operation from either data port A or data port B.

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REVISION HISTORY

PrA: Initial Version

PrB: Included Spec tables, pin out configuration and assignments

PrC: Updated Ordering guide to designate Pb Free part numbers

PrD: Corrected Ordering guide

PrE: Corrected package pin-out error (pins10,11,14,15), corrected product highlights typo (p1)

AD9248–SPECIFICATIONS

DC SPECIFICATIONS

Table 1. (AVDD = 3 V, DRVDD = 2.5 V, Maximum Sample Rate, CLK_A = CLK_B; AIN = -0.5 dBFS Differential Input, 1.0 V Internal Reference, TMIN to TMAX, unless otherwise noted.)

		Test	AD9248BST/BCP-20			AD9248BST/BCP-40			AD9248BST/BCP-65			
Parameter	**Temp**	**Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	VI	14			14			14			Bits
ACCURACY												
No Missing Codes Guaranteed	Full	VI	14			14			14			Bits
Offset Error	Full	VI		±0.5			±0.5			±0.5		% FSR
Gain Error[1]	Full	IV		±0.7			±0.7			±0.7		% FSR
Differential Nonlinearity (DNL)[2]	Full	V		±0.5			±0.5			±0.5		LSB
	25°C	I		±0.5			±0.5			±0.5		LSB
Integral Nonlinearity (INL)[2]	Full	V		±1.4			±1.4			±1.4		LSB
	25°C	I		±1.4	±1.4		±1.4			±1.4		LSB
TEMPERATURE DRIFT												
Offset Error	Full	V		±10			±10			±10		ppm/°C
Gain Error[1]	Full	V		±12			±12			±12		ppm/°C
INTERNAL VOLTAGE REFERENCE												
Output Voltage Error (1 V Mode)	Full	VI		±5	±35		±5	±35		±5	±35	mV
Load Regulation @ 1.0 mA	Full	V		0.8			0.8			0.8		mV
Output Voltage Error (0.5 V Mode)	Full	V		±2.5			±2.5			±2.5		mV
Load Regulation @ 0.5 mA	Full	V		0.1			0.1			0.1		mV
INPUT REFERRED NOISE												
Input Span = 1 V	25°C	V		1.8			1.8			1.8		LSB rms
Input Span = 2.0 V	25°C	V		1.2			1.2			1.2		LSB rms
ANALOG INPUT												
Input Span = 1.0 V	Full	IV		1			1			1		V p-p
Input Span = 2.0 V	Full	IV		2			2			2		V p-p
Input Capacitance[3]	Full	V		7			7			7		pF
REFERENCE INPUT RESISTANCE	Full	V		7			7			7		k?
POWER SUPPLIES												
Supply Voltages												
AVDD	Full	IV	2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	Full	IV	2.25	3.0	3.6	2.25	3.0	3.6	2.25	3.0	3.6	V
Supply Current												
IAVDD[2]	Full	V		60			110			200		mA
IDRVDD[2]	Full	V		4			10			14		mA
PSRR	Full	V		±0.01			±0.01			±0.01		% FSR
POWER CONSUMPTION												
DC Input[4]	Full	V		180			330			600		mW
Sine Wave Input[2]	Full	VI		190	212		360	397		640	698	mW
Standby Power[5]	Full	V		2.0			2.0			2.0		mW
MATCHING												

CHARACTERISTICS						
Offset Error	Full	V	±0.1	±0.1	±0.1	% FSR
Gain Error	Full	V	±0.05	±0.05	±0.05	% FSR

[1] Gain error and gain temperature coefficient are based on the A/D converter only (with a fixed 1.0 V external reference).
[2] Measured at maximum clock rate with a low frequency sine wave input and approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AVSS. Refer to Figure for the equivalent analog input structure.
[4] Measured with dc input at maximum clock rate.
[5] Standby power is measured with the CLK_A and CLK_B pins inactive (i.e., set to AVDD or AGND).
Specifications subject to change without notice.

DC SPECIFICATIONS (CONTINUED)

Table 2. (AVDD = 3 V, DRVDD = 2.5 V, Maximum Sample Rate, CLK_A = CLK_B; AIN = -0.5 dBFS Differential Input, 1.0 V Internal Reference, TMIN to TMAX, unless otherwise noted.)

		Test	AD9248BST/BCP-20			AD9248BST/BCP-40			AD9248BST/BCP-65			Unit
Parameter	**Temp**	**Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	
LOGIC INPUTS												
High Level Input Voltage	Full	IV	2.0			2.0			2.0			V
Low Level Input Voltage	Full	IV			0.8			0.8			0.8	V
High Level Input Current	Full	IV	- 10		+10	- 10		+10	- 10		+10	µA
Low Level Input Current	Full	IV	- 10		+10	- 10		+10	- 10		+10	µA
Input Capacitance	Full	IV		2			2			2		pF
LOGIC OUTPUTS[1]												
DRVDD = 3.3V												
High Level Output Voltage (IOH = 50 mA)	Full	IV	3.29			3.29			3.29			V
High Level Output Voltage (IOH = 0.5 mA)	Full	IV	3.25			3.25			3.25			V
Low Level Output Voltage (IOL = 50 mA)	Full	IV			0.05			0.05			0.05	V
Low Level Output Voltage (IOL = 1.6 mA)	Full	IV			0.2			0.2			0.2	V
DRVDD = 2.5V												
High Level Output Voltage (IOH = 50 mA)	Full	IV	2.49			2.49			2.49			V
High Level Output Voltage (IOH = 0.5 mA)	Full	IV	2.45			2.45			2.45			V
Low Level Output Voltage (IOL = 50 mA)	Full	IV			0.05			0.05			0.05	V
Low Level Output Voltage (IOL = 1.6 mA)	Full	IV			0.2			0.2			0.2	V

[1] Output Voltage Levels measured with 5 pF load on each output.
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

Table 3. Switching Specifications

Parameter	Temp	Test Level	AD9248BST/BCP-20 Min	AD9248BST/BCP-20 Typ	AD9248BST/BCP-20 Max	AD9248BST/BCP-40 Min	AD9248BST/BCP-40 Typ	AD9248BST/BCP-40 Max	AD9248BST/BCP-65 Min	AD9248BST/BCP-65 Typ	AD9248BST/BCP-65 Max	Unit
SWITCHING PERFORMANCE												
Max Conversion Rate	Full	VI	20			40			65			MSPS
Min Conversion Rate	Full	V			1			1			1	MSPS
CLK Period	Full	V	50.0			25.0			15.4			ns
CLK Pulsewidth High[1]	Full	V	15.0			8.8			6.2			ns
CLK Pulsewidth Low[1]	Full	V	15.0			8.8			6.2			ns
DATA OUTPUT PARAMETER												
Output Delay[2] (t_{PD})	Full	VI	2	3.5	6	2	3.5	6	2	3.5	6	ns
Pipeline Delay (Latency)	Full	V		7			7			7		Cycles
Aperture Delay (t_A)	Full	V		1.0			1.0			1.0		ns
Aperture Uncertainty (t_J)	Full	V		0.5			0.5			0.5		Ps rms
Wake-Up Time[3]	Full	V		2.5			2.5			2.5		ms
OUT-OF-RANGE RECOVERY TIME	Full	V		2			2			2		

[1] The AD9248-65 model has a duty cycle stabilizer circuit that, when enabled, corrects for a wide range of duty cycles (see TPC 20).
[2] Output delay is measured from CLOCK 50% transition to DATA 50% transition, with a 5 pF load on each output.
[3] Wake-up time is dependent on the value of the decoupling capacitors; typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.
Specifications subject to change without notice.

AC SPECIFICATIONS

Table 4. (AVDD = 3 V, DRVDD = 2.5 V, Maximum Sample Rate, CLK_A = CLK_B; AIN = –0.5 dBFS Differential Input, 1.0 V Internal Reference, TMIN to TMAX, unless otherwise noted.)

		Test	AD9248BST/BCP-20			AD9248BST/BCP-40			AD9248BST/BCP-65			
Parameter	**Temp**	**Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO												
f_{INPUT} = 2.4 MHz	25°C	V		73			73			73		dBc
f_{INPUT} = 9.7 MHz	Full	V		73								dBc
	25°C	IV	tbd	73								dBc
f_{INPUT} = 19.6 MHz	Full	V					72					dBc
	25°C	IV				tbd	72					dBc
f_{INPUT} = 32.5 MHz	Full	V								72		dBc
	25°C	IV							tbd	72		dBc
f_{INPUT} = 100 MHz	25°C	V		70			70			70		dBc
SIGNAL-TO-NOISE AND DISTORTION RATIO												
f_{INPUT} = 2.4 MHz	25°C	V		72.8			72.8			72.6		dBc
f_{INPUT} = 9.7 MHz	Full	V		72								dBc
	25°C	IV	tbd	72								dBc
f_{INPUT} = 19.6 MHz	Full	V					71.9					dBc
	25°C	IV				tbd	71.6					dBc
f_{INPUT} = 32.5 MHz	Full	V								71.5		dBc
	25°C	IV							tbd	71		dBc
f_{INPUT} = 100 MHz	25°C	V		69.6			69.5			69.4		dBc
EFFECTIVE NUMBER OF BITS (ENOB)												
f_{INPUT} = 2.4 MHz	25°C	V		11.8			11.8			11.8		Bits
f_{INPUT} = 9.7 MHz	Full	V		11.7								Bits
	25°C	IV	tbd	11.7								Bits
f_{INPUT} = 19.6 MHz	Full	V					11.7					Bits
	25°C	IV				tbd	11.7					Bits
f_{INPUT} = 32.5 MHz	Full	V								11.6		Bits
	25°C	IV							tbd	11.5		Bits
f_{INPUT} = 100 MHz	25°C	V		11.4			11.4			11.3		Bits
TOTAL HARMONIC DISTORTION												
f_{INPUT} = 2.4 MHz	25°C	V		- 83.0			- 83.0			- 83.0		dBc
f_{INPUT} = 9.7 MHz	Full	V		- 81.0								dBc
	25°C	I		- 83.0	tbd							dBc
f_{INPUT} = 19.6 MHz	Full	V					- 81.0					dBc
	25°C	I					- 83.0	tbd				dBc
f_{INPUT} = 32.5 MHz	Full	V								- 78.0		dBc
	25°C	I								- 80.0	tbd	dBc
f_{INPUT} = 100 MHz	25°C	V		- 77.0			- 79.0			- 74.0		dBc
WORST HARMONIC (2nd or 3rd)												
f_{INPUT} = 9.7 MHz	Full	V		- 84.0								dBc
f_{INPUT} = 19.6 MHz	Full	V					- 85.0					dBc
f_{INPUT} = 32.5 MHz	Full	V								- 80.0		dBc
SPURIOUS FREE DYNAMIC RANGE												

f_{INPUT} = 2.4 MHz	25°C	V		86.0		86.0		86.0		dBc
f_{INPUT} = 9.7 MHz	Full	V		84.0						dBc
	25°C	I	tbd	86.0						dBc
f_{INPUT} = 19.6 MHz	Full	V				85.0				dBc
	25°C	I			tbd	86.0				dBc
f_{INPUT} = 32.5 MHz	Full	V						83.0		dBc
	25°C	I					tbd	83.0		dBc
f_{INPUT} = 100 MHz	25°C	V						75.0		dBc
CROSSTALK	Full	V		- 85.0		- 85.0		- 85.0		dB

Specifications subject to change without notice.

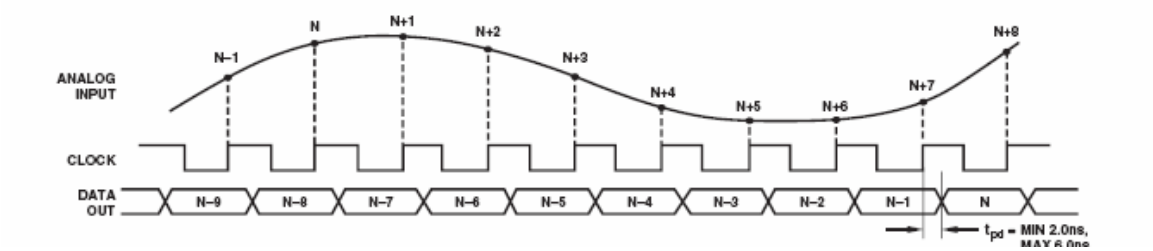


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5. AD9248 Absolute Maximum Ratings[1]

Parameter		Rating		
Pin Name	**With Respect To**	**Min**	**Max**	**Unit**
ELECTRICAL				
AVDD	AGND	- 0.3	+3.9	V
DRVDD	DRGND	- 0.3	+3.9	V
AGND	DRGND	- 0.3	+0.3	V
AVDD	DRVDD	- 3.9	+3.9	V
Digital Outputs CLK, DCS, MUX_SELECT, SHARED_REF,	DRGND	- 0.3	DRVDD + 0.3	V
OEB, DFS	AGND	- 0.3	AVDD + 0.3	V
VINA, VINB	AGND	- 0.3	AVDD + 0.3	V
VREF	AGND	- 0.3	AVDD + 0.3	V
SENSE	AGND	- 0.3	AVDD + 0.3	V
REFB, REFT	AGND	- 0.3	AVDD + 0.3	V
PDWN	AGND	- 0.3	AVDD + 0.3	V
ENVIRONMENTAL[2]				
Operating Temperature		- 45	+85	℃
Junction Temperature			+150	℃
Lead Temperature (10 sec)			+300	℃
Storage Temperature		- 65	+150	℃

[1] Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2] Typical thermal impedances (64-lead LQFP); ? ?$_{JA}$ = 54°C/W. These measurements were taken on a 4 -layer board in still air, in accordance with EIA/JESD51-7.

EXPLANATION OF TEST LEVELS

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

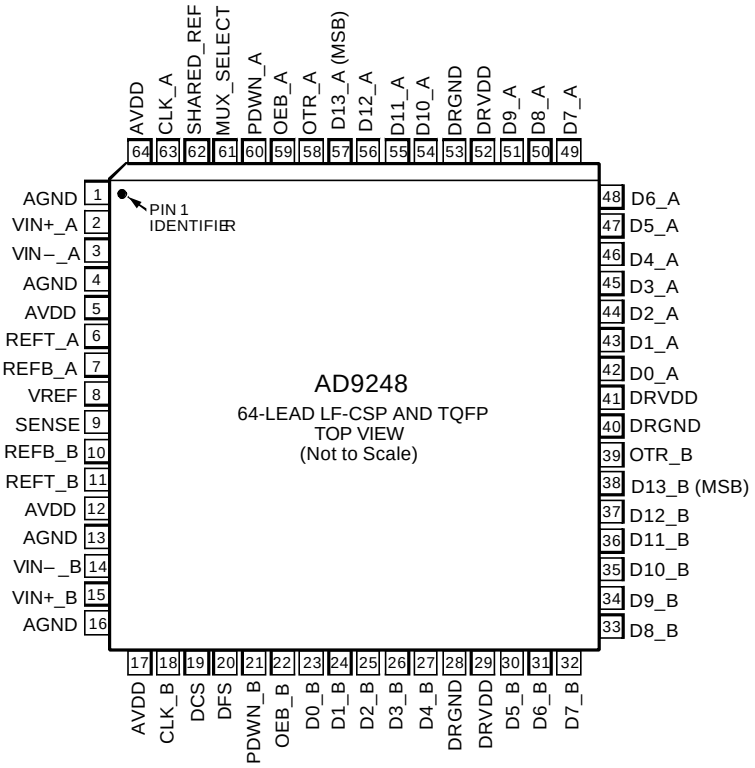


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
2	VIN+_A	Analog Input Pin (+) for Channel A
3	VIN–_A	Analog Input Pin (-) for Channel A
15	VIN+_B	Analog Input Pin (+) for Channel B
14	VIN- _B	Analog Input Pin (-) for Channel B
6	REFT_A	Differential Reference (+) for Channel A
7	REFB_A	Differential Reference (-) for Channel A
11	REFT_B	Differential Reference (+) for Channel B
10	REFB_B	Differential Reference (-) for Channel B
8	VREF	Voltage Reference Input/Output
9	SENSE	Reference Mode Selection
18	CLK_B	Clock Input Pin for Channel B
63	CLK_A	Clock Input Pin for Channel A
19	DCS	Enable Duty Cycle Stabilizer (DCS) Mode
20	DFS	Data Output Format Select Bit (Low for Offset Binary, High for Twos Complement)
21	PDWN_B	Power-Down Function Selection for Channel B (Active High)
60	PDWN_A	Power-Down Function Selection for Channel A (Active High)
22	OEB_B	Output Enable Bit for Channel B
59	OEB_A	Output Enable Bit for Channel A (Low Setting Enables Channel A Output Data Bus)
42–51, 54-57	D0_A (LSB)-D13_A (MSB)	Channel A Data Output Bits
23–27, 30-38	D0_B (LSB) -D13_B (MSB)	Channel B Data Output Bits
39	OTR_B	Out-of-Range Indicator for Channel B
58	OTR_A	Out-of-Range Indicator for Channel A
62	SHARED_REF	Shared Reference Control Bit (Low for Independent Reference Mode, High for Shared Reference Mode)

61	MUX_SELECT	Data Multiplexed Mode. (See description for how to enable; high setting disables output data Multiplexed mode)
5, 12, 17, 64	AVDD	Analog Power Supply
1, 4, 13, 16	AGND	Analog Ground
28, 40, 53	DRGND	Digital Output Ground
29, 41, 52	DRVDD	Digital Output Driver Supply. Must be decoupled to DRGND with a minimum 0.1 µF capacitor. Recommended decoupling is 0.1 µF capacitor in parallel with 10 µF

Table 7. ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9248BCPZ-20	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP)	CP-64-1
AD9248BCPZ-40	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP)	CP-64-1
AD9248BCPZ-65	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP)	CP-64-1
AD9248BCPZRL7-20	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP)	CP-64-1
AD9248BCPZRL7-40	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP)	CP-64-1
AD9248BCPZRL7-65	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP)	CP-64-1
AD9248BST-20	–40°C to +85°C	64-Lead LOW PROFILE QUAD FLAT PACK (TQFP)	ST-64
AD9248BST-40	–40°C to +85°C	64-Lead LOW PROFILE QUAD FLAT PACK (TQFP)	ST-64
AD9248BST-65	–40°C to +85°C	64-Lead LOW PROFILE QUAD FLAT PACK (TQFP)	ST-64
AD9248-20PCB	+25°C	Evaluation Board with AD9248BST-20	
AD9248-40PCB	+25°C	Evaluation Board with AD9248BST-40	
AD9248-65PCB	+25°C	Evaluation Board with AD9248BST-65	

TERMINOLGY

Aperture Delay

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

Aperture Jitter

The variation in aperture delay for successive samples, which is manifested as noise on the input to the A/D converter.

Integral Nonlinearity (INL)

INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 8192 codes must be present over all operating ranges.

Offset Error

The major carry transition should occur for an analog value 1/2 LSB below VIN+ = VIN- . Offset error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift

The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Total Harmonic Distortion (THD)

The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal, expressed as a percentage or in decibels relative to the peak carrier signal (dBc).

Signal-to-Noise and Distortion (S/N+D, SINAD) Ratio

The ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels relative to the peak carrier signal (dBc).

Effective Number of Bits (ENOB)

Using the following formula:

$$ENOB = (SINAD - 1.76)/6.02$$

effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured *SINAD*.

Signal-to-Noise Ratio (SNR)

The ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels relative to the peak carrier signal (dBc).

Spurious Free Dynamic Range (SFDR)

The difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Nyquist Sampling

When the frequency components of the analog input are below the Nyquist frequency ($f_{CLOCK}/2$), this is often referred to as Nyquist sampling.

IF Sampling

Due to the effects of aliasing, an ADC is not necessarily limited to Nyquist sampling. Higher sampled frequencies will be aliased down into the first Nyquist zone (DC - $f_{CLOCK}/2$) on the output of the ADC. Care must be taken that the bandwidth of the sampled signal does not overlap Nyquist zones and alias onto itself. Nyquist sampling performance is limited by the bandwidth of the input SHA and clock jitter (jitter adds more noise at higher input frequencies).

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Out-of-Range Recovery Time

Out-of-range recovery time is the time it takes for the A/D converter to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Crosstalk

Coupling onto one channel being driven by a (- 0.5 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal. Measurement includes all spurs resulting from both direct coupling and mixing components.

TYPICAL PERFORMANCE CHARACTERISTIC

EQUIVALENT CIRCUITS

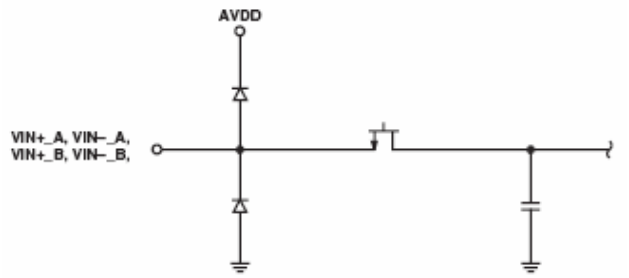


Figure 2. Equivalent Analog Input Circuit

Figure xx. Equivalent Analog Input Circuit

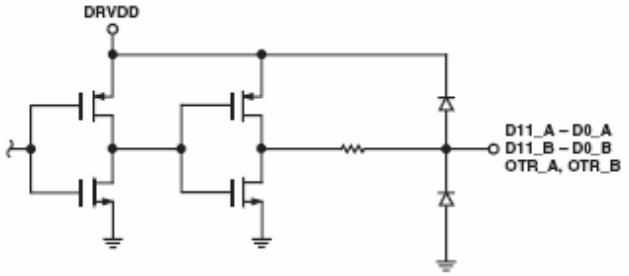


Figure 3. Equivalent Digital Output Circuit

Figure xx. Equivalent Digital Output Circuit

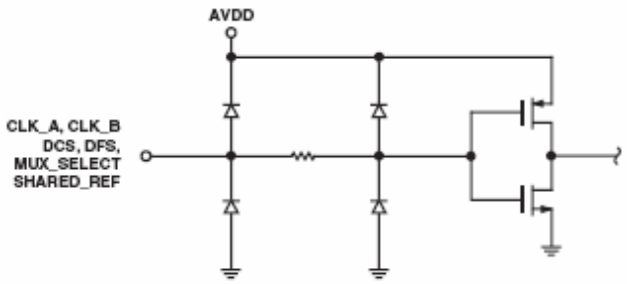


Figure 4. Equivalent Digital Input Circuit

Figure xx. Equivalent Digital Input Circuit

THEORY OF OPERATION

The AD9248 consists of two high performance analog-to-digital converters (ADCs) that are based on the AD9235 converter core. The dual ADC paths are independent, except for a shared internal band gap reference source, VREF. Each of the ADC's paths consists of a proprietary front end sample-and-hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The pipelined ADC is divided into three sections, consisting of a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit fl ash. Each stage provides sufficient overlap to correct for fl ash errors in the preceding stages. The quantized outputs from each stage are comb ined through the digital correction logic block into a final 12-bit result. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the respective clock.

Each stage of the pipeline, excluding the last, consists of a low resolution fl ash ADC and a residual multiplier to drive the next stage of the pipeline. The residual multiplier uses the fl ash ADC output to control a switched capacitor digital-to-analog converter (DAC) of the same resolution. The DAC output is subtracted from the stage's input signal and the residual is amplified (multiplied) to drive the next pipeline stage. The residual multiplier stage is also called a multiplying DAC (MDAC). One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be configured as ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing.

ANALOG INPUT

The analog input to the AD9248 is a differential switched capacitor, SHA, that has been designed for optimum performance while processing a differential input signal. The SHA input accepts inputs over a wide common-mode range. An input common-mode voltage of mid supply is recommended to maintain optimal performance.

The SHA input is a differential switched capacitor circuit. In Figure , the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network will create a low-pass filter at the ADC's

input; therefore, the precise values are dependant on the application. In IF under sampling applications, any shunt capacitors should be removed. In combination with the driving source impedance, they would limit the input bandwidth. For best dynamic performance, the source impedances driving VIN+ and VIN- should be matched such that common-mode settling errors are symmetrical. These errors will be reduced by the common-mode rejection of the ADC.

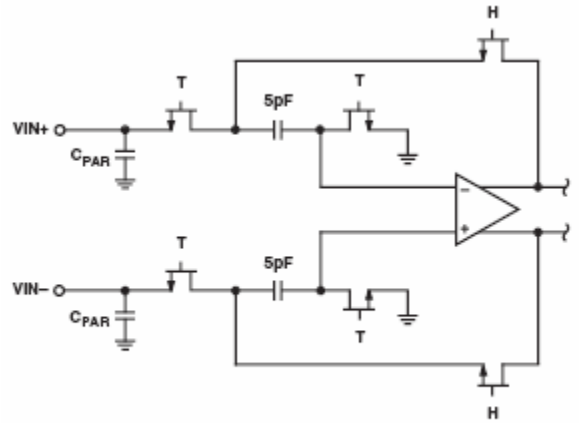


Figure 5. Switched Capacitor Input

Figure xx. Switched Capacitor Input

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common-mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as follows:

$$REFT = 1/2\left(AVDD + V_{REF}\right)$$

$$REFB = 1/2\left(AVDD + V_{REF}\right)$$

$$Span = 2\times\left(REFT - REFB\right) = 2\times V_{REF}$$

It can be seen from the equations above that the REFT and REFB voltages are symmetrical about the mid-supply voltage and, by definition, the input span is twice the value of the V_{REF} voltage.

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V, or adjusted within the same range as discussed in the Internal Reference Connection section. Maximum SNR performance will be achieved with the AD9248 set to the largest input span of 2 V_{P-P}. The relative SNR degradation will be 3 dB when changing from 2 V_{P-P} mode to 1 V_{P-P} mode.

The SHA may be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as follows:

$$VCM_{MIN} = V_{REF}/2$$

$$VCM_{MAX} = \left(AVDD + V_{REF}\right)/2$$

The minimum common-mode input level allows the AD9248 to accommodate ground-referenced inputs. Although optimum performance is achieved with a differential input, a single-ended source may be driven into VIN+ or VIN- . In this configuration, one input will accept the signal, while the opposite input should be set to midscale by connecting it to an appropriate reference. For example, a 2 V_{P-P} signal may be applied to VIN+ while a 1 V reference is applied to VIN- . The AD9248 will then accept an input signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance may degrade significantly as compared to the differential case. However, the effect will be less noticeable at lower input frequencies and in the lower speed grade models (AD9248-40 and AD9248-20).

Differential Input Configurations

As previously detailed, optimum performance will be achieved while driving the AD9248 in a differential input configuration. For base band applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers will not be adequate to achieve the true performance of the AD9248. This is especially true in IF under sampling applications where frequencies in the 70 MHz to 200 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration, as shown in Figure .

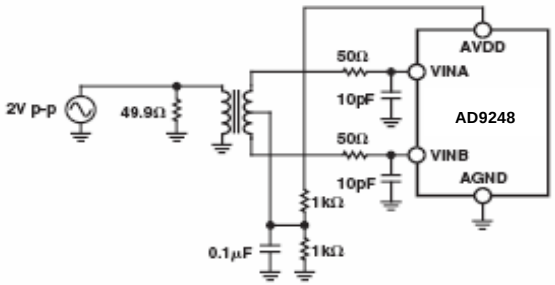


Figure 6. Differential Transformer Coupling

Figure xx. Differential Transformer Coupling

The signal characteristics must be considered when selecting a transformer. Most RF transformers will saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, there will be a

degradation in SFDR and in distortion performance due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance.

CLOCK INPUT AND CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9248 provides separate clock inputs for each channel. The optimum performance is achieved with the clocks operated at the same frequency and phase. Clocking the channels asynchronously may degrade performance significantly. In some applications, it is desirable to skew the clock timing of adjacent channels. The AD9248's separate clock inputs allow for clock timing skew (typically ±1 ns) between the channels without significant performance degradation.

The AD9248-65 contains two clock duty cycle stabilizers, one for each converter, that retime the nonsampling edge, providing an internal clock with a nominal 50% duty cycle (DCS is not available on the - 40 MSPS or - 20 MSPS versions). Input clock rates of over 40 MHz can use the DCS so that a wide range of input clock duty cycles can be accommodated. Maintaining a 50% duty cycle clock is particularly important in high speed applications, when proper track-and-hold times for the converter are required to maintain high performance. The DCS can be enabled by tying the DCS pin high.

The duty cycle stabilizer utilizes a delay locked loop to create the nonsampling edge. As a result, any changes to the sampling frequency will require approximately 2 µs to 3 µs to allow the DLL to acquire and settle to the new rate.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_J) can be calculated

with the following equation:

$$SNR\,\text{degradation} = 20 \times \log 10\left[1/2 \times p \times f_{INPUT} \times t_J\right]$$

In the equation, the rms aperture jitter, t_J , represents the root-sum square of all jitter sources, which includes the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

For optimal performance, especially in cases where aperture jitter may affect the dynamic range of the AD9248, it is important to minimize input clock jitter. The clock input circuitry should use stable references, for example using analog power and ground planes to generate the valid high and low digital levels for the AD9248 clock input. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

POWER DISSIPATION AND STANDBY MODE

The power dissipated by the AD9248 is proportional to its sampling rates. The digital (DRVDD) power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The digital drive current can be calculated by

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLOCK} \times N$$

where N is the number of bits changing and C_{LOAD} is the average load on the digital pins that changed.

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increases with clock frequency.

Either channel of the AD9248 can be placed into standby mode independently by asserting the PWDN_A or PDWN_B pins.

It is recommended that the input clock(s) and analog input(s) remain static during either independent or total standby, which will result in a typical power consumption of 1 mW for the ADC. Note that if DCS is enabled, it is mandatory to disable the clock of an independently powered-down channel. Otherwise, significant distortion will result on the active channel. If the clock inputs remain active while in total standby mode, typical power dissipation of 12 mW will result.

The minimum standby power is achieved when both channels are placed into full power-down mode (PDWN_A = PDWN_B = HI). Under this condition, the internal references are powered down. When either or both of the channel paths are enabled after a power-down, the wake-up time will be directly related to the recharging of the REFT and REFB decoupling capacitors and to the duration of the power-down. Typically, it takes approximately 5 ms to restore full operation with fully discharged 0.1 µF and 10 µF decoupling capacitors on REFT and REFB.

A single channel can be powered down for moderate power savings. The powered-down channel shuts down internal circuits, but both the reference buffers and shared reference remain powered. Because the buffer and voltage reference remain powered, the wake-up time is reduced to several clock cycles.

DIGITAL OUTPUTS

The AD9248 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

The data format can be selected for either offset binary or twos complement. This is discussed later in the Data Format section.

TIMING

The AD9248 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Refer to Figure 2 for a detailed timing diagram.

The internal duty cycle stabilizer can be enabled on the AD9248-65 using the DCS pin. This provides a stable 50% duty cycle to internal circuits.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9248. These transients can detract from the converter's dynamic performance. The lowest typical conversion rate of the AD9248 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance may degrade.

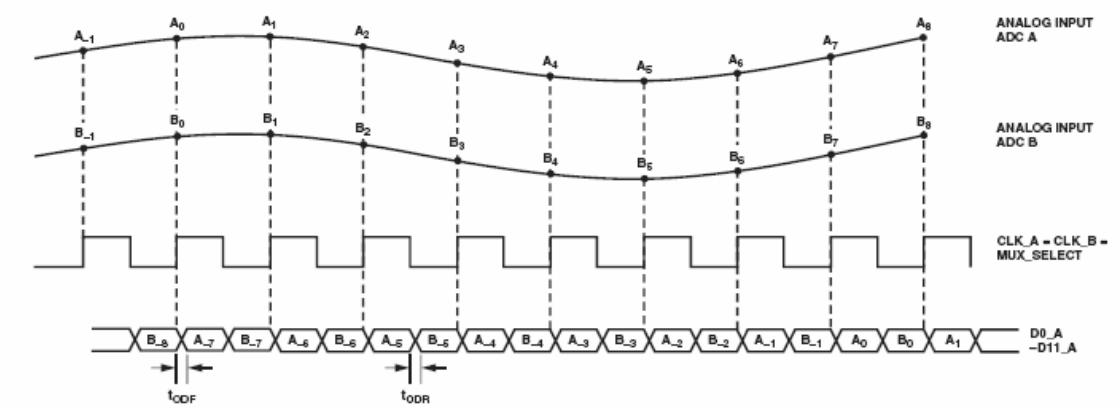


Figure 7. Example of Multiplexed Data Format Using the Channel A Output and the Same ClockTied to CLK_A, CLK_B, and MUX_SELECT

Figure xx. Example of Multiplexed Data Format Using the Channel A Output and the Same Clock Tied to CLK_A, CLK_B, and MUX_SELECT

DATA FORMAT

The AD9248 data output format can be configured for either twos complement or offset binary. This is controlled by the Data Format Select pin (DFS). Connecting DFS to AGND will produce offset binary output data. Conversely, connecting DFS to AVDD will format the output data as twos complement.

The output data from the dual A/D converters can be multiplexed onto a single 12-bit output bus. The multiplexing is accomplished by toggling the MUX_SELECT bit, which directs channel data to the same or opposite channel data port. When MUX_SELECT is logic high, the Channel A data is directed to Channel A output bus, and Channel B data is directed to the Channel B output bus. When MUX_SELECT is logic low, the channel data is reversed, i.e., Channel A data is directed to the Channel B output bus and Channel B data is directed to the Channel A output bus. By toggling the MUX_SELECT bit, multiplexed data is available on either of the output data ports.

If the ADCs are run with synchronized timing, this same clock can be applied to the MUX_SELECT bit. After the MUX_SELECT rising edge, either data port will have the data for its respective channel; after the falling edge, the alternate channel's data will be placed on the bus. Typically, the other unused bus would be disabled by setting the appropriate OEB high to reduce power consumption and noise. Figure xx shows an example of multiplex mode. When multiplexing data, the data rate is two times the sample rate. Note that both channels must remain active in this mode and that each channel's power-down pin must remain low.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9248. The input range can be adjusted by varying the reference voltage applied to the AD9248, using either the internal reference with different external resistor configurations or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly.

If the ADC is being driven differentially through a transformer, the reference voltage can be used to bias the center tap (common mode voltage).

The Shared Reference mode allows the user to connect the references from the dual ADCs together externally for superior gain and offset matching performance. If the ADCs are to function independently, the reference decoupling can be treated independently and can provide superior isolation between the dual channels. To enable Shared Reference mode, the SHARED_REF pin must be tied high and external differential references must be externally shorted. (REFT_A must be externally shorted to REFT_B and REFB_A must be shorted to REFB_B.)

Internal Reference Connection

A comparator within the AD9248 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table 8. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 4), setting V_{REF} to 1 V. Connecting the SENSE pin to V_{REF} switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected as shown in Figure , the switch will again be set to the SENSE pin. This will put the reference amplifier in a noninverting mode with the V_{REF} output defined as follows:

$$V_{REF} = 0.5 \times (1 + R2/R1)$$

In all reference configurations, REFT and REFB drive the ADC core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

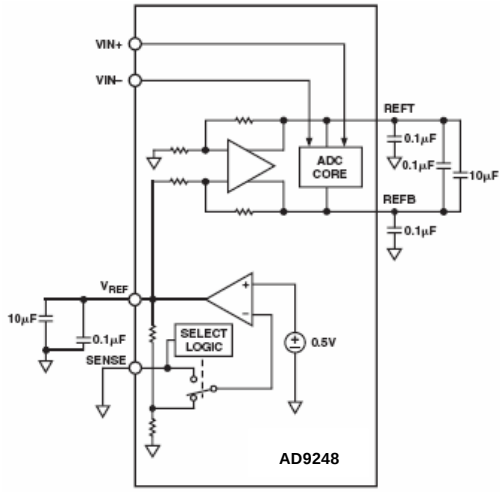


Figure 8. Internal Reference Configuration

Figure 4. Internal Reference Configuration

Table 8. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting V_{REF} (V)	Resulting Differential Span (V_{P-P})
External Reference	AVDD	N/A	2 × External Reference
Internal Fixed Reference	V_{REF}	0.5	1.0
Programmable Reference	0.2 V to V_{REF}	0.5 × (1 + R2/R1)	2 × V_{REF} (See Figure)
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) may be necessary to reduce gain matching errors to an acceptable level. A high precision external reference may also be selected to provide lower gain and offset temperature drift. Figure 10 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes. When the SENSE pin is tied to AVDD, the internal reference will be disabled, allowing the use of an external reference. An internal reference buffer will load the external reference with an equivalent 7 k? load. The internal buffer will still generate the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span will always be twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V. If the internal reference of the AD9248 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure depicts how the internal reference voltage is affected by loading.

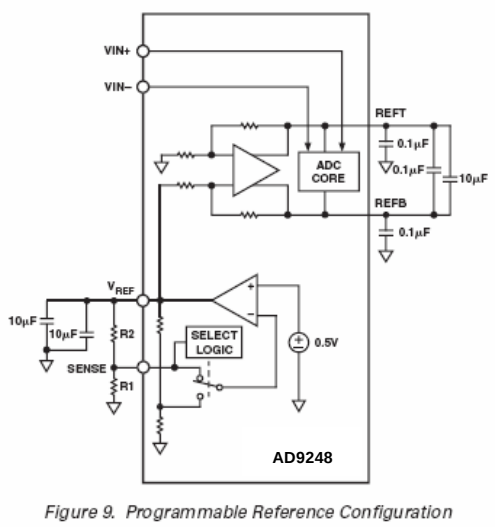


Figure 9. Programmable Reference Configuration

Figure xx. Programmable Reference Configuration

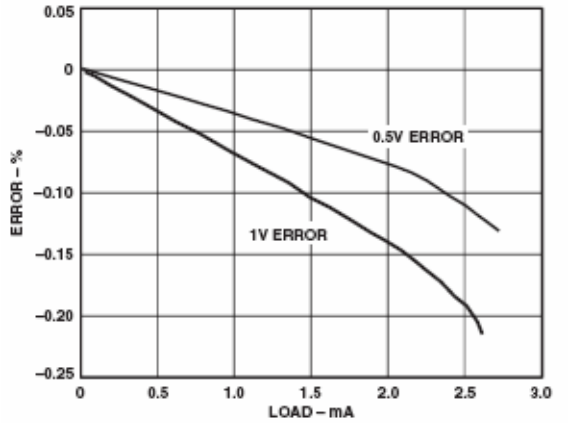


Figure 11. V_{REF} Accuracy vs. Load

Figure xx. V_{REF} Accuracy vs. Load

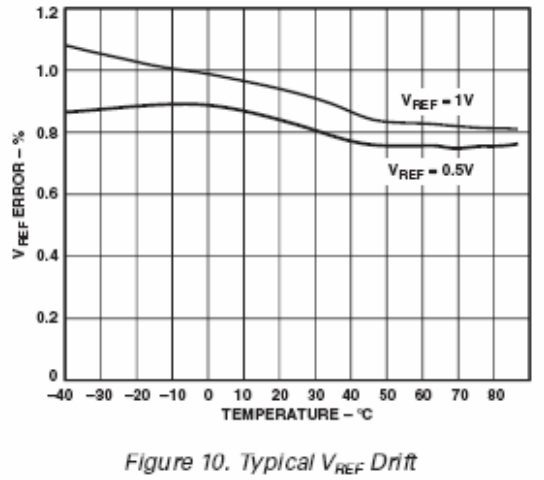


Figure 10. Typical V_{REF} Drift

Figure xx. Typical V_{REF} Drift

EVALUATION BOARD DIAGRAMS

OUTLINE DIMENSIONS

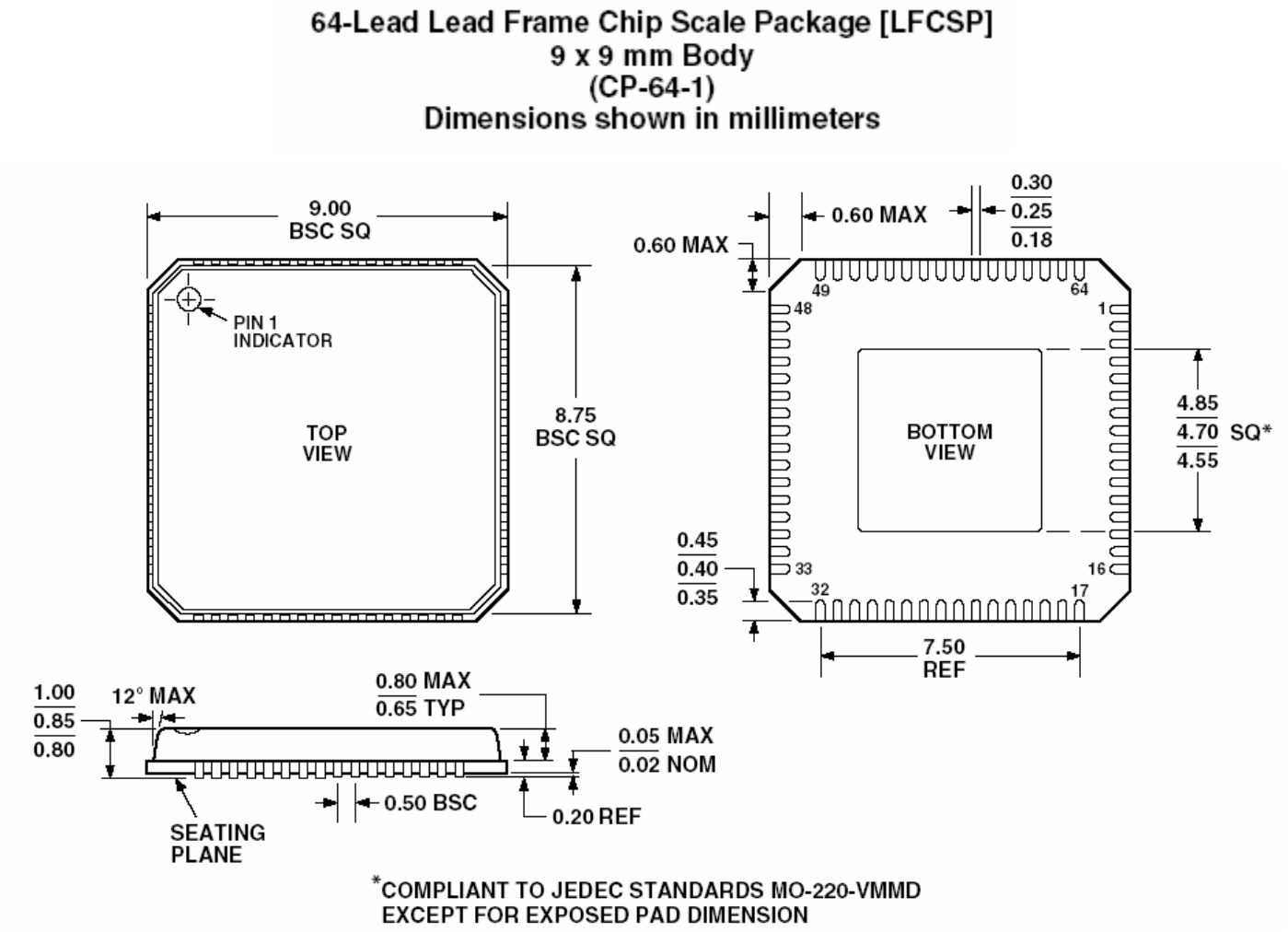
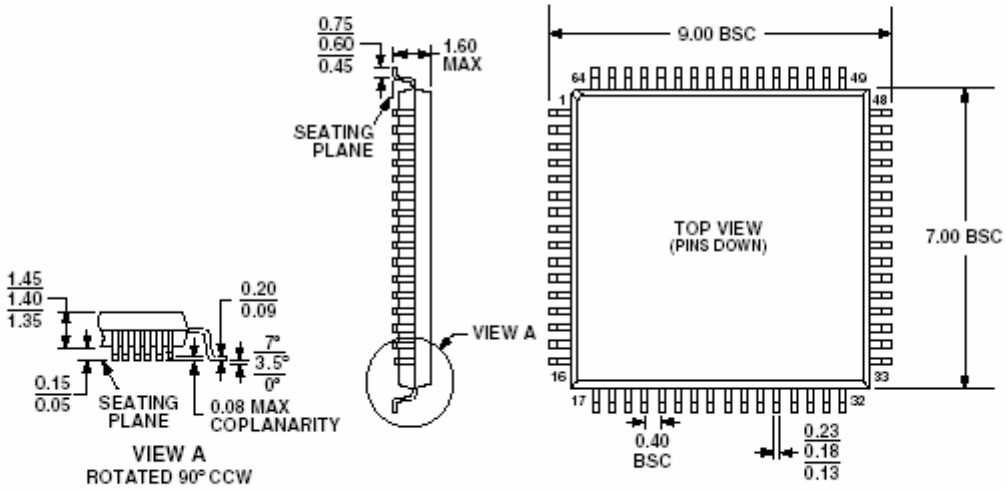


Figure 5. ***64-Lead Lead Frame Chip Scale Package (LFCSP)***

OUTLINE DIMENSIONS

64-Lead Quad Flat Pack [LQFP]
(ST-64)
Dimensions shown in millimeters



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